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GaAs DC/DC CONVERTERS

by

SHIHAB AL-KURAN

A dissertation submitted to the Graduate Faculty in Engineering in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York.

2000

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Abstract

GaAs DC/DC Converters

by

Shihab Al-Kuran

Advisor: Professor Norman Scheinberg

This thesis presents the results of a study on the design of GaAs DC/DC converters. The study began with a comparison between GaAs and Si technologies. Then it was explained why there is a need for GaAs DC/DC converters. In preparation for the design of GaAs DC/DC converter circuits, the most common switch-mode DC/DC converter topologies are presented in detail. Two GaAs circuit designs are then presented, both were fabricated in depletion-mode MESFET technology. Their results are introduced discussing their advantages and disadvantages.

Next, two of the practical applications where these converters are used are introduced. The first is a wireless power amplifier and the second is a transimpedance design.

Finally, some notes on possible future work are discussed.

Acknowledgment

I would like to thank my advisor Professor Norman Scheinberg, who introduced me to the group at Anadigics, Inc. This introduction gave me the opportunity to work with exceptional designers who possess a wealth of experience in designing GaAs and Si circuits. Norman's proven technical track record, along with his extraordinary designs and patents, gave me the enthusiasm and the confidence to become a major contributor in my field; GaAs DC/DC conversion. He always respected my ideas and reminded me to never give in to self-doubt. He challenged me with technical problems that intrigued me. These challenges led me to develop innovative solutions. Thank you, Norman.

I would also like to thank my parents, my brothers and my sisters, who gave me unconditional support throughout my schooling. This positive environment was crucial in pursuing my dreams. Therefore, this work is their dream as much as it is mine. Special thanks go to my supportive friends, who always stood by me and are a part of my extended family.

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1 CHAPTER I

Introduction

1.1 Introduction

Gallium-Arsenide (GaAs) integrated circuits are a main building block in today's communication circuits, high mobility and low noise figure makes them ideal for high frequency and low noise applications. GaAs integrated circuits are widely used in communication circuits, but rarely used in power supply circuits. Recent demand for higher levels of integration and smaller overall size has pressured GaAs IC manufacturers into considering the integration of communication and power supply circuits on one chip. This paper proposes to investigate different topologies of DC/DC converters and the features of these topologies that might lend themselves to GaAs technology. Some of these topologies will be fabricated in GaAs and their performance will be evaluated along with other communication circuits.

1.2 GaAs and Si, a brief comparison

GaAs is the technology of choice in many communication circuits. Some of the properties that make GaAs suitable for the fabrication of high frequency microwave devices are the high electron mobility and high peak velocity, Fig. 1.1. These translate into high frequency operation. In addition, the high resistivity of the semi-insulating GaAs substrate reduces parasitic effects and permits the fabrication of IC's that have high quality active and passive components, this is especially true in the case of inductors. On the other hand, GaAs has low hole mobility which limits its ability to support

complementary devices. Silicon (Si), on the other hand, has lower electron mobility and higher substrate conductivity, but the technology is more mature and the material is well characterized.

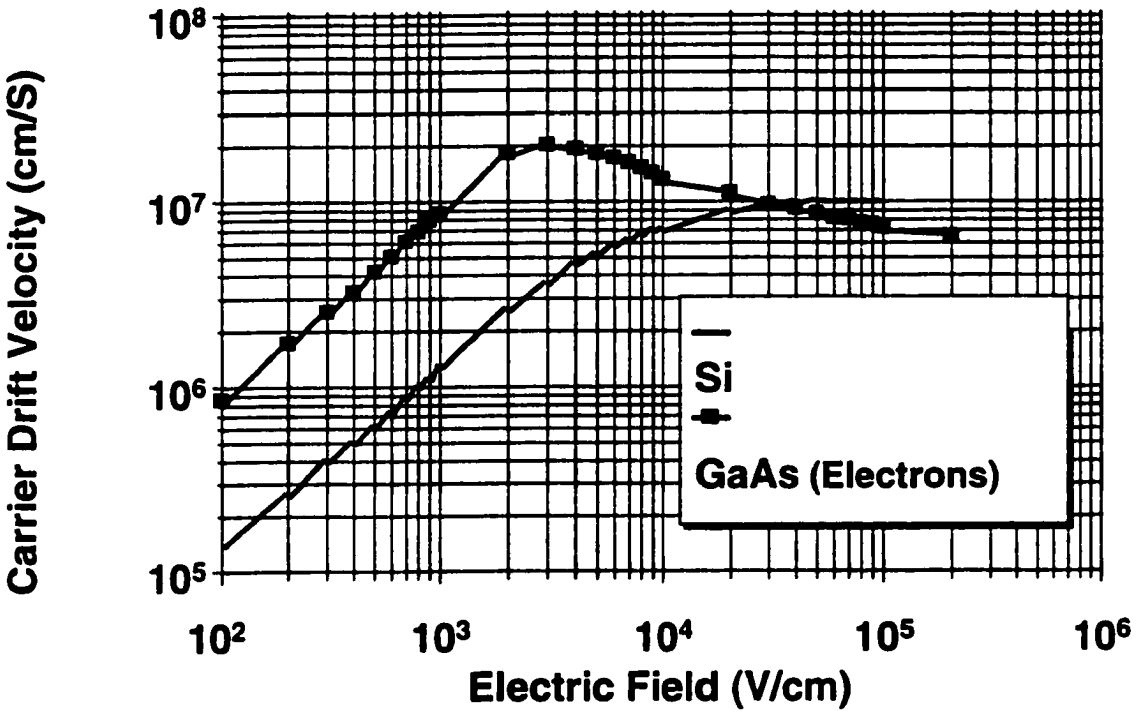

Fig. 1.1 Measured carrier velocity vs. electric field for high purity Si and GaAs.[2]

Mechanical strength and thermal conductivity is better than that of GaAs. Mechanical strength translates into larger wafer diameters, hence, Si wafers have diameters as large as 12 inches compared to 6 inches for GaAs. This makes Si IC's available in high quantities and at lower prices. Table 1 shows material properties of Si and GaAs. Another important property of Si, is the ability to grow high-quality oxide layers, allowing for the fabrication of MOSFET's, which have very low gate leakage current.

Property	Silicon	GaAs
Intrinsic resistivity (Ω.cm)	2.3×10^5	10^8
Dielectric constant	11.9	13.1
Thermal conductivity (W/cm.°K)	1.5	0.46
Bandgap at 300 °K (eV)	1.12	1.42
Electron mobility (cm^2 / V.s)	1500	8500
Hole mobility (cm^2 / V.s)	450	400
Maximum wafer diameter (in.)	12	6

Table 1.1 Material properties of Si and GaAs @ 300 °K.[2]

Fig. 1.2 shows a cross section of the devices available in the GaAs process used in fabricating the DC to DC converter. The process provides for MIM capacitors, spiral inductors, NiCr resistors, implanted resistors, Schottky diodes, and N-channel MESFET's. The MESFET's are 0.5μm recessed gate depletion mode FETS with a threshold voltage of -0.5 Volts and an F_t of about 20GHz.

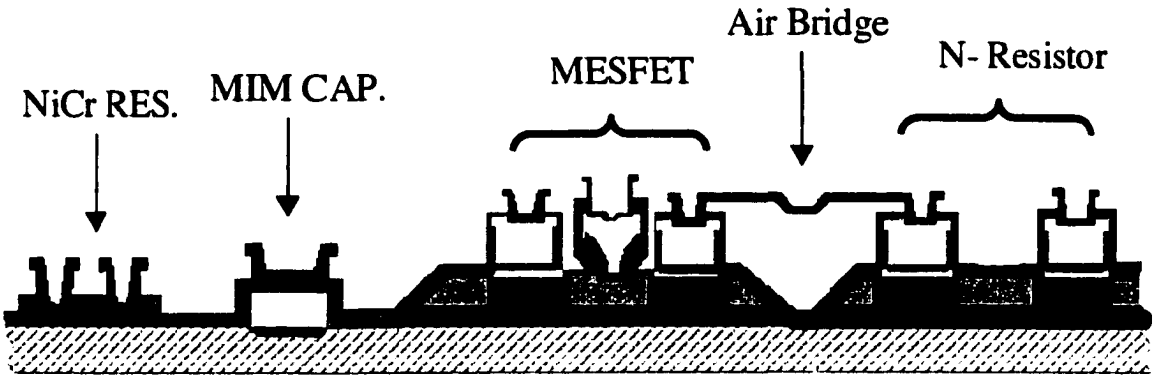

Fig. 1.2 X-section of GaAs devices structures.[1]

1.3 GaAs circuits and the need for DC to DC converters

Ion implanted GaAs MESFET's are of two types, enhancement and depletion mode. Depletion mode devices (D-MESFET's) have a much higher current density (Fig. 1.3) than the enhancement mode devices. Actually, enhancement mode MESFET's are quasi-depletion mode MESFET's with light doping so that the channel is depleted with Vgs=0 volts, resulting in a slightly positive pinch off voltage [2].

The D-MESFET's high current density and high breakdown voltages, make them ideal for high power communication circuits. Power amplifiers in wireless communication are often fabricated with D-MESFET's. As seen in Fig. 1.3, D-MESFET's have a negative pinch off voltage, and since, it is most convenient to ground the source, a negative supply voltage is used to turn the devices off, or to bias them at currents lower than IDSS. The positive supply is used for biasing the drains.

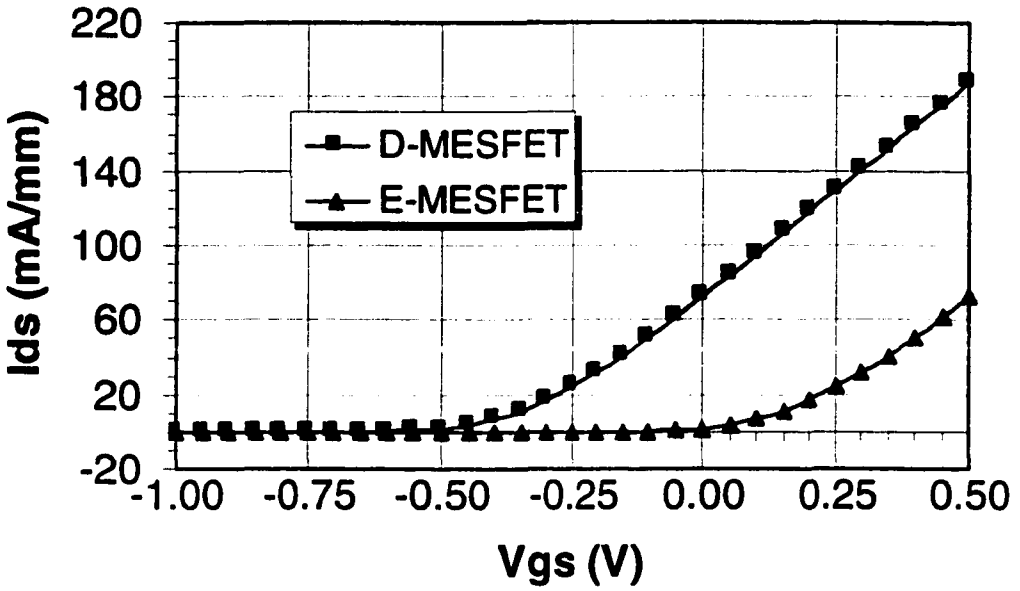

Fig. 1.3 IDS vs. VGS for a depletion mode MESFET and an enhancement mode MESFET.

Fig. 1.4 shows a simplified equivalent circuit of a GaAs MESFET, where the gate-source and gate-drain diodes are Schottky barrier with a turn-on voltage of about 0.7 V. The figure shows that the gate is not insulated, which leads to a clamping action if the gate voltage was more than 0.7 V higher than either source or drain voltages.

Fig. 1.5 shows a typical biasing structure for a depletion mode MESFET. The source is grounded for optimum noise performance and maximum gain, and the gate is negatively biased (-VG) through a large resistor. This arrangement allows for the maximum voltage VDS across the FET.

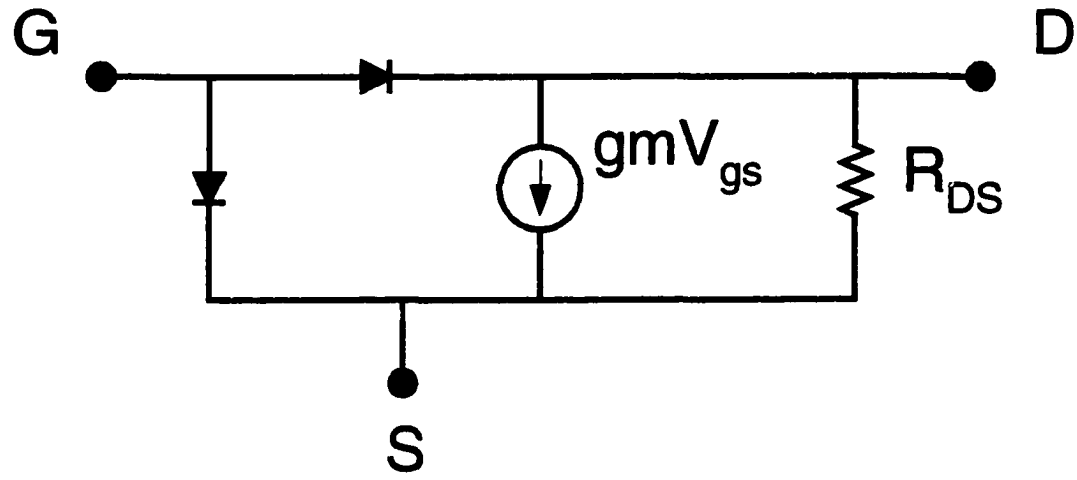

Fig. 1.4 Simplified dc equivalent circuit of a MESFET.

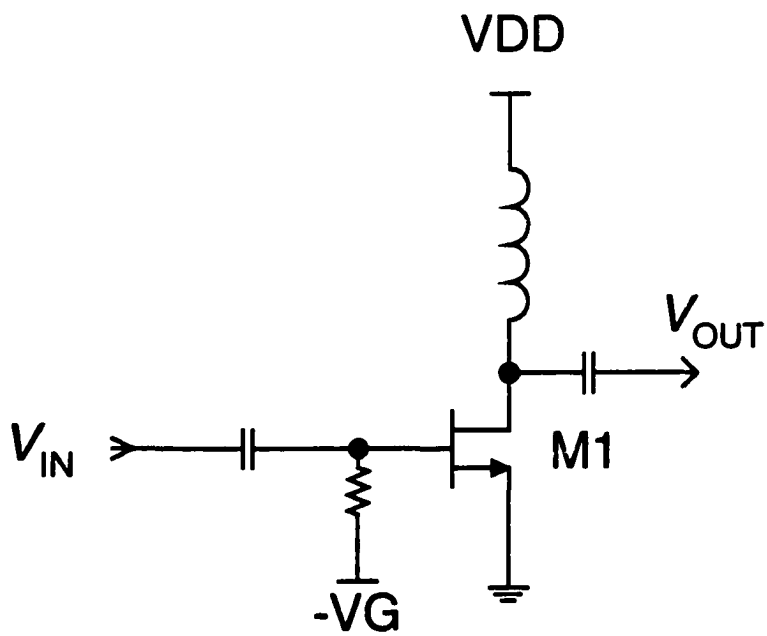

Fig. 1.5 A typical biasing arrangement of a D-MESFET.

Negative voltage is also used in current mirrors (Fig. 1.6). In this circuit M2 is connected as a current source and is connected to the negative voltage (VSS). The current through M3 is set by adjusting the value of R, and the gate voltage of M3 is applied to the gates of other FET's in the circuit.

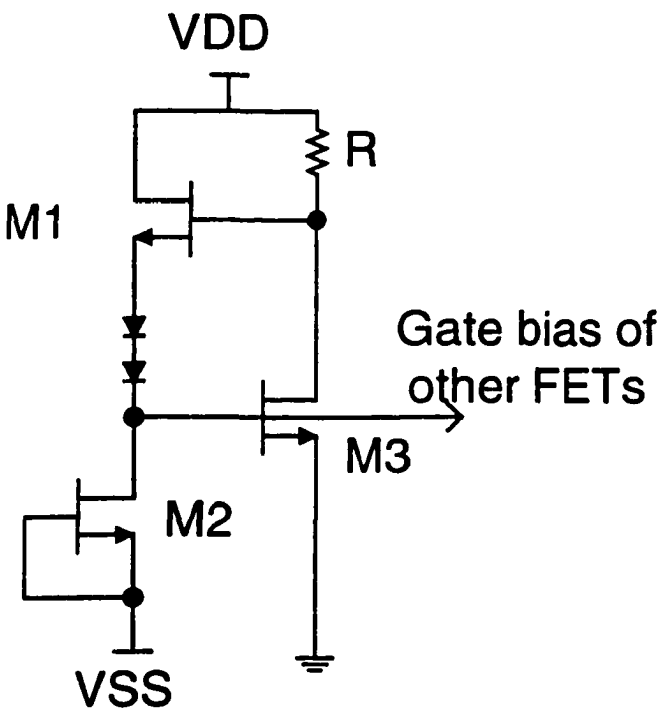

Fig. 1.6 Current mirror circuit that uses a negative voltage (VSS).

Negative voltage is also required for interstage level shifting as shown in Fig. 1.7. Interstage level shifters are required because the gate and drain voltages of D-MESFET's are not compatible voltage wise. The level shifting circuitry consists of a series of diodes connected between a source follower (M2) and a current source (M3) that is connected to

the negative voltage (VSS). This provides the DC level shifting between the drain of (M1) and the gate of (M4).

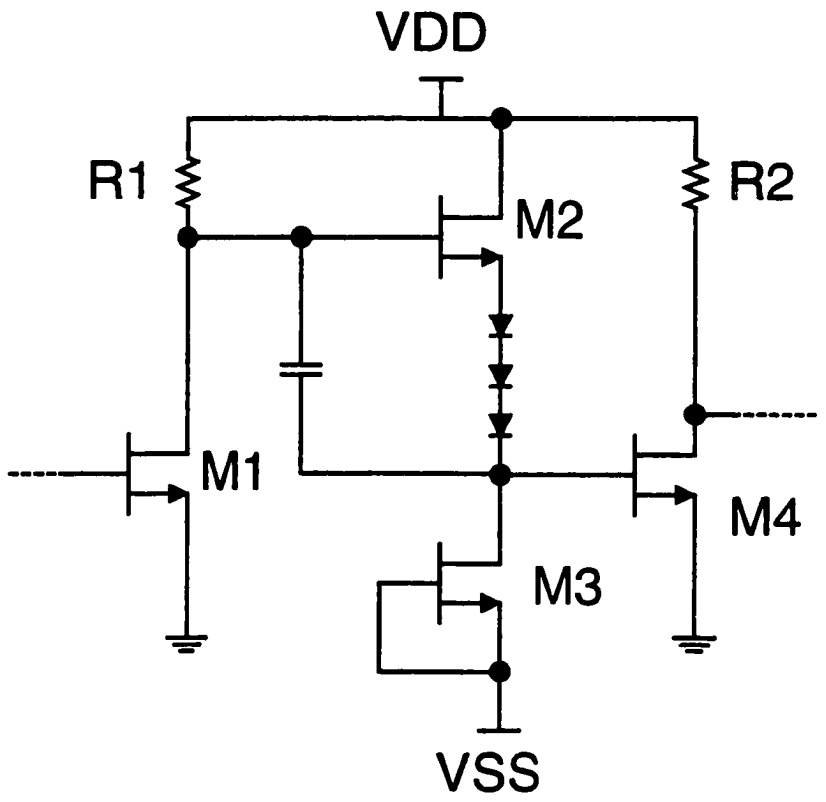

Fig. 1.7 Negative voltage (VSS) used in a level shifting circuit.

To supply this negative voltage, a Si DC to DC converter can be used but this leads to a two chip solution which is not compact.

Negative DC/DC converters are the most needed circuits to support GaAs circuits, but other types of DC/DC converters are of importance as well. One of these cases where a *positive* step-up DC/DC converter is used, is when a switch is used with GaAs circuits

(Fig. 1.8). Power supply switch transistors (called PASS transistors) are used with GaAs MESFET's, to ensure minimum leakage current when the circuit is off, which in the case of battery operated equipment like cellular phones translates into longer stand-by time. N-channel PASS transistors (N-MOSFET's) have lower ON resistance than P-channel ones for the same die size, but in order to get the lowest ON resistance in the n-type, the gate voltage (VSW) has to be set more positive than the drain voltage (VBAT) which is usually equal to the supply voltage. This calls for the need for step-up DC/DC converters or DC/DC doublers.

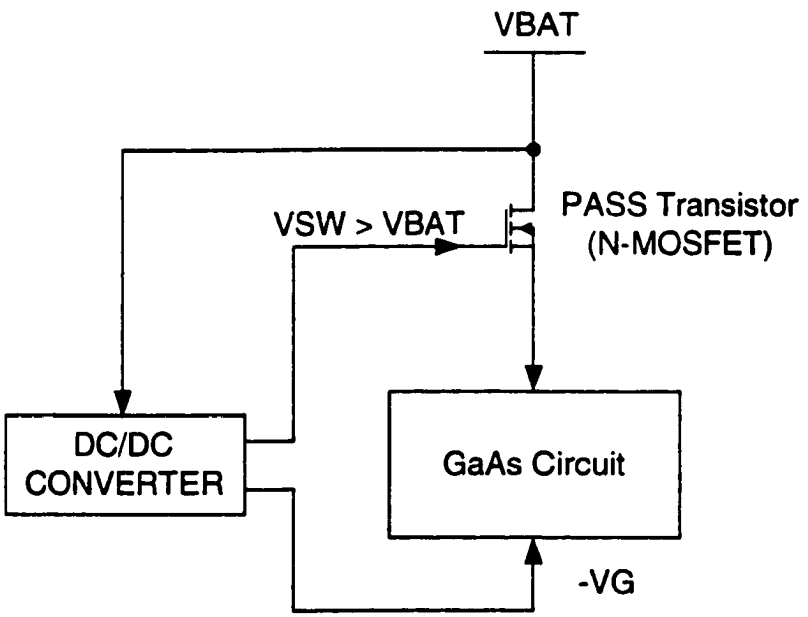

Fig. 1.8 Circuit diagram showing the use of the positive and negative voltages with a GaAs circuit.

Another application for step-up DC/DC converters is in low-voltage portable equipment, where both battery technology and digital IC's favor operation at low voltages, yet analog circuits do not have optimum performance at lower voltages, so, step-up DC/DC

converters are used to provide higher than the supply voltages for these analog sections to get higher performance.

Combining a communication circuit and a power supply circuit on the same die or as a hybrid in the same package can cause problems. Communication circuits are sensitive to noise, and power supply circuits tend to have either large switching voltages or large switching currents, both induce large EMI levels. Special ground planes and shielding mechanisms have to be implemented to reduce the level of interference. Receiver circuits are more prone to pick up noise from other adjacent circuits, since they operate on very low signal levels; transmitter circuits on the other hand, are more forgiving since the signal levels are much larger.

2 CHAPTER II

DC/DC Converter Topologies

2.1 Introduction

There are many classes and variations of DC/DC converters. In this chapter we will cover the major ones that lend themselves to high level of integration and can be operated in portable or hand held devices. Converters that require large magnetic devices such as transformers will be mentioned briefly but not analyzed.

2.2 Linear versus Switching Power Supplies

Historically, the linear power supply (Fig. 2.1) was the primary method of creating a regulated output voltage. It operates by reducing a higher input voltage down to the lower output voltage by linearly controlling the conductivity of a series power device or a pass unit. The control signal could be changing based on changes in the load. This results in a large voltage being placed across the pass unit with the full load current passing through it. This headroom loss causes the linear regulator or converter to be inefficient. Large percentage of the power lost is dissipated in the pass unit, which might require a heat sink. However, linear converters are cost effective for step-down applications.

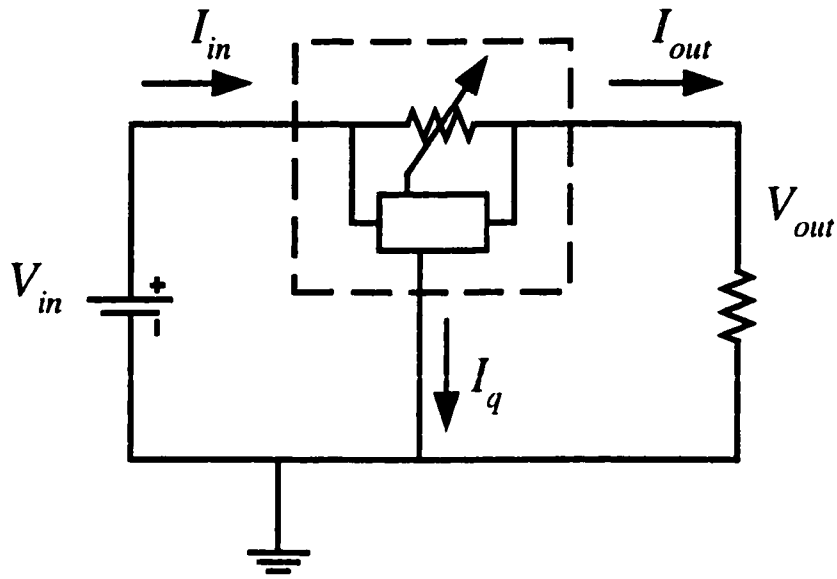

Fig. 2.1 Linear regulator

The power conversion efficiency in Fig. 2.1 is given by

$$\eta = \frac{P_{out}}{P_{in}} \tag{2.1}$$

and in terms of voltages and currents

$$\eta = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \tag{2.2}$$

But, I_q is usually much smaller than I_{in} and I_{out} , then

$$I_{in} \approx I_{out} \tag{2.3}$$

and

$$\eta \approx \frac{V_{out}}{V_{in}} \tag{2.4}$$

The efficiency changes linearly with the output voltage. It is desirable to have the efficiency independent of the load.

The switching converter operates the power device in the full-on and cutoff states. This then results in large currents being passed through the power device with a low "on" voltage or no current flowing with high voltage across the device. This results in much lower power being dissipated.

Higher levels of integration have driven the cost of switching power supplies downward and made them popular in most applications.

2.3 Buck Converter (positive and negative)

Buck converters are used to reduce or "step-down" a given voltage to an output voltage of the same polarity, this architecture can support multiple outputs. Positive (Fig. 2.2) and negative (Fig. 2.3) buck converters work in an identical manner. During the interval when the switch is on, the diode is reversed biased and the input supply provides energy to the load and to the inductor, when the switch opens current in the inductor continues to flow in the same direction forcing the diode into conduction and causing some of the inductor's stored energy to be transferred to the load.

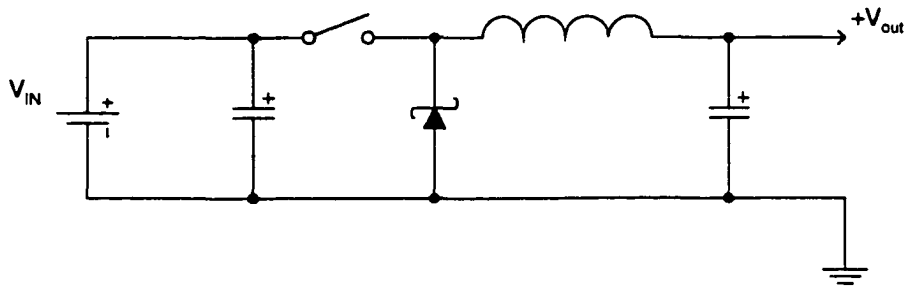

Fig. 2.2 Positive Buck (Step-Down)

Large values of inductance are needed for the inductors, hence they are difficult to integrate on a chip, and external inductors are used instead, which tend to be bulky and they emit high levels of EMI. Buck converters have relatively "noisy "

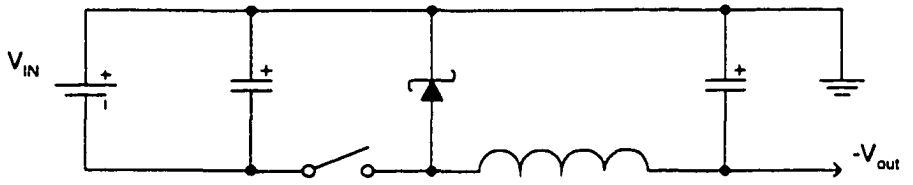

Fig. 2.3 Negative Buck (Step-Down)

input and a "quiet" output, that is due to the fact that the input current gets chopped and ends up having large AC components, while the output current has less AC components due to the presence of the inductor, where it impedes changes in the load current.

One of the key characteristics of a buck converter is the filtering action offered by the inductor. This acts to reduce the output voltage ripple and eliminates high amplitude harmonics, giving the buck converter the lowest output noise of any topology. The peak

switch, inductor, and diode currents are not much higher than the output current and maximum switch and diode voltages are slightly higher than the output voltage.

There are two modes of buck converter operation, continuous and discontinuous, where the reference is made to whether the inductor current reaches zero or not.

2.3.1 Positive Buck Circuit Operation

This section will describe the positive buck converter in detail. All components apply to the negative buck converter; simply invert the polarity of the input and output voltages.

A basic buck converter, along with its current and voltage waveforms, is shown in Fig. 2.4. The circuit operation is as follows: switch S1 opens and closes at a rate dependent upon the oscillator frequency. When the switch turns on, the V_{SW} node is pulled to the input voltage. Trace A is the V_{SW} node voltage waveform, and Trace B shows the switch current waveform. While the switch is on, current flows from the input through the switch and the inductor, and into the load. The inductor current (Trace C) rises linearly during this period. The change in inductor current, or ripple (ΔI), is determined by the voltage applied across the inductor, its inductance, and the switch-on time.

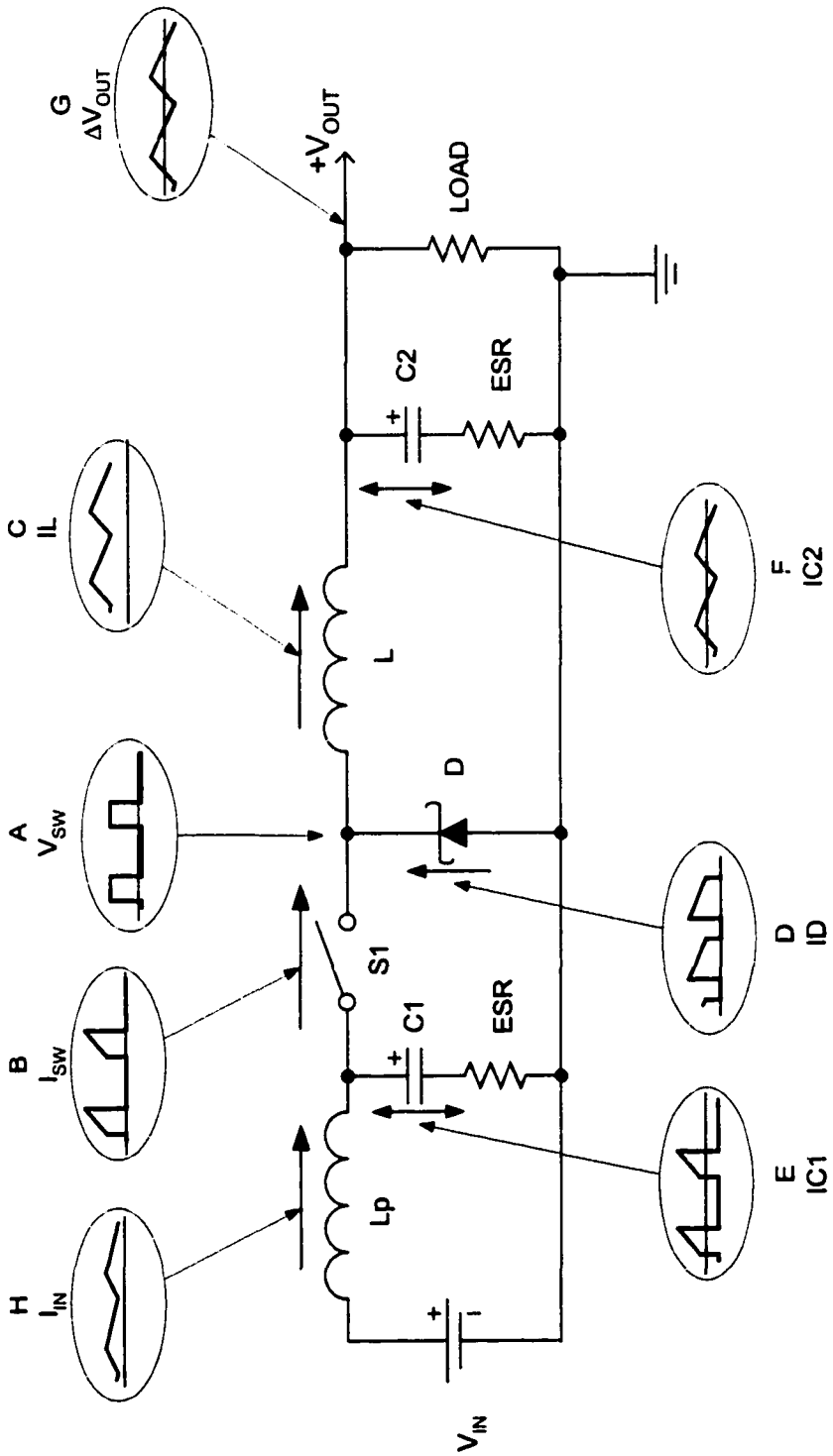

Fig. 2.4 Positive Buck Converter with its Voltage and Current Waveforms

When the switch opens, current flowing through the inductor forces the V_{SW} node voltage to drop until D1 (catch diode) becomes forward biased (Trace D), providing a path for the inductor current. The V_{SW} node is clamped to one diode drop below ground, and the inductor current begins ramping down. The slope of this ramp is a function of the inductance and the voltage across the inductor. The whole cycle repeats itself at the end of the switch off time.

The filter capacitors provide a low impedance path for the AC component of the input and diode currents. The input capacitor's current waveform (Trace E) is the same as the switch current (Trace B), except that the capacitor has no DC component. As a rule of thumb, the input capacitor RMS ripple current for a buck converter is equal to approximately ½ the DC output current. An input filter capacitor is essential for the proper operation of the circuit. It absorbs the current pulses inherent in a buck converter. Without an input filter capacitor close to the buck circuit, this ripple current in conjunction with lead and printed circuit trace inductances, could cause enough ripple voltage to produce erratic operation.

The output filter capacitor current waveform (Trace F) is the same as the inductor current, less the DC component. The RMS ripple current value is low, which makes it possible to use smaller capacitor for the output than for the input. However, a larger output capacitor may be necessary to reduce output voltage ripple.

The pulsating current found in switching converter circuits requires careful attention, High ripple currents in filter capacitors cause internal heat build-up. Circuit traces to the input capacitor, switch, and diode must be short to limit inductive spikes that could cause

erratic operation or, in the worst case, destructive breakdown. To illustrate this, let us consider a 300mA in 30 ns, which results in a current slew rate of 10A/μs. The voltage across the parasitic line inductance (LP in Fig. 2.4) is the product of slew rate and inductance. One inch of wire or printed circuit trace has an inductance of about 0.02μH. Simple multiplication yields 0.2V for each inch of wire.

Current and voltage waveforms of a continuous mode basic buck converter are shown in Fig. 2.5. While Fig. 2.6 shows the waveforms of a discontinuous mode. Continuous mode operation is described next in detail. It is preferred to discontinuous mode because it maximizes the available output power for a given converter. The difference between the two is in the characteristics of the inductor current. If the inductor current falls to zero during the switch-off time, the converter operates in the discontinuous mode, as shown in Fig. 2.6C. Continuous mode implies that the inductor is still carrying some current when the switch turns on, and the current never falls to zero. The discontinuous mode waveforms are lower in amplitude than the continuous mode waveforms because a fixed inductance value was assumed. With smaller inductance values, the discontinuous peak current will be considerably higher. Most designs "go discontinuous " when the output is lightly loaded.

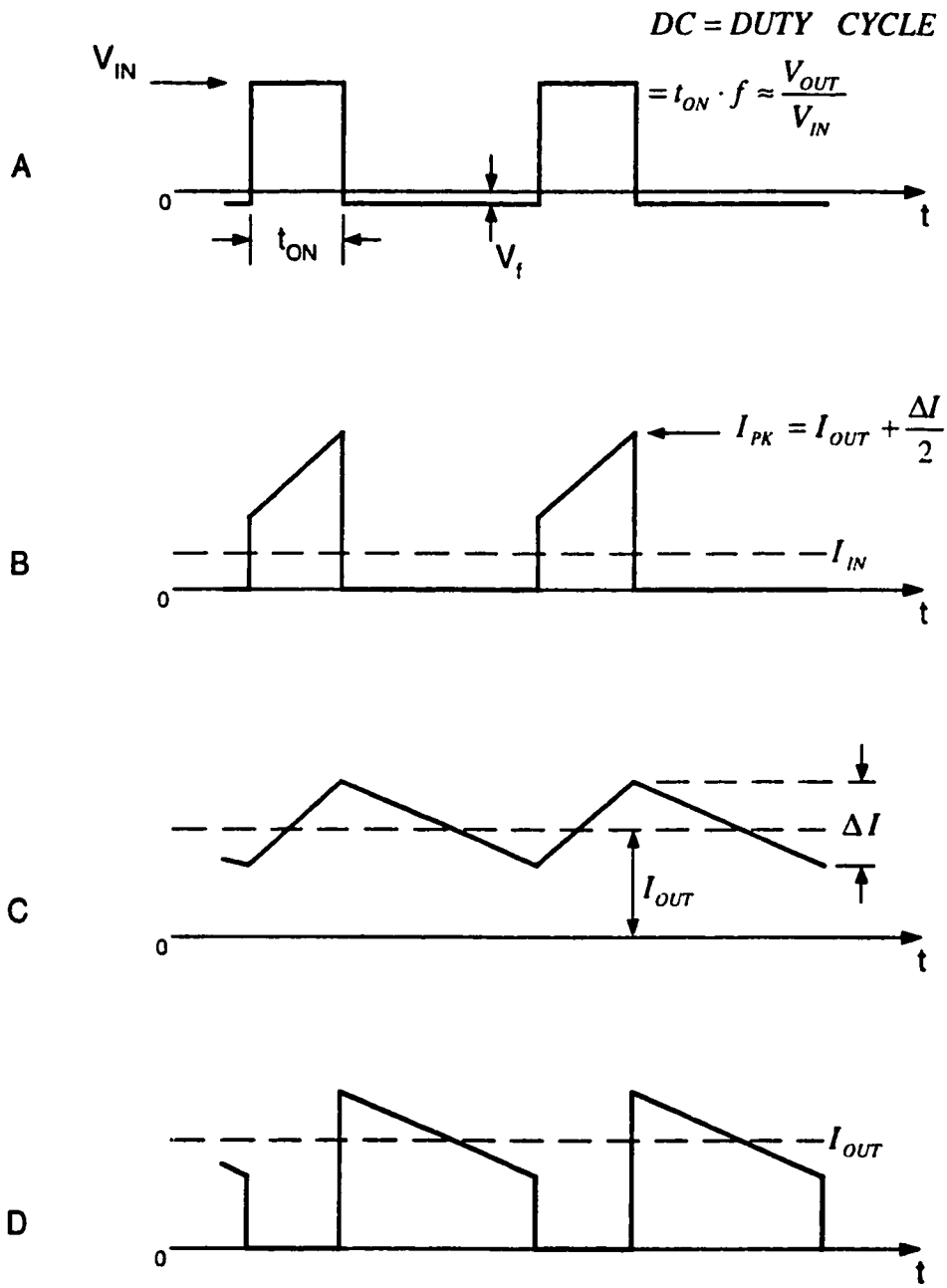

Fig. 2.5 Positive Buck Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

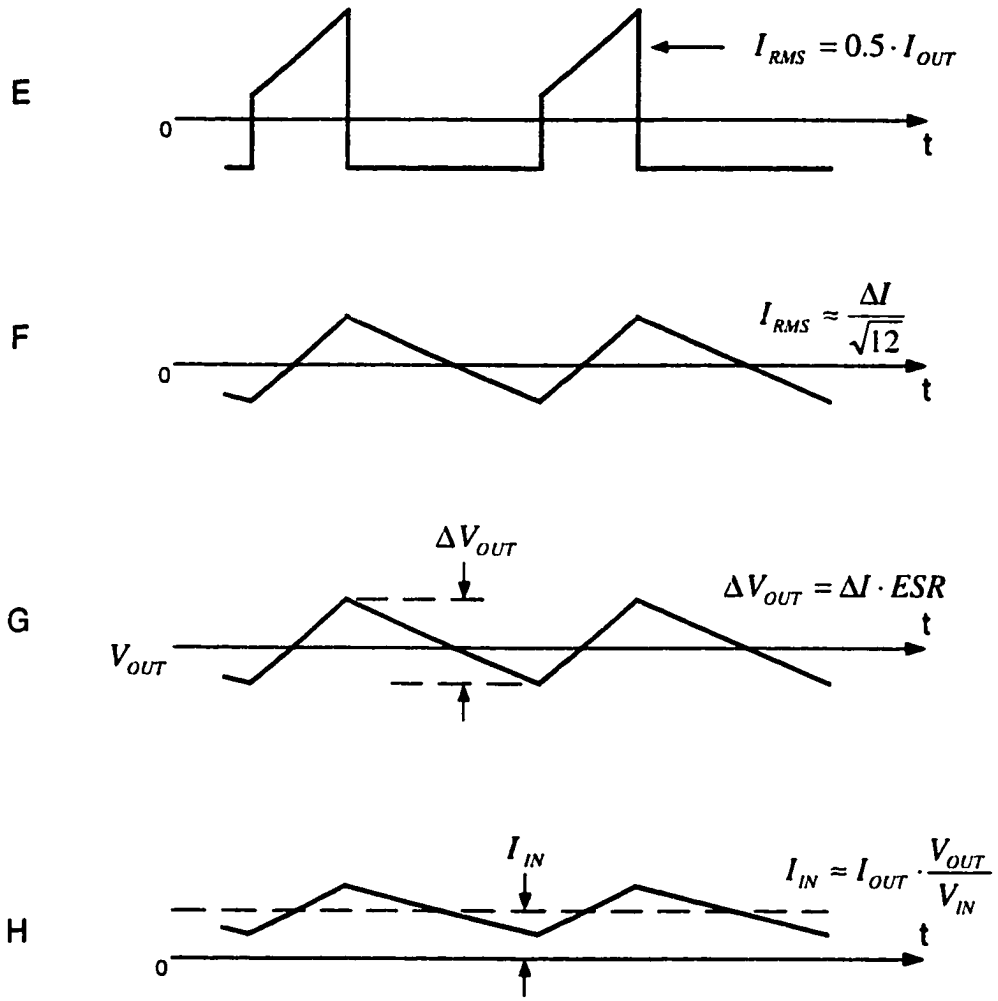

Fig. 2.5 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

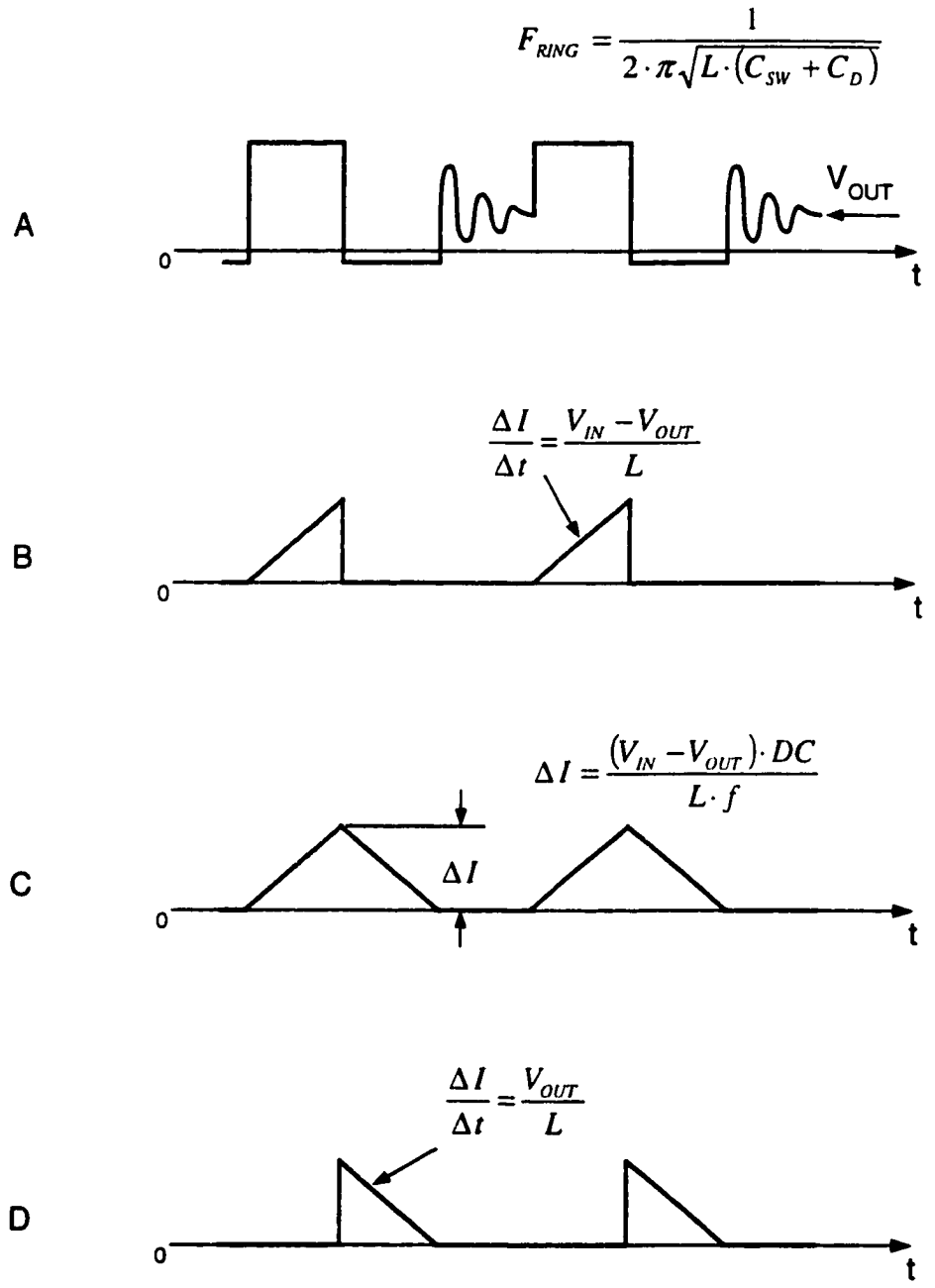

Fig. 2.6 Positive Buck Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

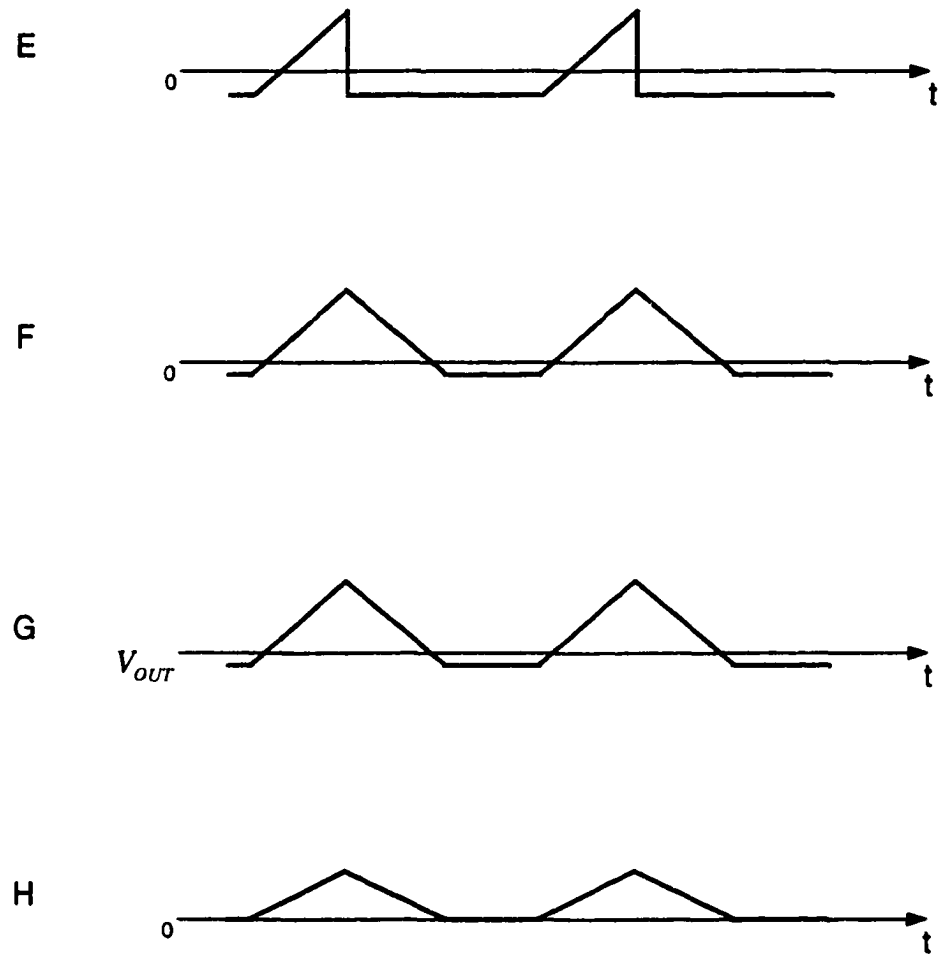

Fig. 2.6 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

The ringing shown in Fig. 2.6A is a characteristic of discontinuous mode and is not caused by loop oscillations or other circuit instabilities. Rather, the ringing is the result of a small amount of energy circulating between inductor and diode/switch parasitic capacitance. The ringing does no harm and damping it wastes energy. Because of its sinusoidal characteristics, it radiates very little energy, and hence does not cause electromagnetic interference (EMI) problems.

Switch Node Voltage: Fig. 2.5A, the voltage here switches between one diode drop below ground and input voltage (V_{IN}). This node is the major source of electric field radiation, so it should not be routed near sensitive nodes in the converter circuit. Trace widths to the switch, diode, and inductor must be wide enough to handle the high currents, but the areas should be minimized to avoid excess coupling or radiation.

Switch Current: Fig. 2.5B, the switch current steps from zero to an average value equal to load current. The slew rate is very high, so connections between the switch and other adjacent circuit elements must be short to prevent unwanted voltage spikes and parasitic resonances.

Inductor Current: Fig. 2.5C, the average inductor current is equal to load current. Peak-to-peak ripple current is determined mostly by inductance value and switching frequency, but it also changes with input voltage. Smaller inductance values result in higher ripple currents and increase core losses and output ripple voltage. Larger inductance values reduce these effects, but usually result in a physically larger coil.

Diode Current: Fig. 2.5D, the diode current switches from zero to a value approximately equal to load current. In most applications the average diode current is significantly less than the load current.

Input Capacitor Ripple Current: Fig. 2.5E, the peak-to-peak value of the input capacitor ripple current is approximately equal to the DC load current. The RMS equivalent is about ½ the DC load current.

Output Capacitor Ripple Current: Fig. 2.5F, the output capacitor absorbs the inductor ripple current. The RMS ripple current is approximately 0.3 times the peak-to-peak value.

Output Ripple Voltage: Fig. 2.5G, the output ripple voltage is determined by inductor ripple current and the ESR of the output capacitor. The capacitive reactance is usually considered a short at the switching frequencies, leaving the effective series resistance (ESR) is the only impedance.

Input Current: Fig. 2.5H, input current normally appears as a moderate amount of ripple superimposed on an average DC level because the input capacitor absorbs most of the AC ripple current created by the switching operation. L_P is the equivalent parasitic inductance of the input lines, which aids in the filtering action. Ripple current in the input lines is one cause of EMI, so the magnitude of this current is important.

2.3.2 Negative Buck Circuit Description

Fig. 2.7 shows the negative buck converter, along with its current and voltage waveforms. The operating waveforms are identical to those of Fig. 2.4, with the exception of polarity.

Fig. 2.8 shows the current and voltage waveforms of a continuous mode negative buck converter. Fig. 2.9 shows the discontinuous mode waveforms.

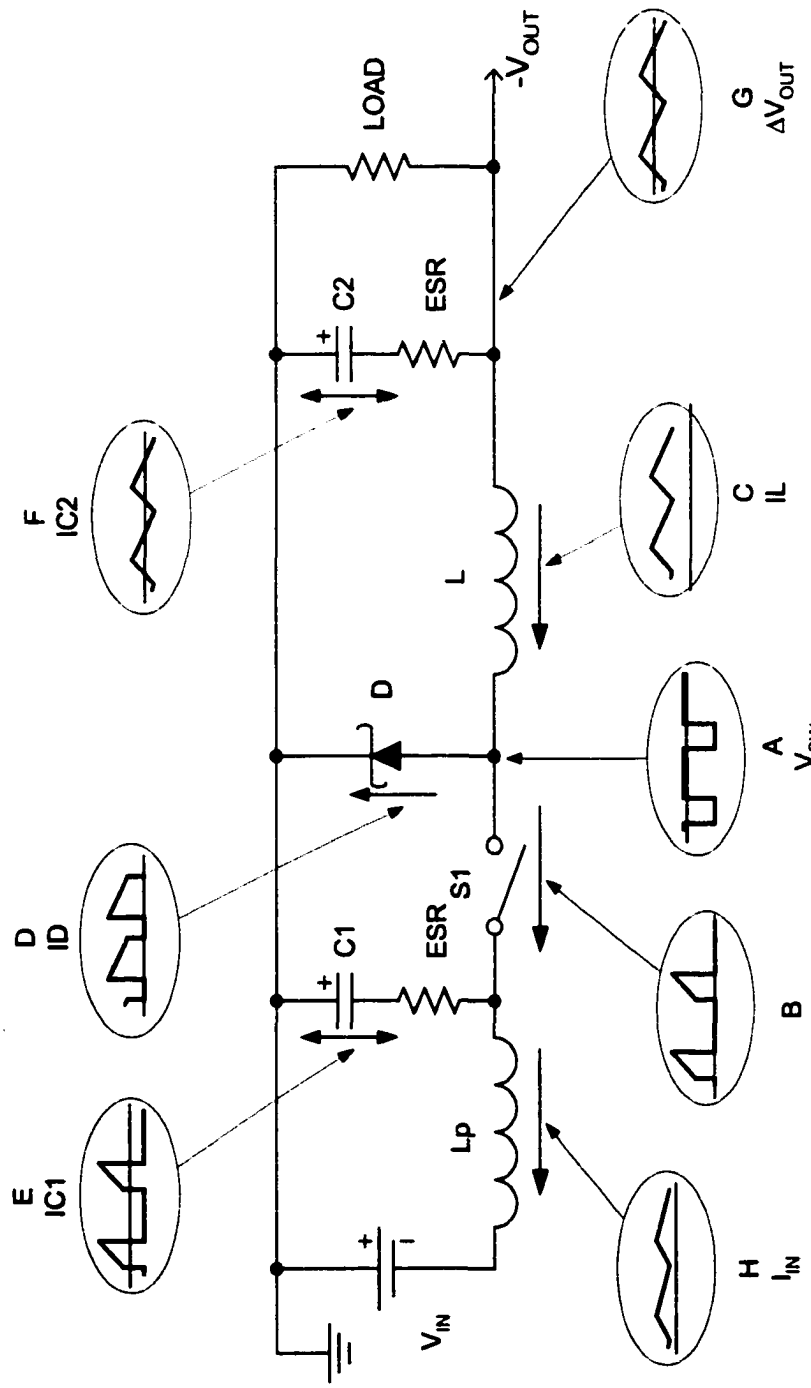

Fig. 2.7 Negative Buck Converter with its Current and Voltage Waveforms

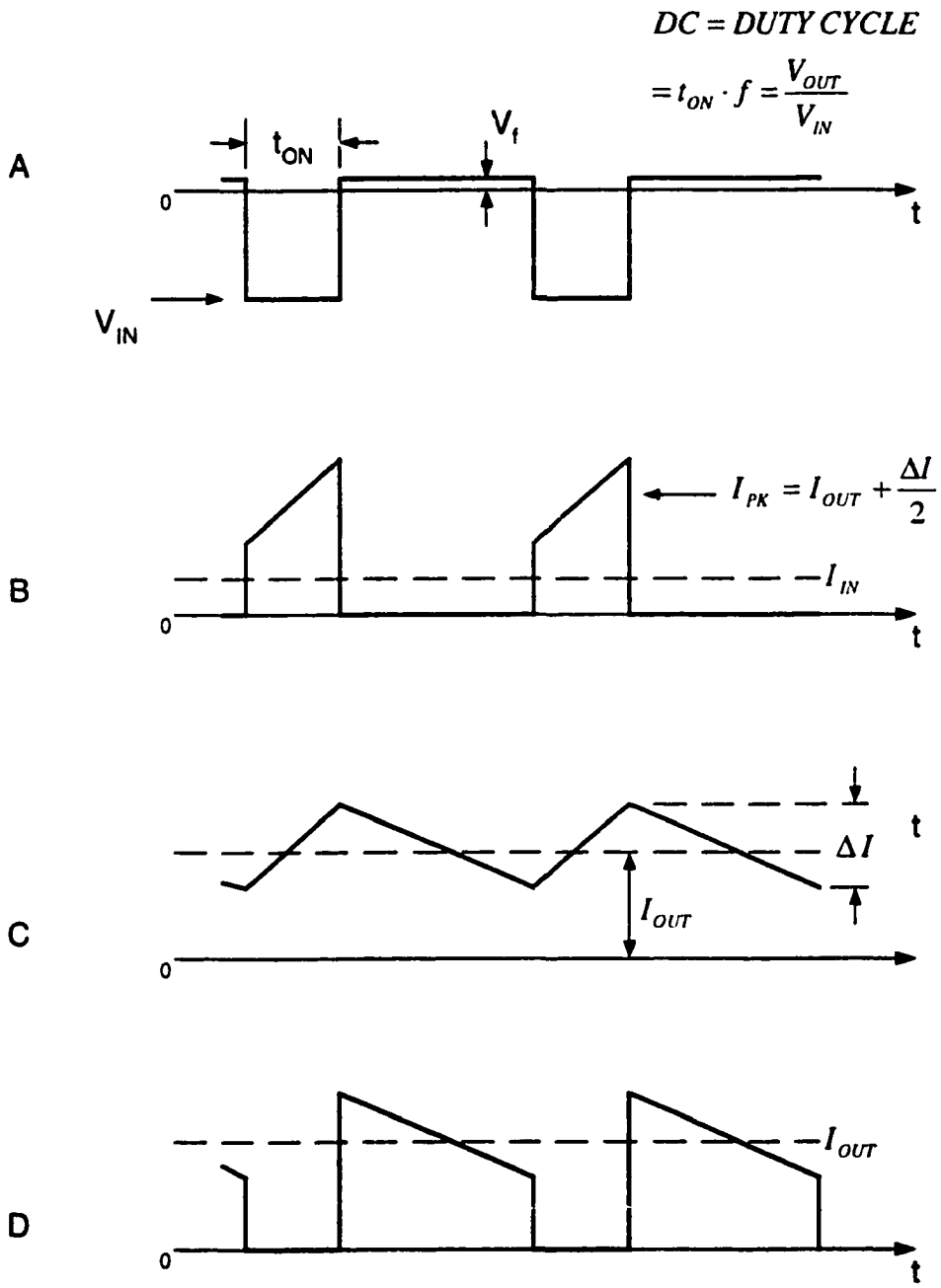

Fig. 2.8 Negative Buck Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

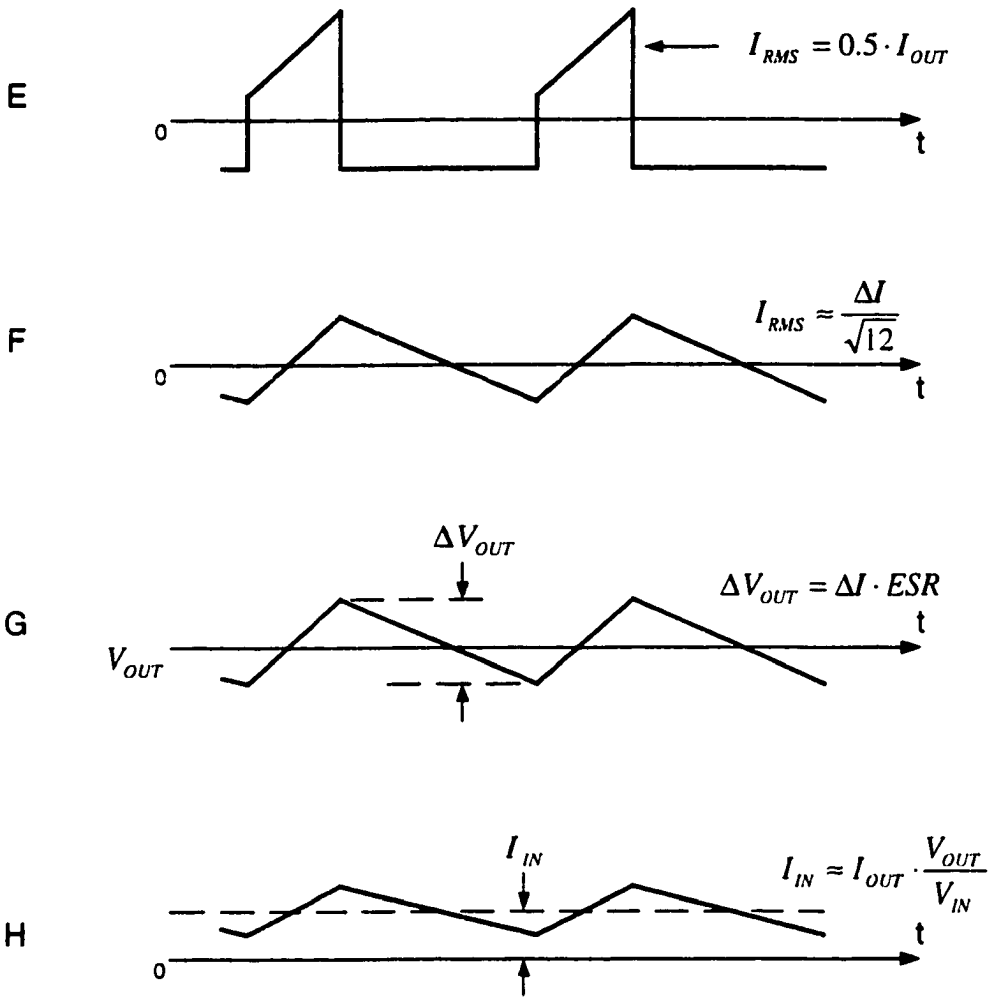

Fig. 2.8 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

$$F_{RING} = \frac{1}{2 \cdot \pi \sqrt{L \cdot (C_{SW} + C_D)}}$$

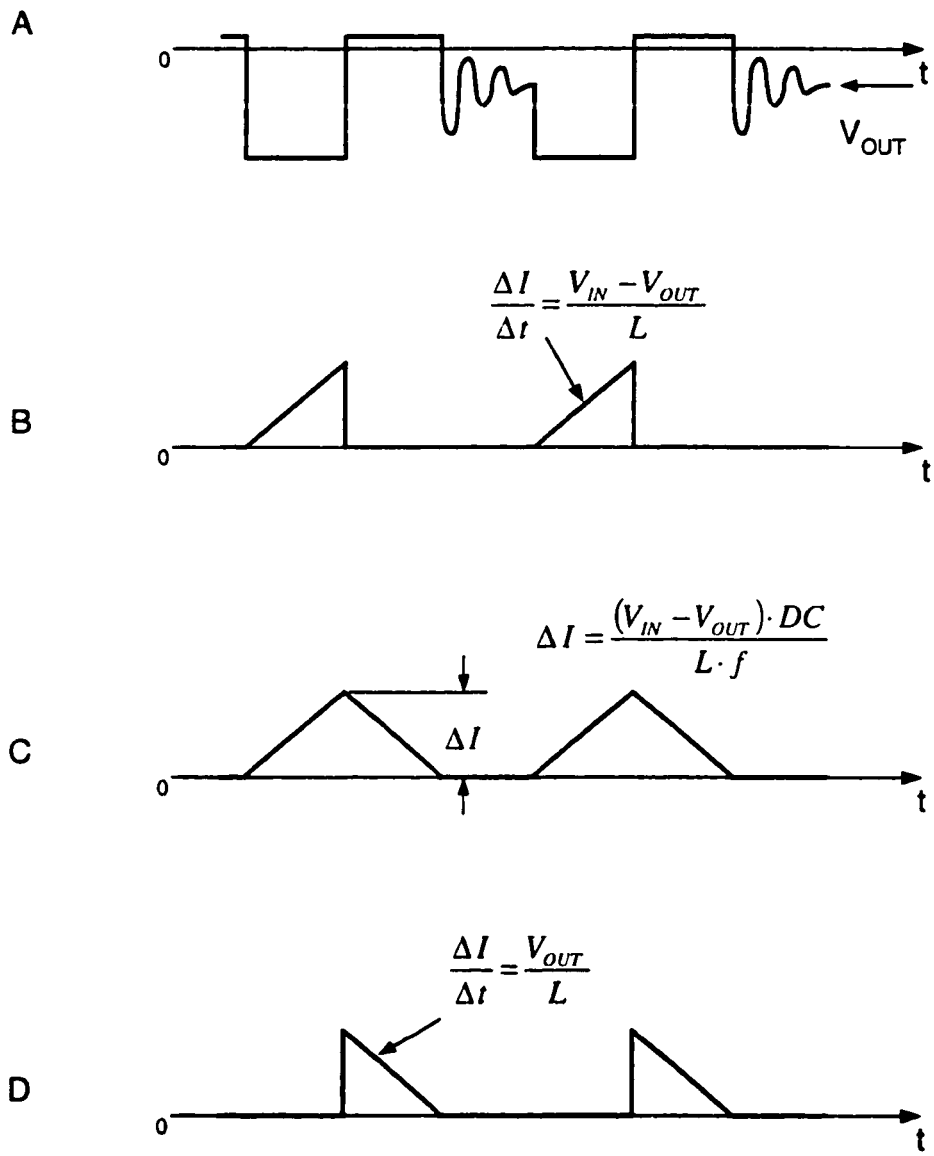

Fig. 2.9 Negative Buck Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

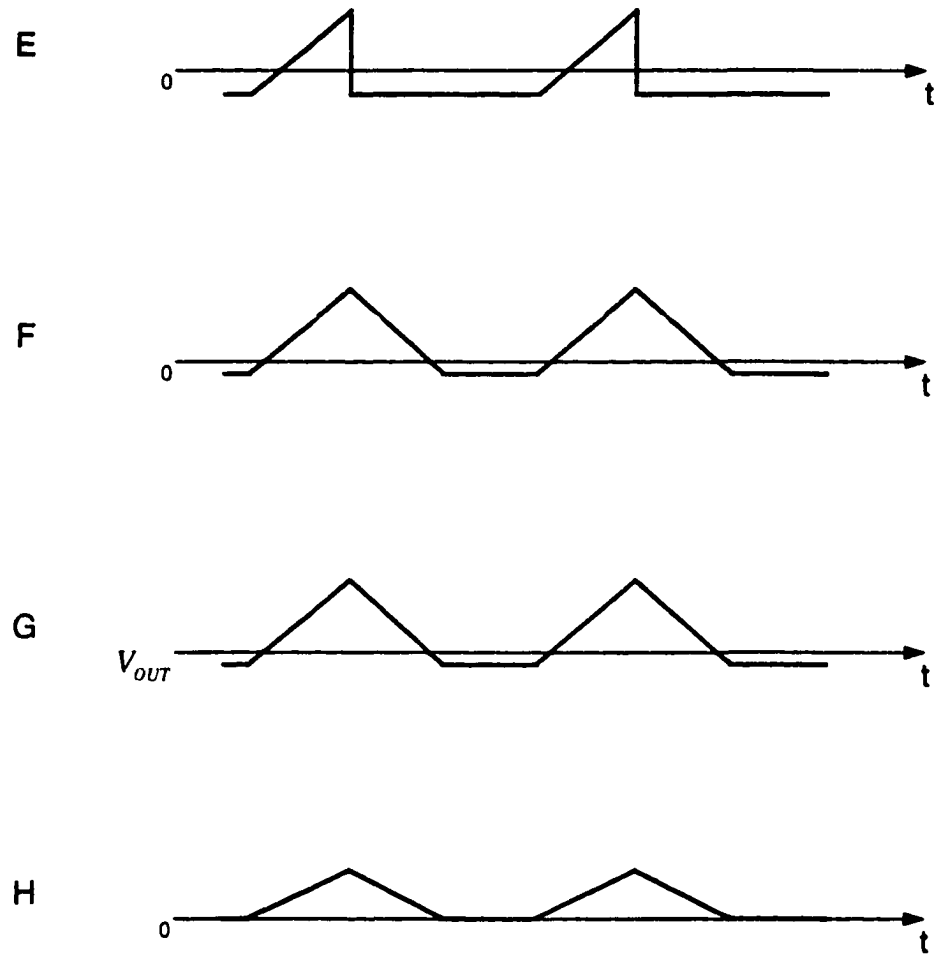

Fig. 2.9 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

2.4 Boost Converter (positive and negative)

Boost converters always produce an output voltage that is higher than the input voltage, there are two possible boost architectures; one for positive inputs (Fig. 2.10) and one for negative inputs (Fig. 2.11). Those topologies are mirror images of each other, but work identically. They are extremely popular in battery-powered applications because they can minimize the number of batteries used.

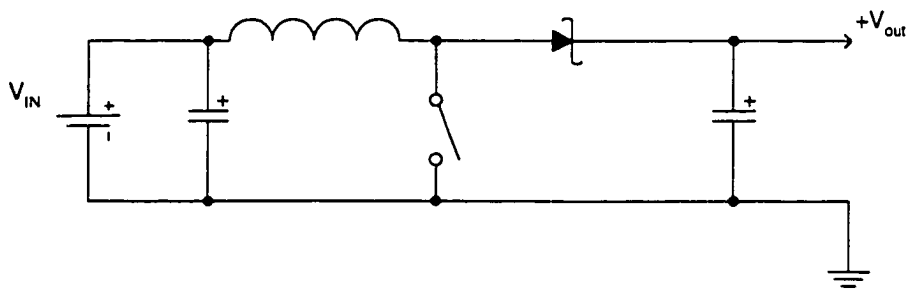

Fig. 2.10 Positive Boost (Step-Up)

During the switch-on time, the input voltage is applied across the inductor providing energy to the inductor. During this interval the diode is reversed biased and no energy is being supplied to the output filter capacitor. When the switch opens, the diode is forward biased and the energy stored in the inductor is transferred to the output. Since one side of the inductor continuous to draw current from the input and deliver it to the load.

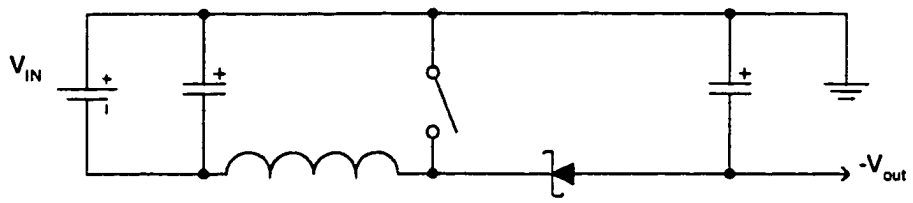

Fig. 2.11 Negative Boost (Step-Up)

Boost converters have relatively "quiet " input and a "noisy" output, that is due to the fact that the output current gets chopped and is steered between the inductor and the capacitor and ends up having large AC components, while the input current has less AC components due to the presence of the inductor, where it impedes changes in the load current.

The biggest advantage of this architecture is that it can boost the input voltage by as much as a factor of 10 without the use of a transformer. Inductors are more economical than transformers in many converter designs and they are readily available. If higher output voltages, multiple outputs, or isolation are required, a flyback converter with a transformer are used.

One drawback of boost converters is that they cannot be current limited for output shorts, because the output diode makes a direct connection between the input and the output. Fuses or circuit breakers must be used if the input supply is not limited and true short circuit is needed.

2.4.1 Positive Boost Circuit Operation

This section will describe the positive boost converter in detail, all comments apply to the negative boost converter; where the polarity of the input and the output voltages are inverted.

A basic boost converter, along with its current and voltage waveforms, is shown in Fig. 2.12. The circuit operation is as follows: switch S1 opens and closes at a rate dependent upon the IC oscillator frequency. When the switch turns on, the V_{SW} node is pulled to ground. Trace A is the V_{SW} node waveform, and trace B is the switch current waveform. While the switch is on, current flows from the input and through the inductor and into the switch. During this interval, no current is being provided by the inductor to the load. The inductor current (Trace C) rises linearly during this period. The change in inductor current or ripple (ΔI) is determined by the input voltage, inductance and switch-on time.

When the switch opens, current flowing through the inductor forces the V_{SW} node voltage to increase until D1 (the catch diode) becomes forward biased (Trace D) providing a path for the inductor current. The V_{SW} node is clamped to one diode drop above the output voltage and the inductor current begins ramping down. The slope of this ramp is a function of the inductance and the input to output voltage difference. The whole cycle repeats itself at the end of the switch-off time.

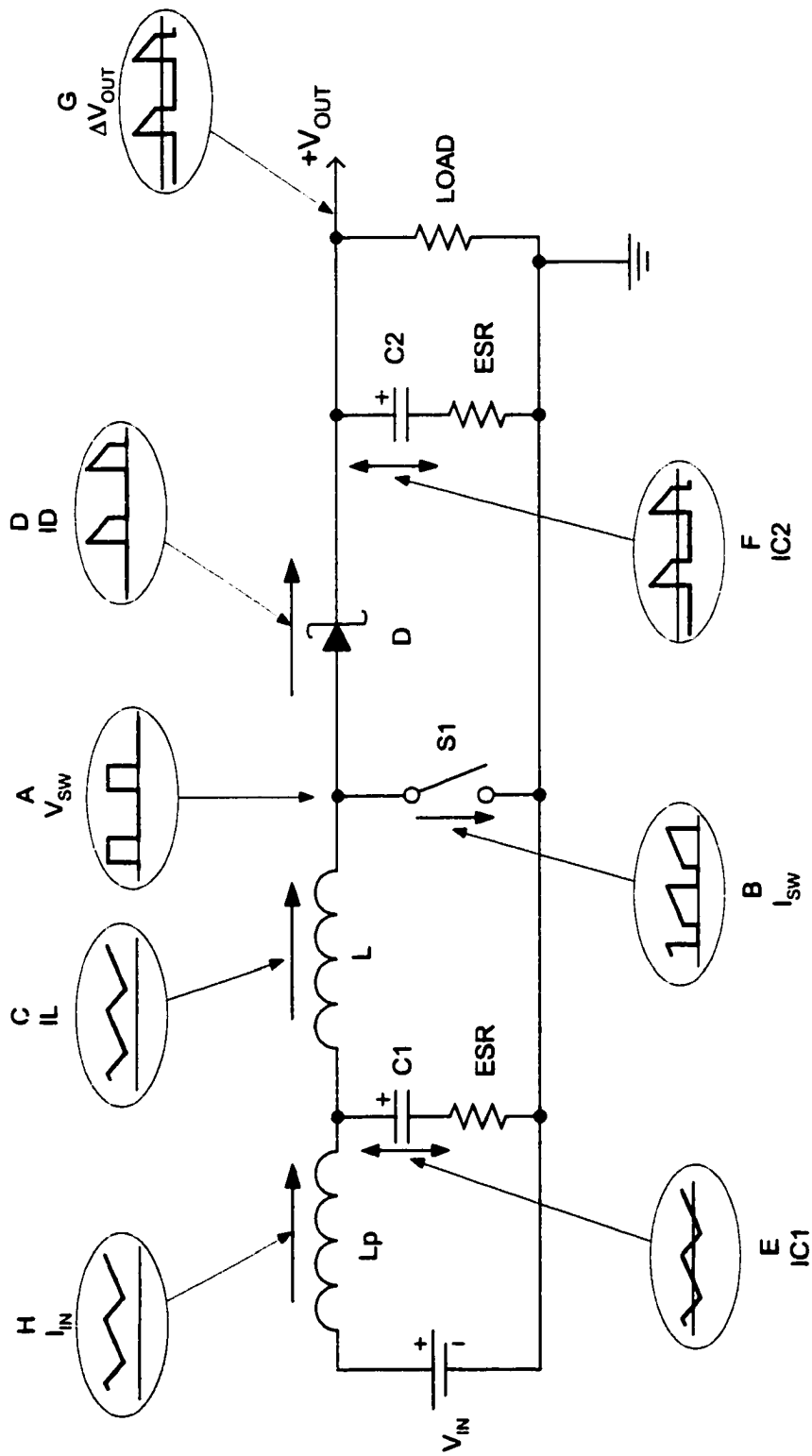

Fig. 2.12 Positive Boost Converter with its Current and Voltage Waveforms

The filter capacitors provide a low impedance path for the AC components of the input and output current. The input capacitor's current waveforms (Trace E) are the same as the inductor current waveform (Trace C), except that the capacitor current has no DC component. The input capacitor RMS ripple current is equal to approximately 0.3 times the inductor's peak-to-peak ripple current (ΔI). An input filter capacitor is essential for the proper operation of the circuit. It absorbs the ripple current inherent in the boost converter's input.

The output filter capacitor current waveform (Trace F) is the same as the diode current waveform, less the DC component. The RMS ripple current in the output capacitor is equal to the output current when the input voltage is half the output voltage. It increases as the input voltage is reduced.

Current and voltage waveforms of a continuous mode basic boost converter are shown in Fig. 2.13. While Fig. 2.14 shows the waveforms of a discontinuous mode. Continuous mode operation is described next in detail. It is preferred to discontinuous mode because it maximizes the available output power for a given converter. The difference between the two is in the characteristics of the inductor current. If the inductor current falls to zero during the switch-off time, the converter operates in the discontinuous mode, as shown in Fig. 2.14C. Continuous mode implies that the inductor is still carrying some current when the switch turns on, and the current never falls to zero. The discontinuous mode waveforms are lower in amplitude than the continuous mode waveforms because a fixed inductance value was assumed. With smaller inductance values, the discontinuous

peak current will be considerably higher. Most designs "go discontinuous " when the output is lightly loaded.

As in the case of the buck converter, the ringing shown in Fig. 2.14A is a characteristic of discontinuous mode and is not caused by loop oscillations or other circuit instabilities. Rather, the ringing is the result of a small amount of energy circulating between inductor and diode/switch parasitic capacitance. The ringing does no harm and damping it wastes energy. Because of its sinusoidal characteristics, it radiates very little energy, and hence does not cause electromagnetic interference (EMI) problems.

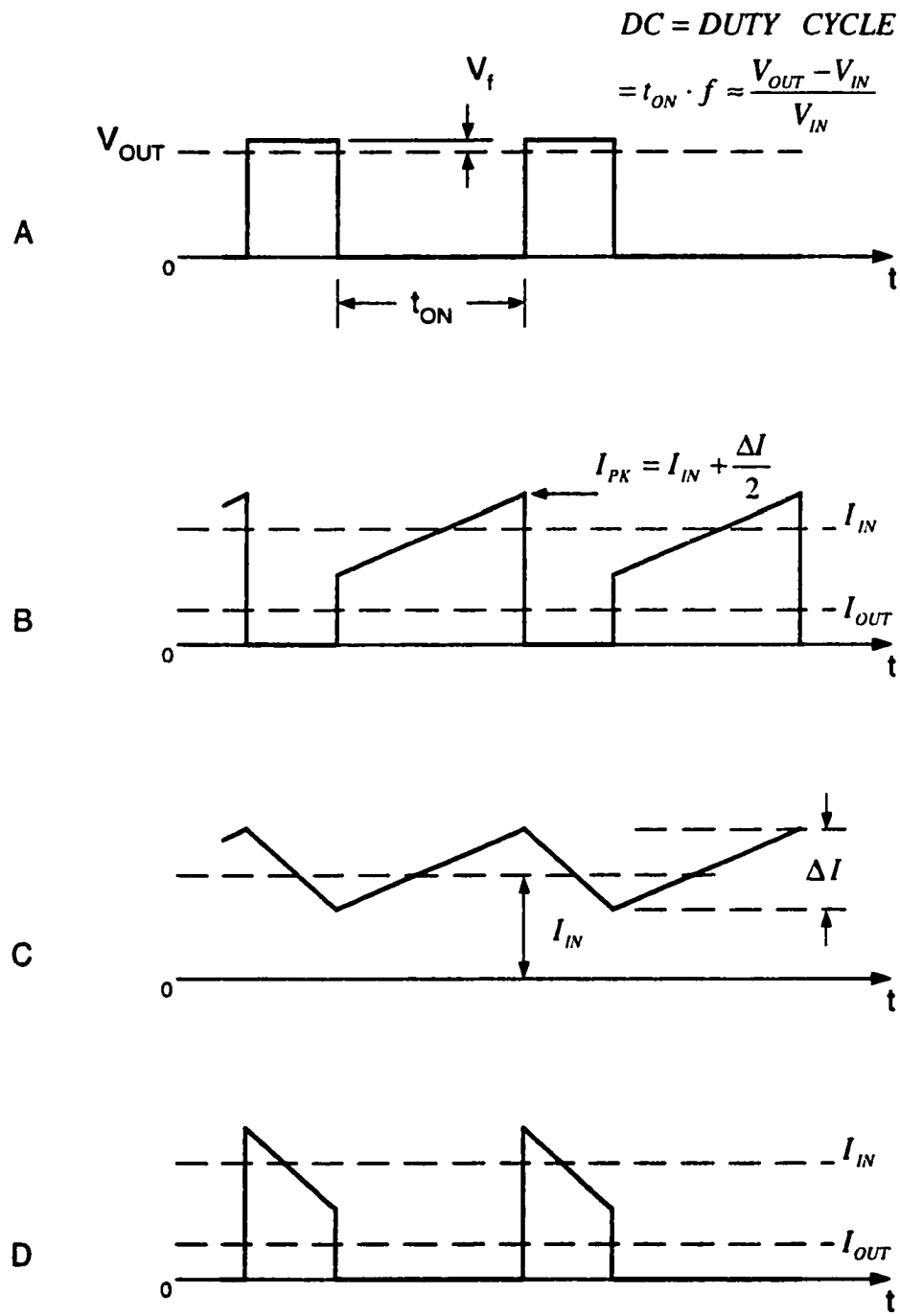

Fig. 2.13 Positive Boost Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

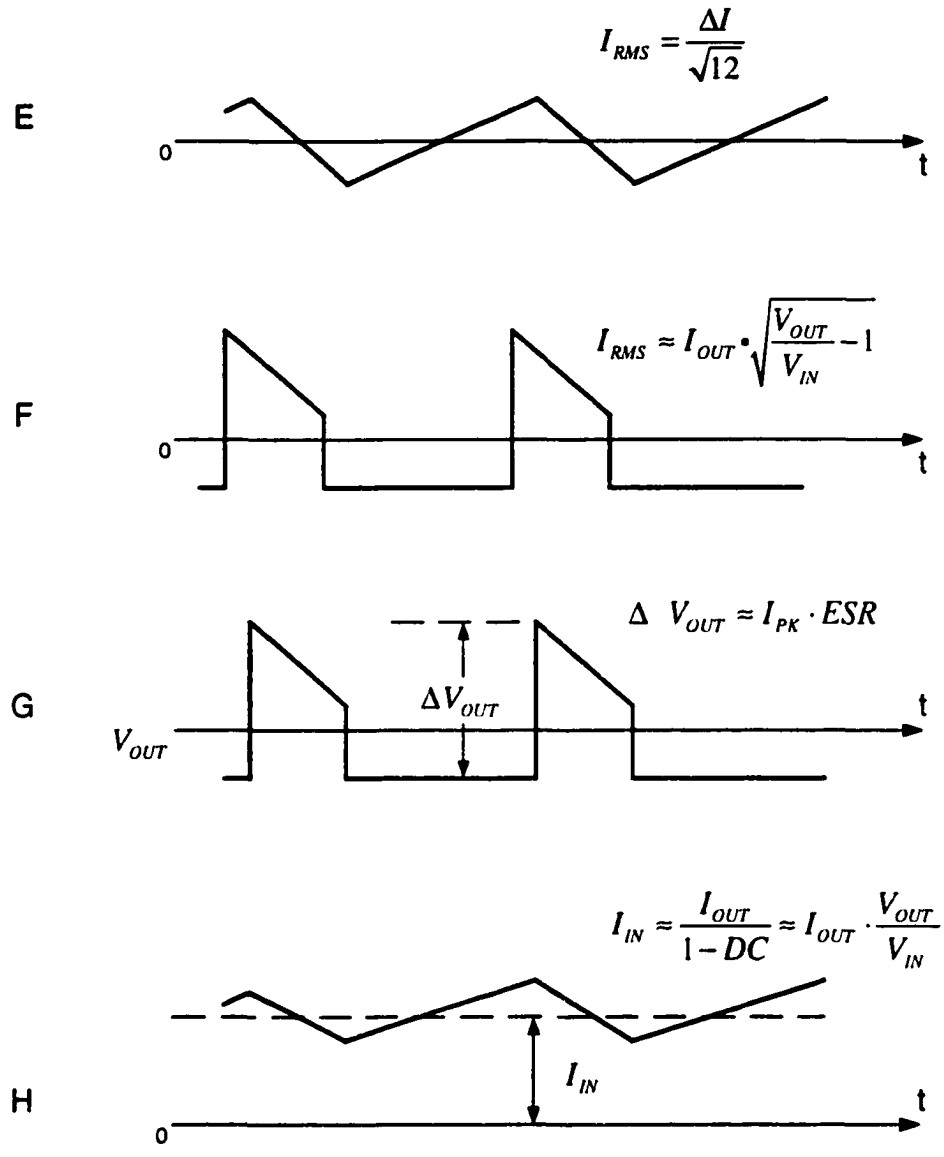

Fig. 2.13 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

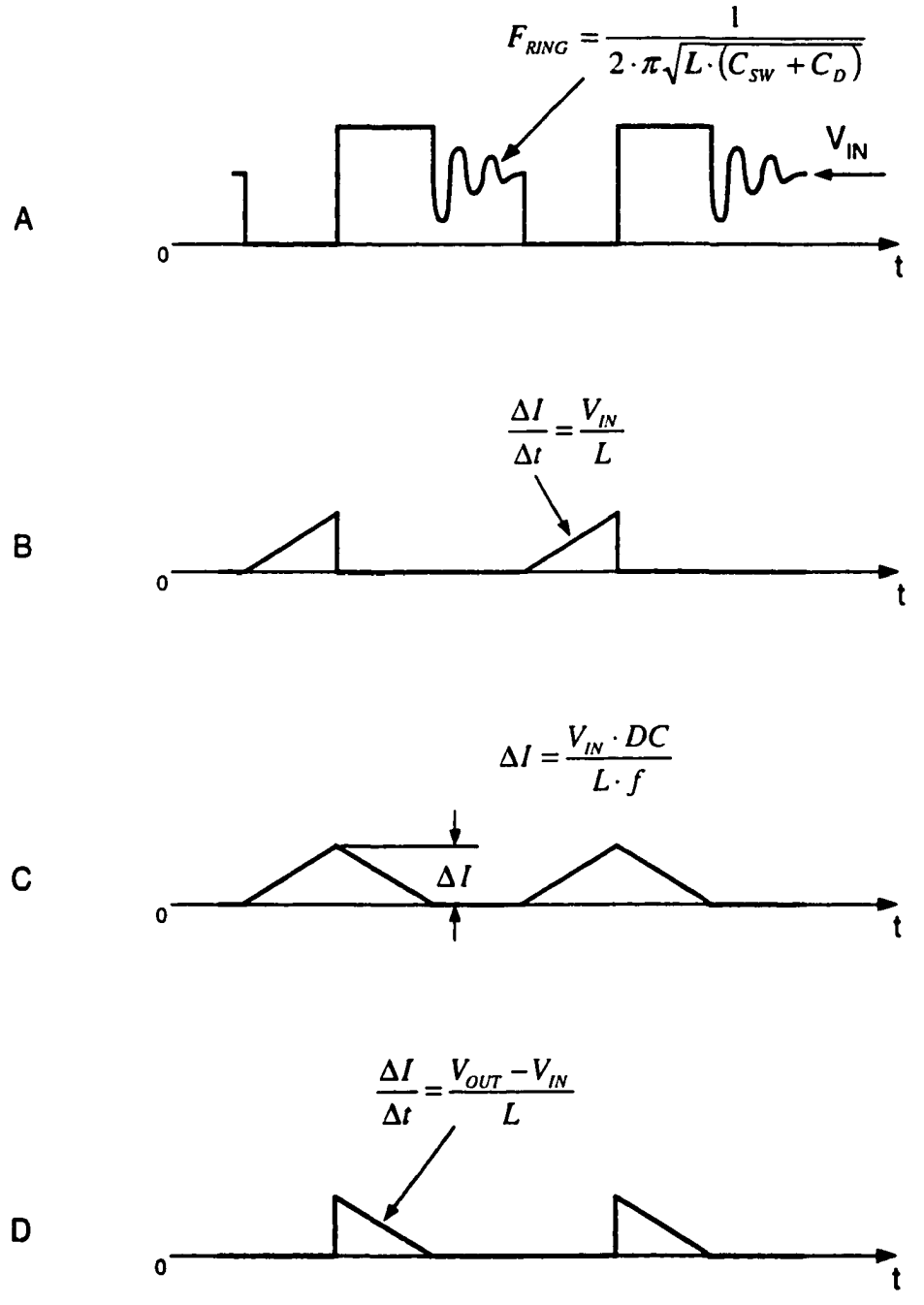

Fig. 2.14 Positive Boost Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

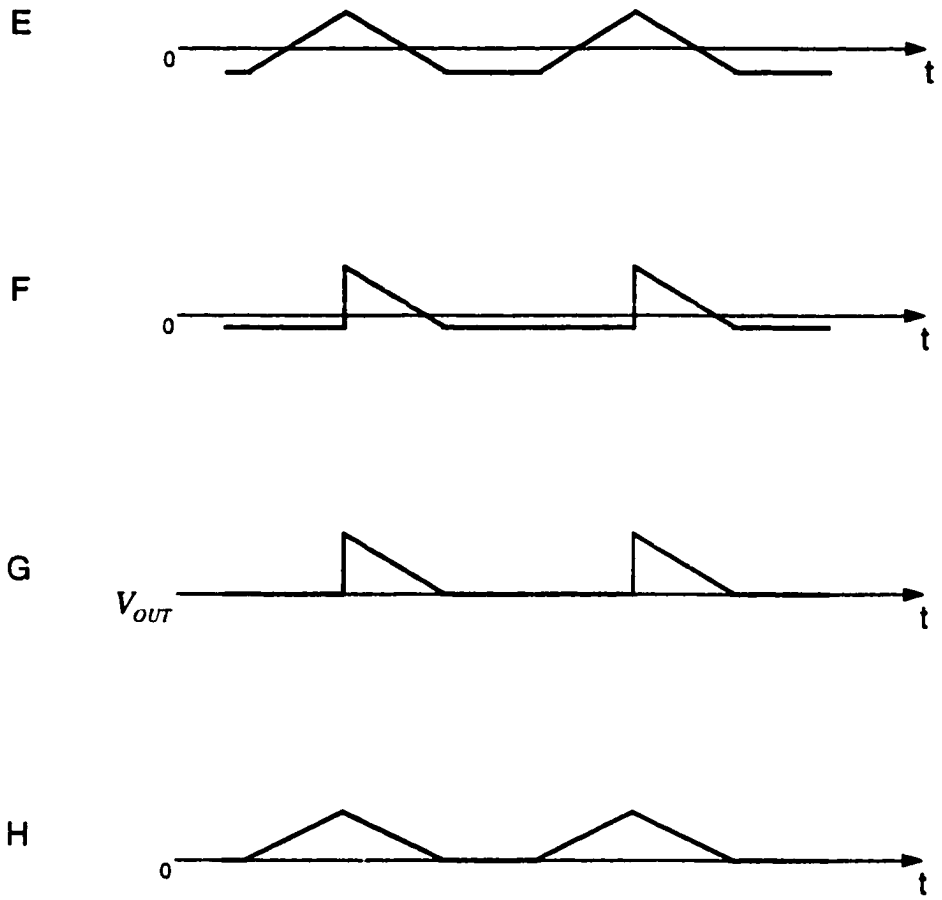

Fig. 2.14 E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

Switch Node Voltage: Fig. 2.13A, the voltage here switches between ground and one diode drop above the output voltage (V_{OUT}). This node is the major source of electric field radiation, so it should not be routed near sensitive nodes in the converter circuit. Trace widths to the switch, diode, and inductor must be wide enough to handle the high currents, but the areas should be minimized to avoid excess coupling or radiation.

Switch Current: Fig. 2.13B, the switch current steps from zero to an average value equal to output current divided by one minus duty cycle. The switch current can be many times higher than the output current when the output voltage is much higher than the input voltage. The slew rate is very high, so connections between the switch and other adjacent circuit elements must be short to prevent unwanted voltage spikes and parasitic resonances.

Inductor Current: Fig. 2.13C, the average inductor current is equal to load current divided by one minus the duty cycle, so it can be much higher than the output current.. Peak-to-peak ripple current is determined mostly by inductance value and switching frequency, but it also changes with input voltage. Smaller inductance values result in higher ripple currents and increase core losses and output ripple voltage. Larger inductance values reduce these effects, but usually result in a physically larger coil.

Diode Current: Fig. 2.13D, the diode current switches from zero to an average value approximately equal to load current divided by one minus the duty cycle. The peak diode current can be many times higher than the output current when the output voltage is higher than the input voltage. The average diode current will be equal to the output current.

Input Capacitor Ripple Current: Fig. 2.13E, The input capacitor absorbs inductor ripple current. The RMS ripple current value is approximately 0.3 times the peak-to-peak value (ΔI).

Output Capacitor Ripple Current: Fig. 2.13F, the output capacitor's peak-to-peak value is equal to peak switch current. The RMS ripple current is equal to the output current when the output voltage is twice the input voltage and increases as the input voltage is reduced.

Output Ripple Voltage: Fig. 2.13G, the output ripple voltage is determined by inductor ripple current and the ESR of the output capacitor. The capacitive reactance is usually considered a short at the switching frequencies, leaving the effective series resistance (ESR) is the only impedance. This simplifying assumption does not take into account the capacitor's inductance. Capacitor inductance is important because it determines the amplitude of narrow spikes that appear superimposed on the calculated ripple voltage. These spikes are the result of the fast edges on the current pulses delivered to the output capacitor through the diode. A current slew rate of 10^8/sec will create 1V spikes 10ns-100ns wide for a capacitor inductance of 0.01μH. These spikes are normally eliminated at the load by parasitic inductance in the lines and by the load bypass capacitors. The effect can be greatly enhanced by inserting a small ferrite bead in the output line.

Input Current: Fig. 2.13H, because the input capacitor absorbs most of the AC ripple current created by the switching operation, input current normally appears as a moderate amount of ripple superimposed on an average DC level. L_P is the equivalent parasitic

inductance of the input lines, which aids in the filtering action. Ripple current in the input lines is one cause of EMI, so the magnitude of this current is important.

2.4.2 Negative Boost Circuit Description

Fig. 2.15 shows the negative boost converter, along with its current and voltage waveforms. The operating waveforms are identical to those of Fig. 2.12, with the exception of polarity.

Fig. 2.16 shows the current and voltage waveforms of a continuous mode negative buck converter. Fig. 2.17 shows the discontinuous mode waveforms.

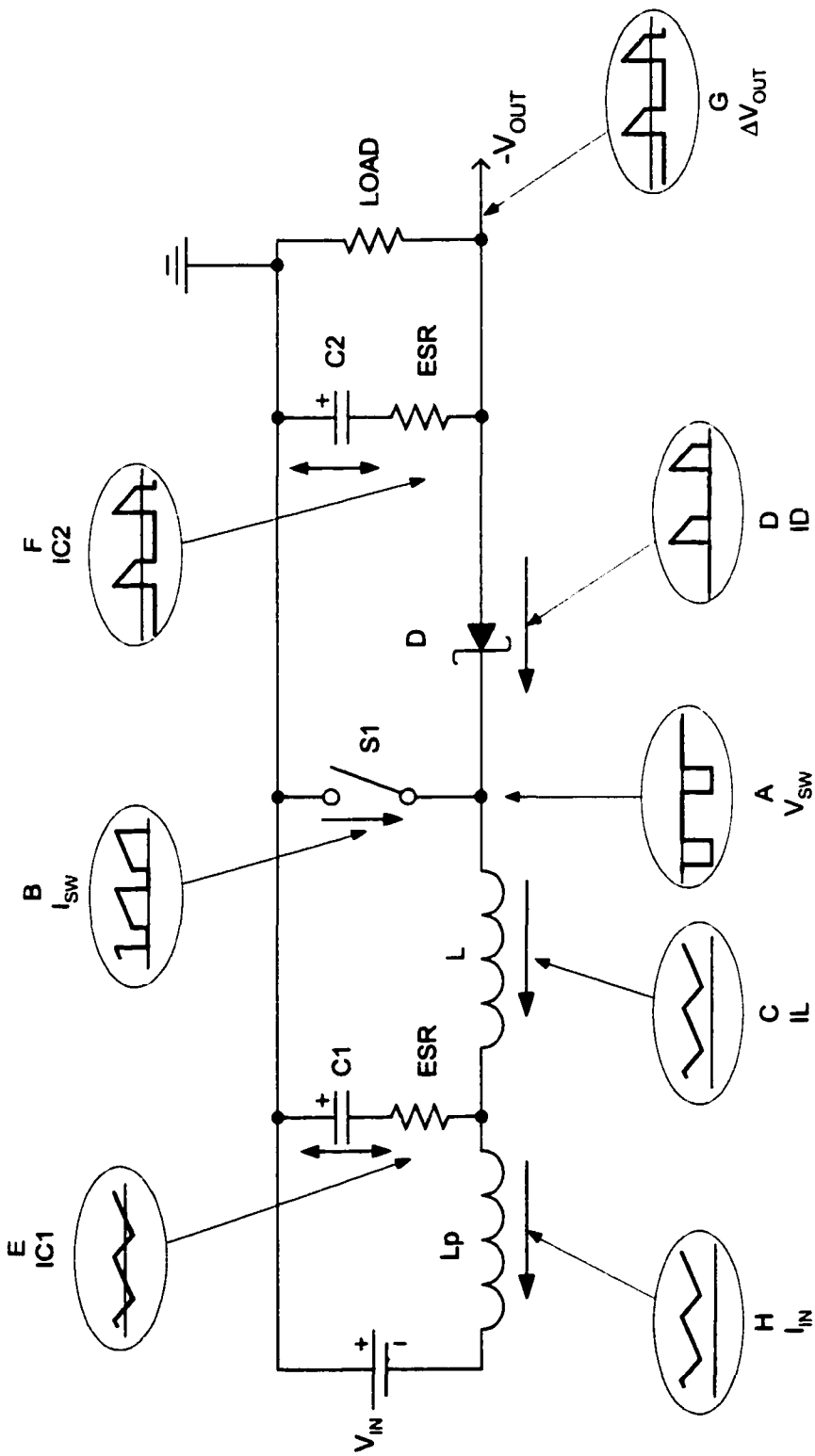

Fig. 2.15 Negative Boost Converter with its Current and Voltage Waveforms

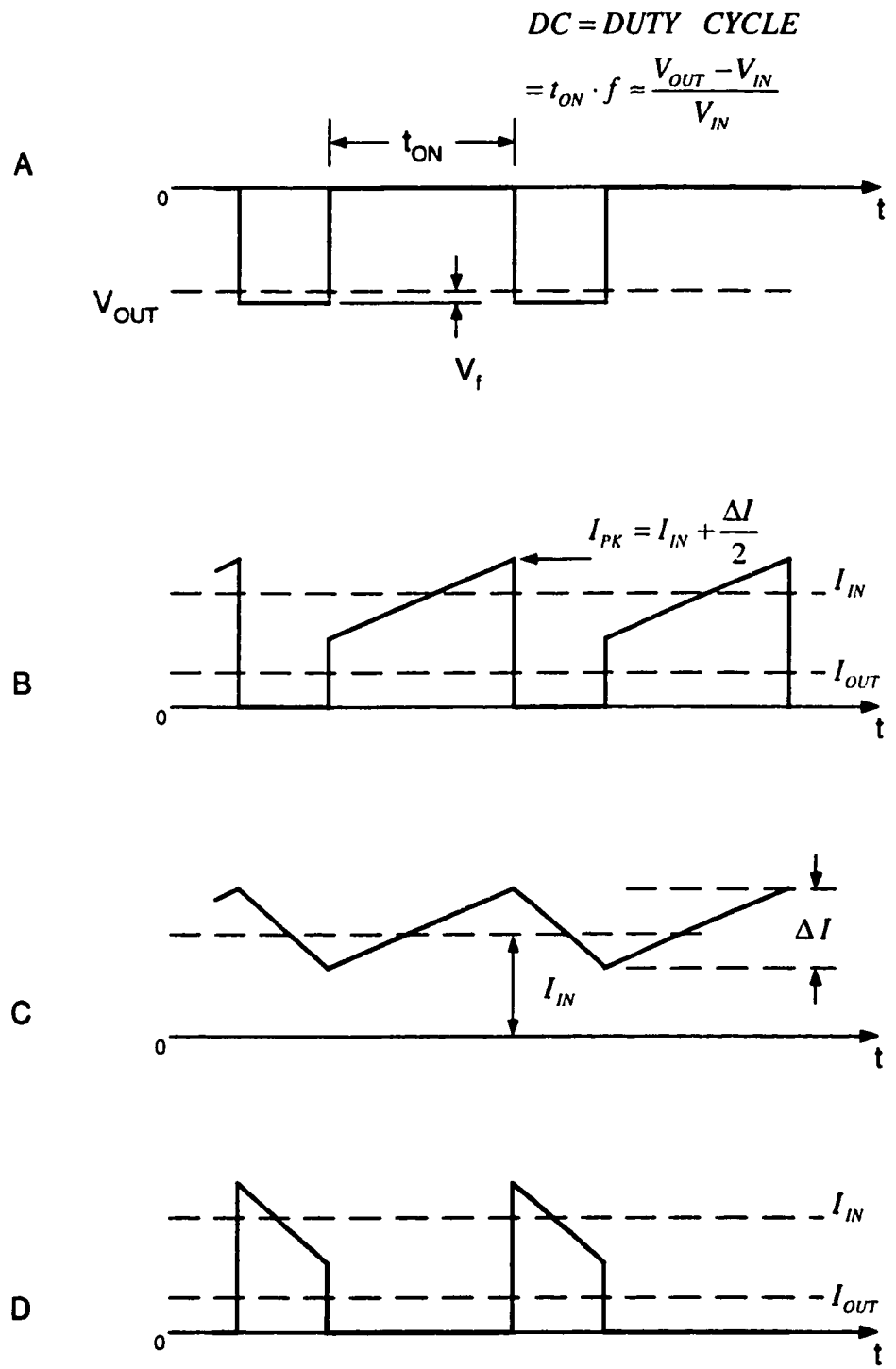

Fig. 2.16 Negative Boost Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

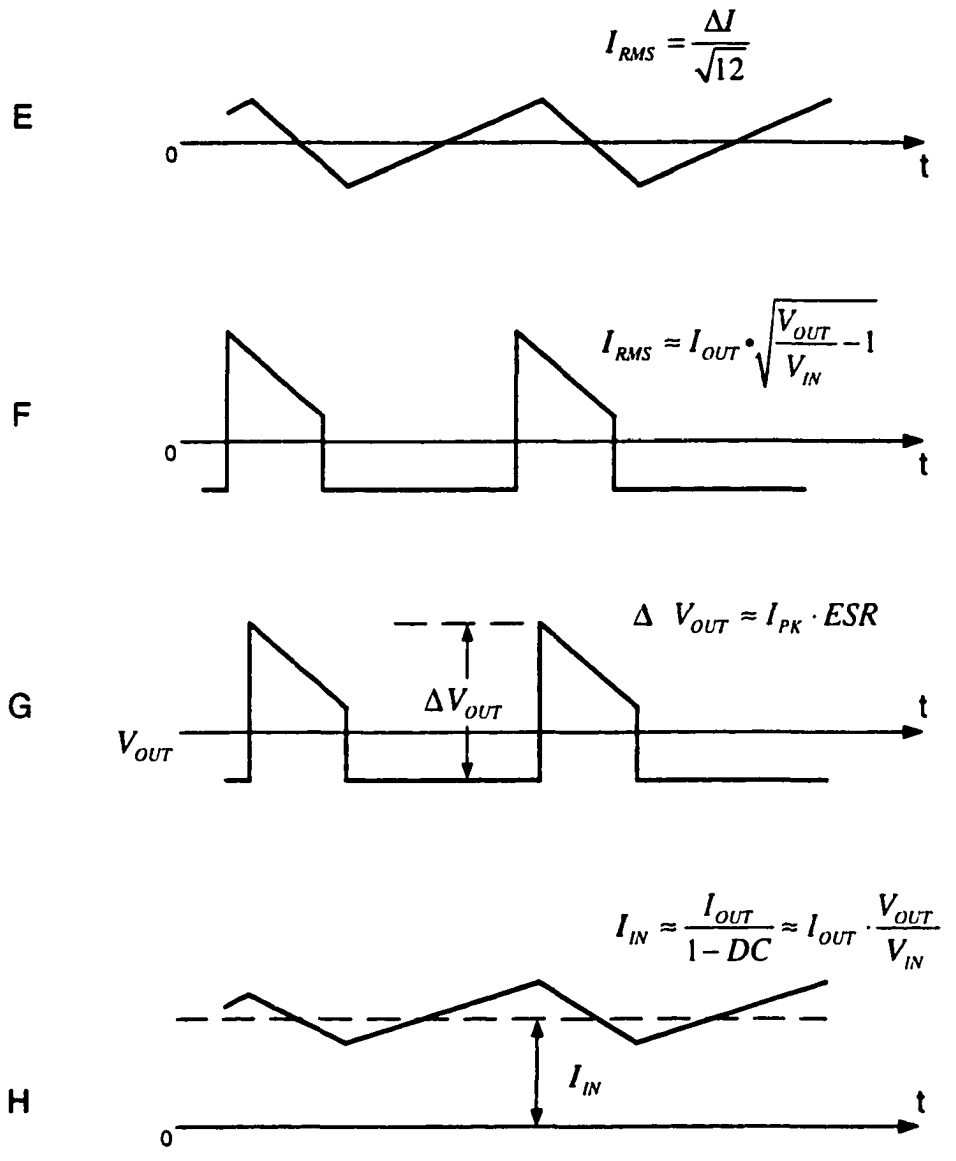

Fig. 2.16 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

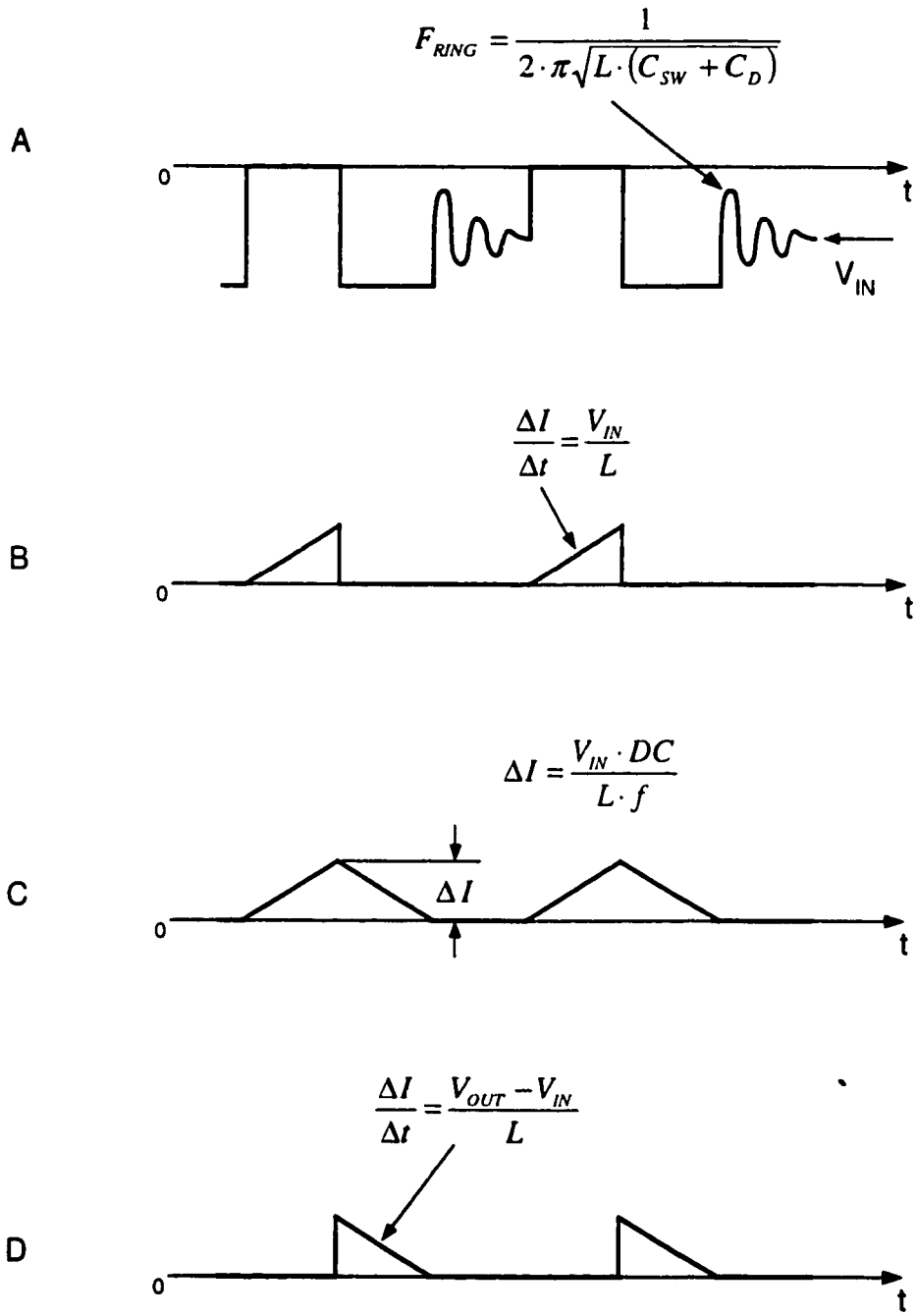

Fig. 2.17 Negative Boost Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

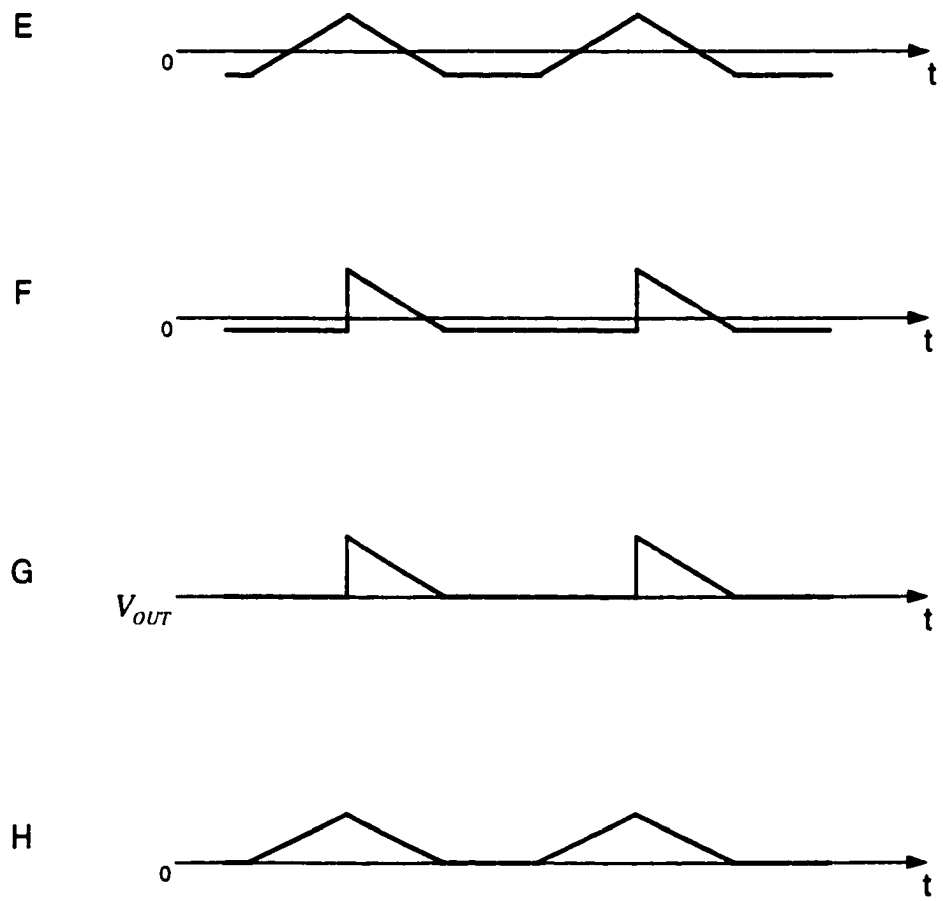

Fig. 2.17 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

2.5 Buck-Boost Converters

Buck-Boost circuits are used to generate an output with a polarity opposite to that of the input. The output voltage can be either higher or lower in magnitude than the input voltage. There are two buck-boost converter architectures, positive to negative buck-boost(Fig. 2.18), and negative to positive buck-boost (Fig. 2.19). These circuits are popular because they provide voltage inversion without the use of a transformer. They

are similar to boost converters, except one side of the inductor is tied to ground instead of the input voltage.

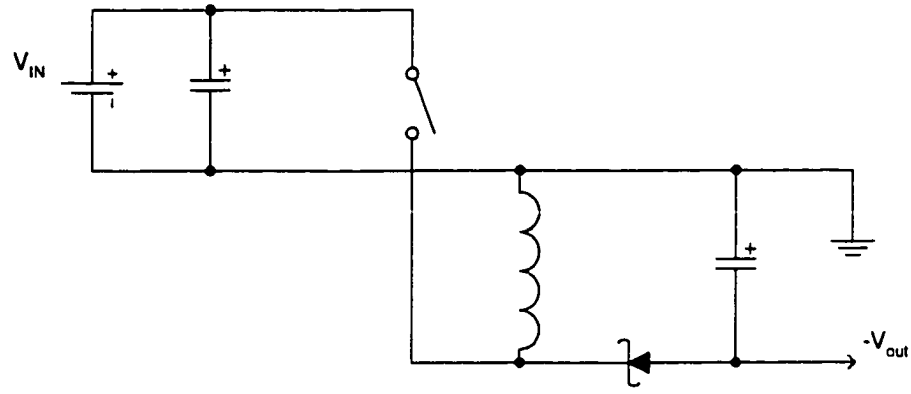

Fig. 2.18 Positive to Negative Buck-Boost

During the switch-on time, the input voltage is applied across the inductor, providing energy to the inductor. During this interval the diode is reverse biased. When the switch opens, the diode is forward biased and the energy stored is transferred to the output.

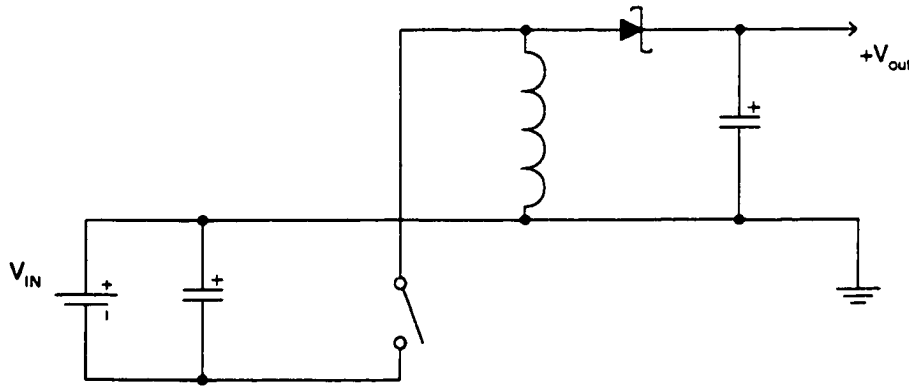

Fig. 2.19 Negative to Positive Buck-Boost

Buck-boost converters provide an output voltage that is equal to the product of the conversion factor of the Buck times the boost architecture, hence the output voltage can be lower or higher in magnitude that the input voltage. Buck-boost converters have

relatively "noisy" input and output, both of the input and output currents are chopped and have large AC components.

The biggest advantage of the buck-boost architecture is that it inverts polarity without the use of a transformer. Transformers are usually not of the shelf components and have to be custom made. Inductors are more desirable than transformers in many converter designs because they are readily available and economical, but is multiple outputs or isolation are required, a transformer must be used.

2.5.1 Positive to Negative Buck-Boost Circuit Operation

This section will describe the positive to Negative buck-boost converter in detail. All components apply to the negative to positive buck-boost converter; simply invert the polarity of the input and output voltages.

A basic positive to negative buck-boost converter, along with its current and voltage waveforms, is shown in Fig. 2.20. The circuit operation is as follows: switch S1 opens and closes at a rate dependent upon the oscillator frequency. When the switch turns on, the V_{SW} node is pulled to the input voltage. Trace A is the V_{SW} node voltage waveform, and Trace B shows the switch current waveform. While the switch is on, current flows from the input through the switch and into the inductor. During this interval there is no current being provided by the inductor to the load. The inductor current (Trace C) rises linearly during this period. The change in inductor current, or ripple (ΔI), is determined by the input voltage, inductance, and the switch-on time.

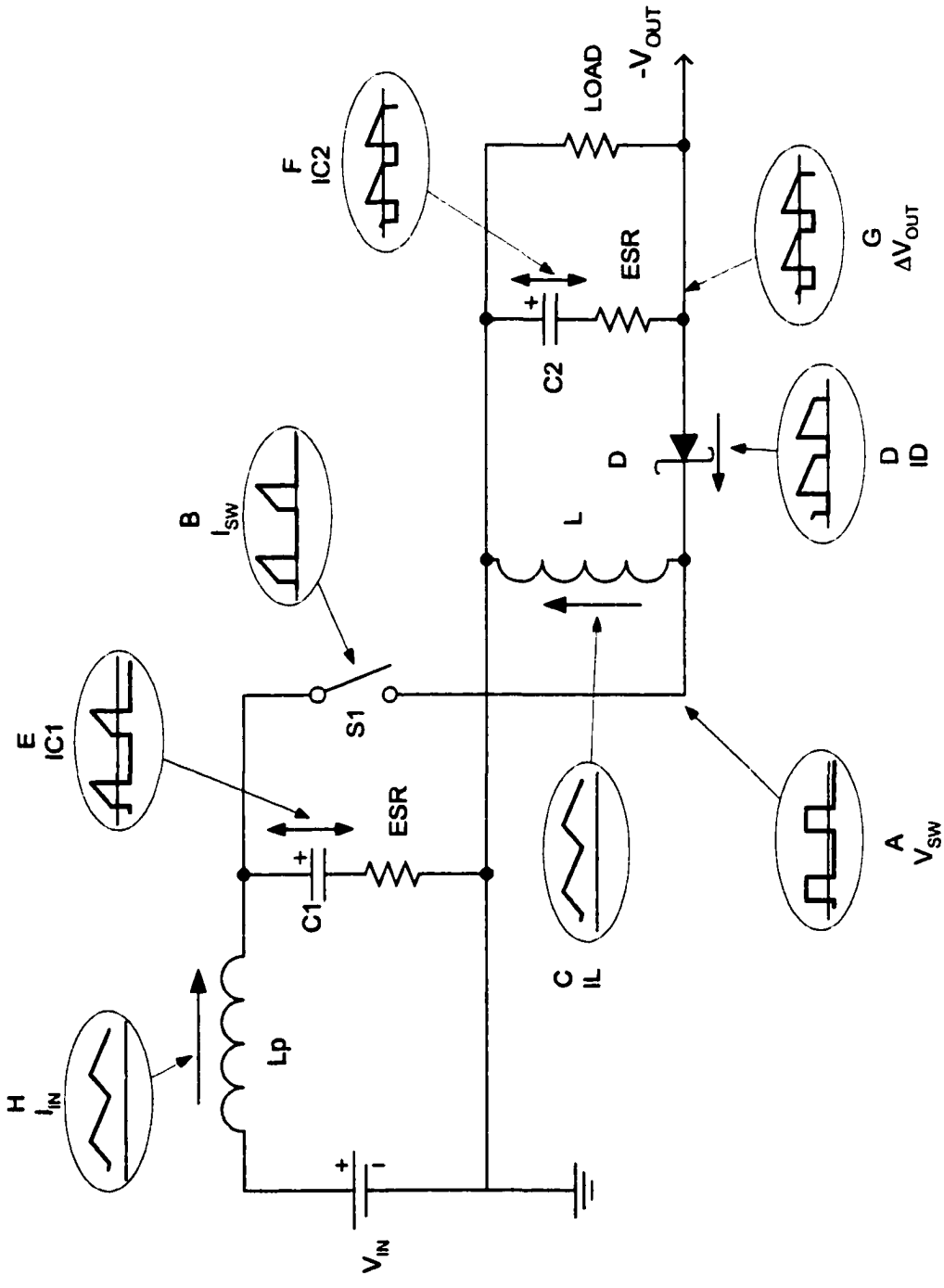

Fig. 2.20 Positive to Negative Buck-Boost Converter with its Voltage and Current Waveforms

When the switch opens, current flowing through the inductor forces the V_{SW} node voltage to drop until D1 (catch diode) becomes forward biased (Trace D), providing a path for the inductor current. The V_{SW} node is clamped to one diode drop below ground, and the inductor current begins ramping down. The slope of this ramp is a function of the inductance and the voltage across the inductor. The whole cycle repeats itself at the end of the switch off time.

The filter capacitors provide a low impedance path for the AC component of the input and diode currents. The input capacitor's current waveform (Trace E) is the same as the switch current (Trace B), except that the capacitor has no DC component. RMS ripple current in the input capacitor can vary from somewhat less than the output current to several times output current, depending on the ratio of the input to output voltage. An input filter capacitor is essential for the proper operation of the circuit. It absorbs the current pulses inherent in a buck-boost converter. Without an input filter capacitor close to the buck-boost circuit, this ripple current in conjunction with lead and printed circuit trace inductances, could cause enough ripple voltage to produce erratic operation.

The output filter capacitor current waveform (Trace F) is the same as the diode current, less the DC component. The RMS ripple current value can be less than or considerably more than DC load current, depending on the input voltage.

Current and voltage waveforms of a continuous mode basic positive to negative buck-boost converter are shown in Fig. 2.21. While Fig. 2.22 shows the waveforms of a discontinuous mode. Continuous mode operation is described next in detail. It is preferred to discontinuous mode because it maximizes the available output power for a

given converter. The difference between the two is in the characteristics of the inductor current. If the inductor current falls to zero during the switch-off time, the converter operates in the discontinuous mode, as shown in Fig. 2.22C. Continuous mode implies that the inductor is still carrying some current when the switch turns on, and the current never falls to zero. The discontinuous mode waveforms are lower in amplitude than the continuous mode waveforms because a fixed inductance value was assumed. With smaller inductance values, the discontinuous peak current will be considerably higher. Most designs "go discontinuous " when the output is lightly loaded.

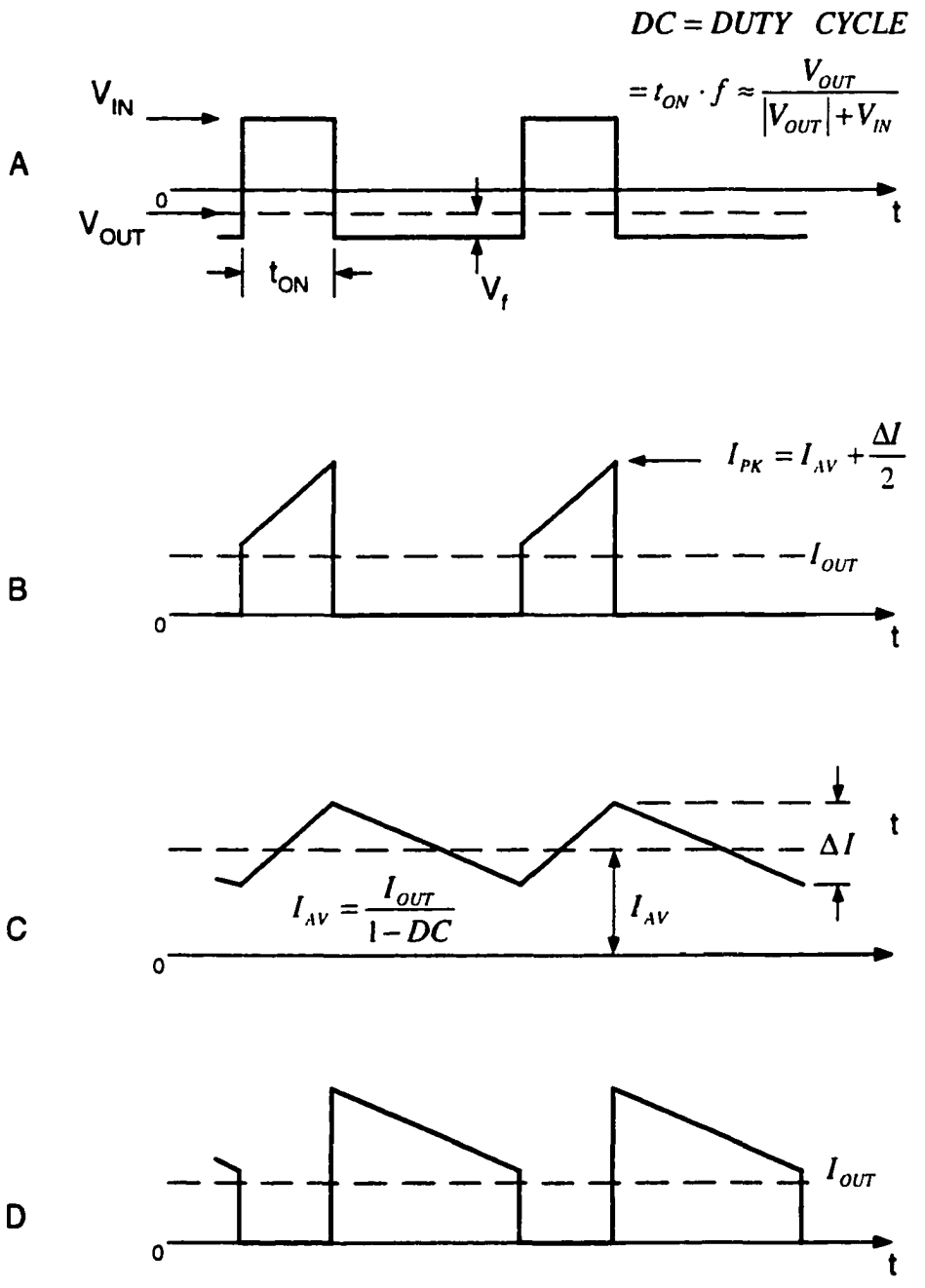

Fig. 2.21 Positive to Negative Buck-Boost Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

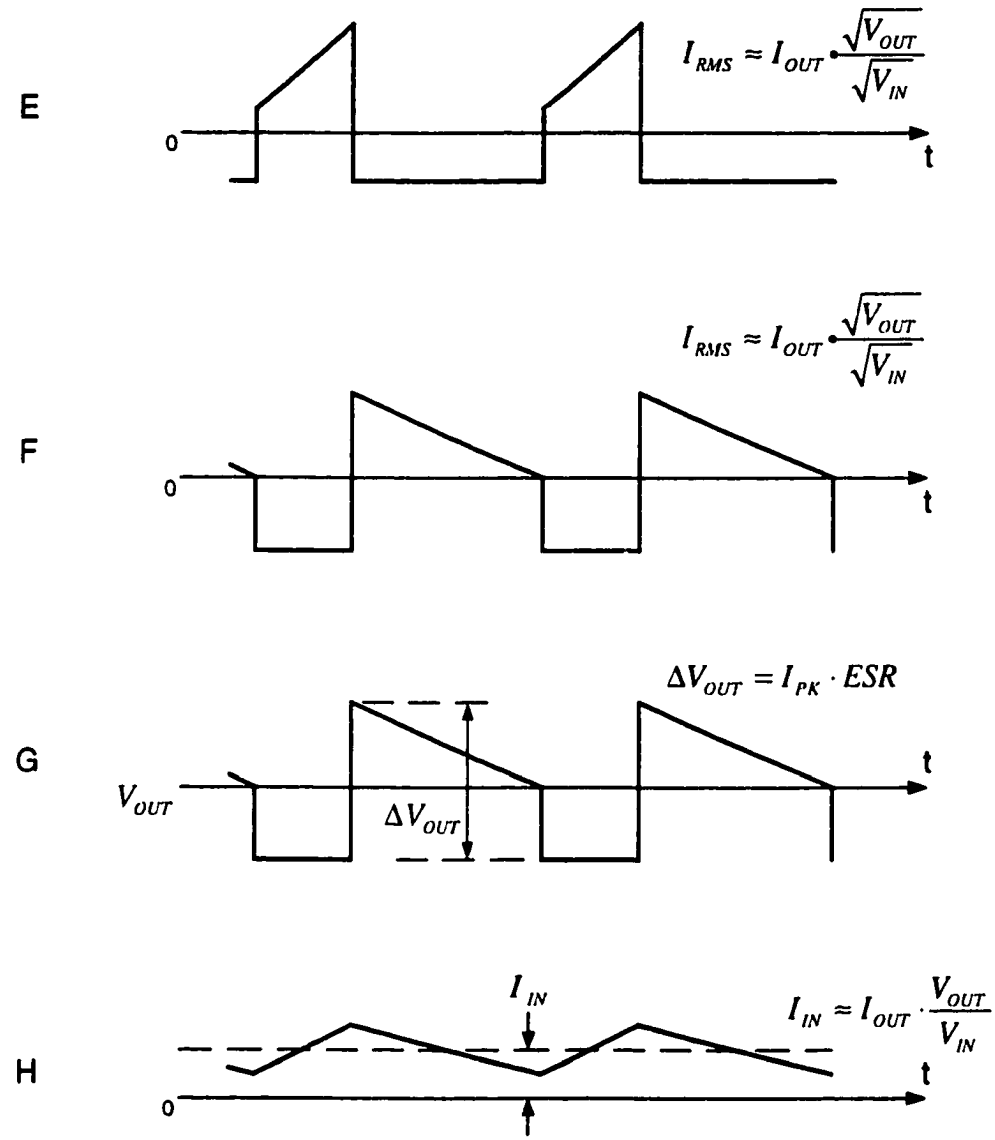

Fig. 2.21 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

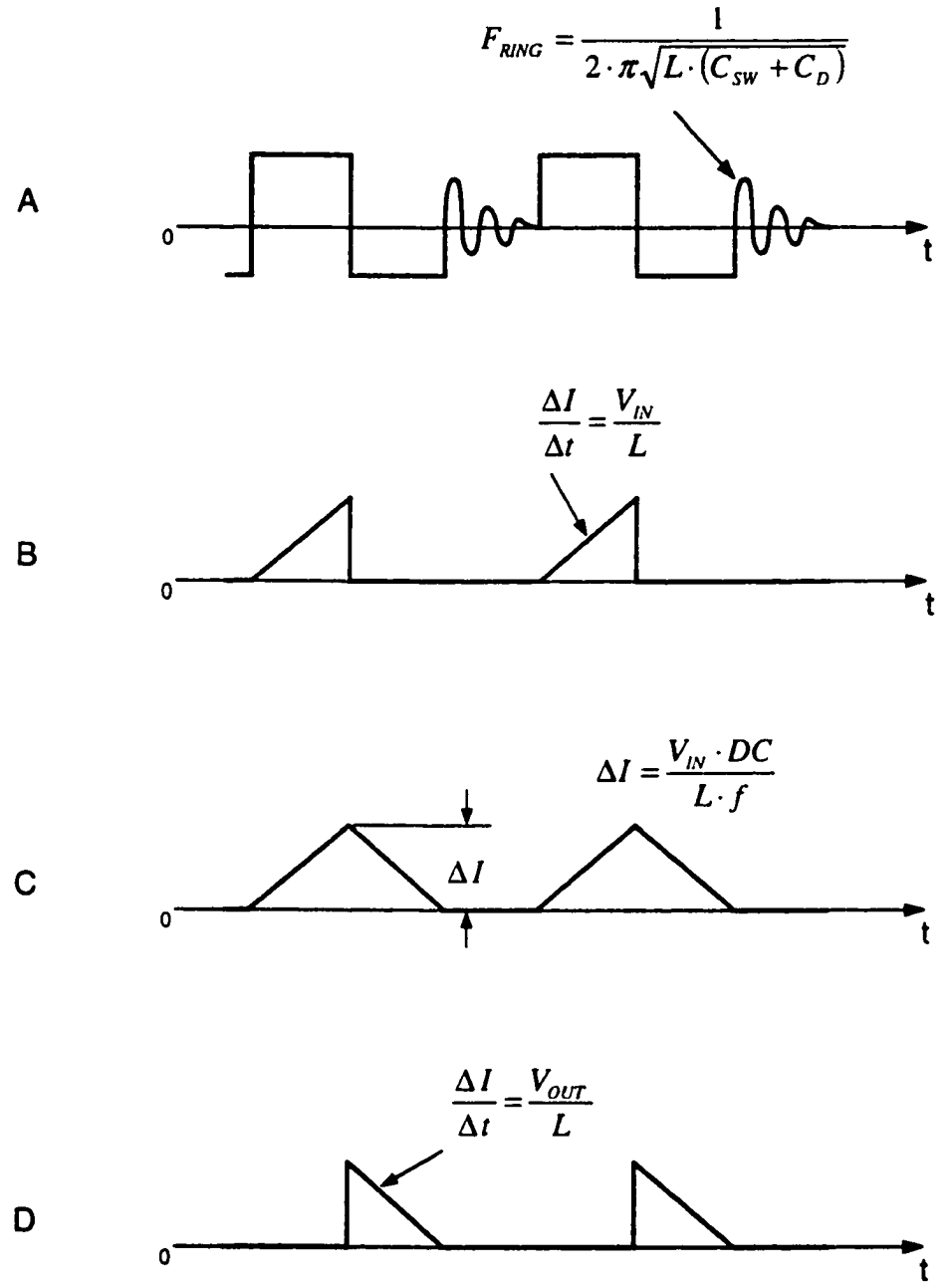

Fig. 2.22 Positive to Negative Buck-Boost Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

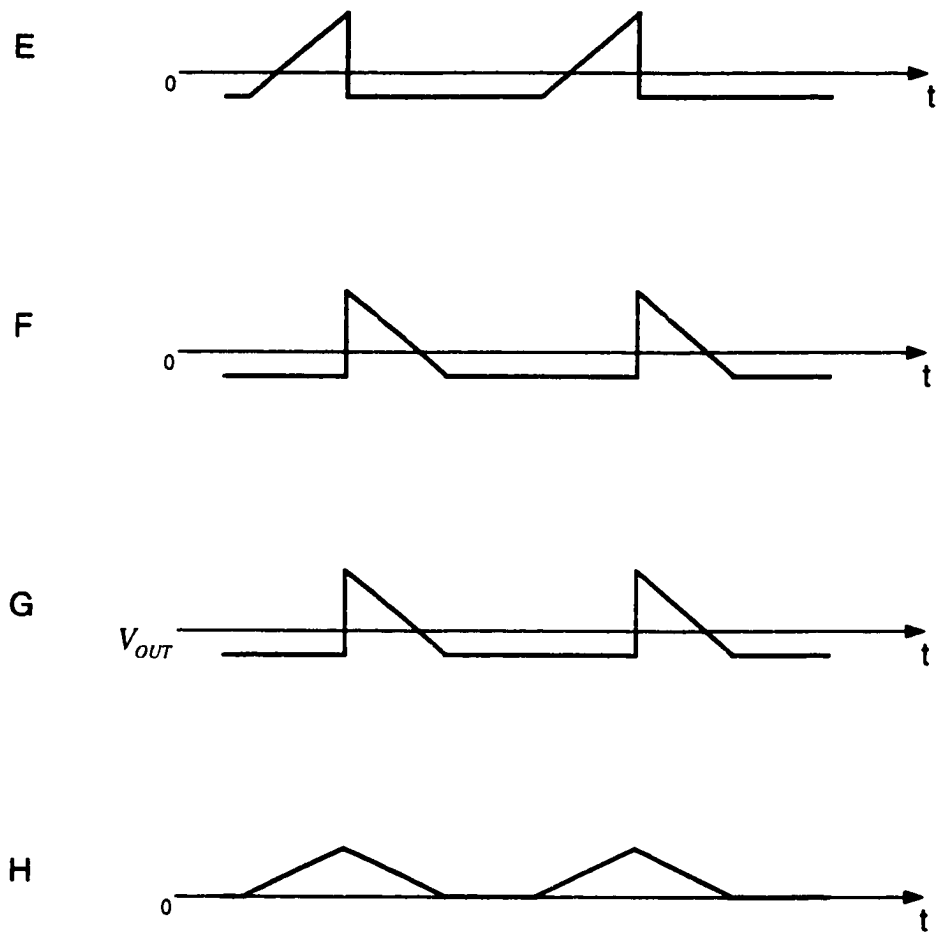

Fig. 2.22 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

The ringing shown in Fig. 2.22A is a characteristic of discontinuous mode and is not caused by loop oscillations or other circuit instabilities. Rather, the ringing is the result of a small amount of energy circulating between inductor and diode/switch parasitic capacitance. The ringing does no harm and damping it wastes energy. Because of its sinusoidal characteristics, it radiates very little energy, and hence does not cause electromagnetic interference (EMI) problems.

Switch Node Voltage: Fig. 2.21A, the voltage here switches between one diode drop below the output voltage and the input voltage (V_{IN}). This node is the major source of electric field radiation, so it should not be routed near sensitive nodes in the converter circuit. Trace widths to the switch, diode, and inductor must be wide enough to handle the high currents, but the areas should be minimized to avoid excess coupling or radiation.

Switch Current: Fig. 2.21B, the switch current steps from zero to an average value equal to load current divided by one minus duty cycle. The switch current can be many times higher than the output current when the output voltage is much higher than the input voltage. The slew rate is very high, so connections between the switch and other adjacent circuit elements must be short to prevent unwanted voltage spikes and parasitic resonances.

Inductor Current: Fig. 2.21C, the average inductor current is equal to load current divided by one minus duty cycle, so it can be much higher than the output current. Peak-to-peak ripple current is determined mostly by inductance value and switching frequency, but it also changes with input voltage. Smaller inductance values result in higher ripple

currents and increase core losses and output ripple voltage. Larger inductance values reduce these effects, but usually result in a physically larger coil.

Diode Current: Fig. 2.21D, the diode current steps from zero to an average value approximately equal to load current divided by one minus duty cycle. The peak current can be many times higher than the output current when the output voltage is much higher than the input voltage. The average diode current will be equal to the output current.

Input Capacitor Ripple Current: Fig. 2.21E, the peak-to-peak value of the input capacitor ripple current is approximately equal to the peak switch current. The RMS ripple current is equal to the output current when the output voltage equals the input voltage and it increases as the input voltage is reduced.

Output Capacitor Ripple Current: Fig. 2.21F, the peak-to-peak value of output capacitor ripple current is equal to the peak switch current: the RMS ripple current is equal to the output current when the output voltage equals the input voltage and it increases as the input voltage is reduced.

Output Ripple Voltage: Fig. 2.21G, the output ripple voltage is determined by the output current and the ESR of the output capacitor. The capacitive reactance is usually considered a short at the switching frequencies, leaving the effective series resistance (ESR) is the only impedance.

Input Current: Fig. 2.21H, input current normally appears as a moderate amount of ripple superimposed on an average DC level, because the input capacitor absorbs most of the AC ripple current created by the switching operation. L_P is the equivalent parasitic

inductance of the input lines, which aids in the filtering action. Ripple current in the input lines is one cause of EMI, so the magnitude of this current is important.

2.5.2 Negative to Positive Buck-boost Circuit Description

Fig. 2.23 shows the negative to positive buck-boost converter, along with its current and voltage waveforms. The operating waveforms are identical to those of Fig. 2.20, with the exception of polarity.

Fig. 2.24 shows the current and voltage waveforms of a continuous mode negative to positive buck-boost converter. Fig. 2.25 shows the discontinuous mode waveforms.

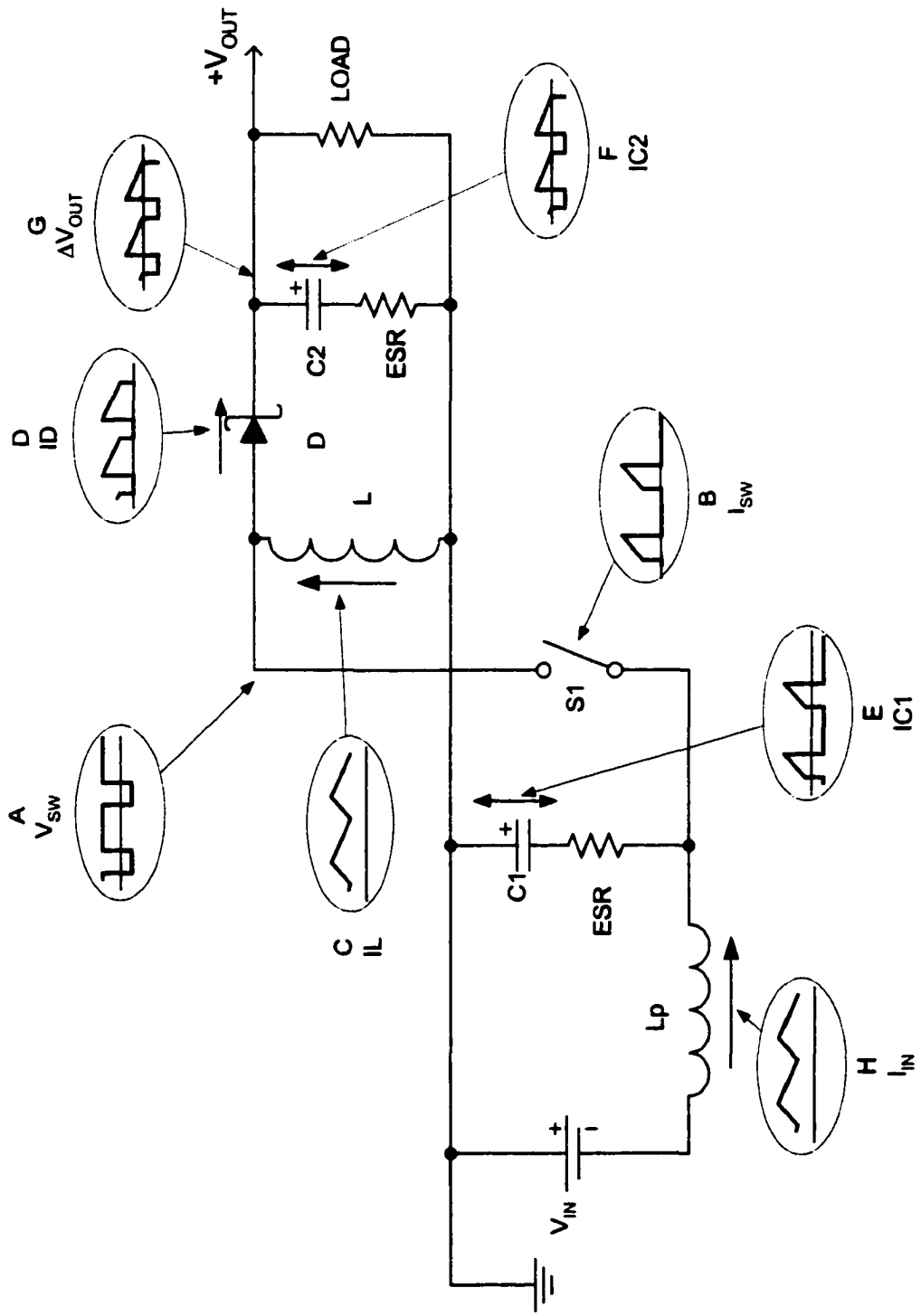

Fig. 2.23 Negative to Positive Buck-Boost Converter with its Current and Voltage Waveforms

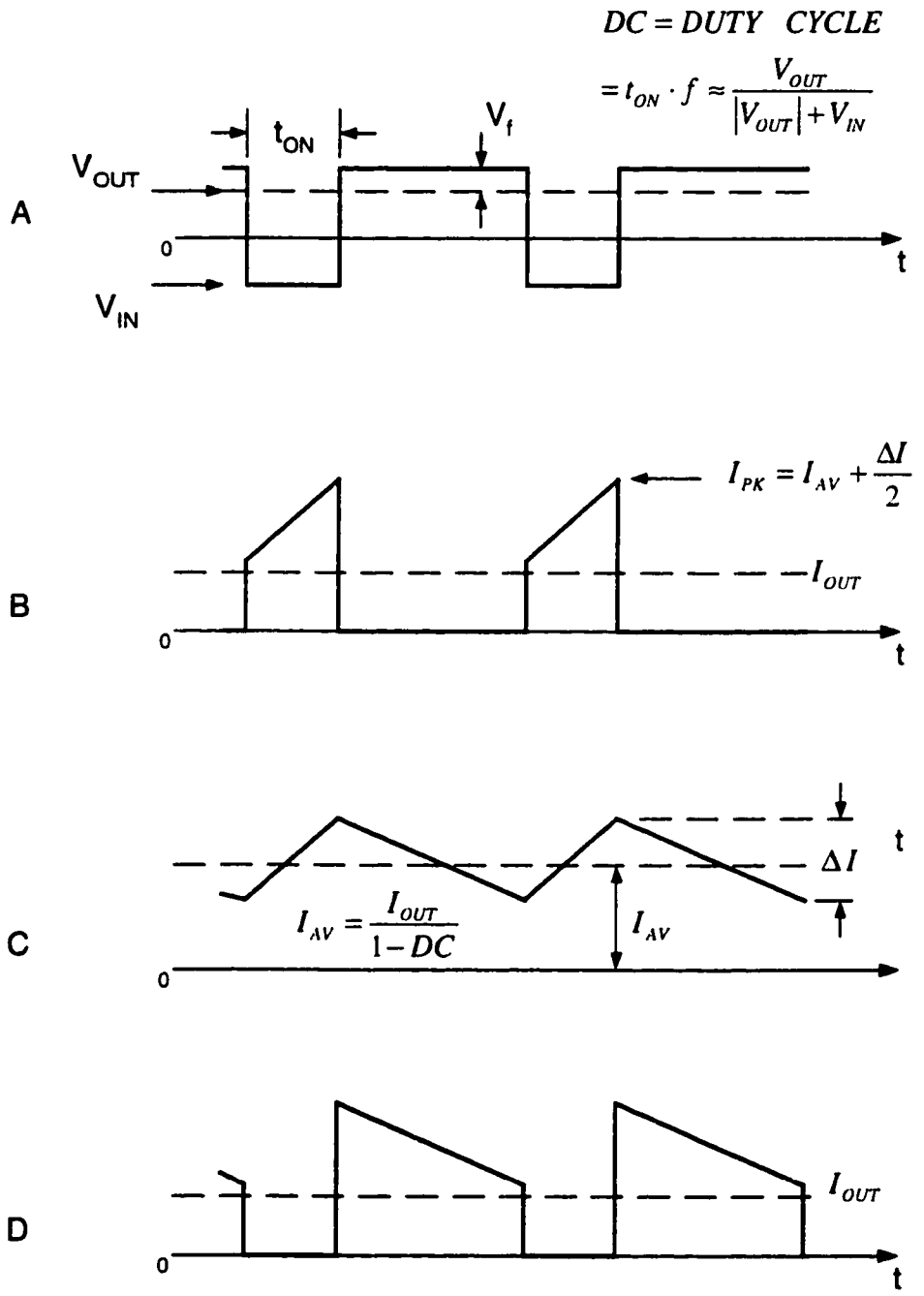

Fig. 2.24 Negative to Positive Buck-Boost Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

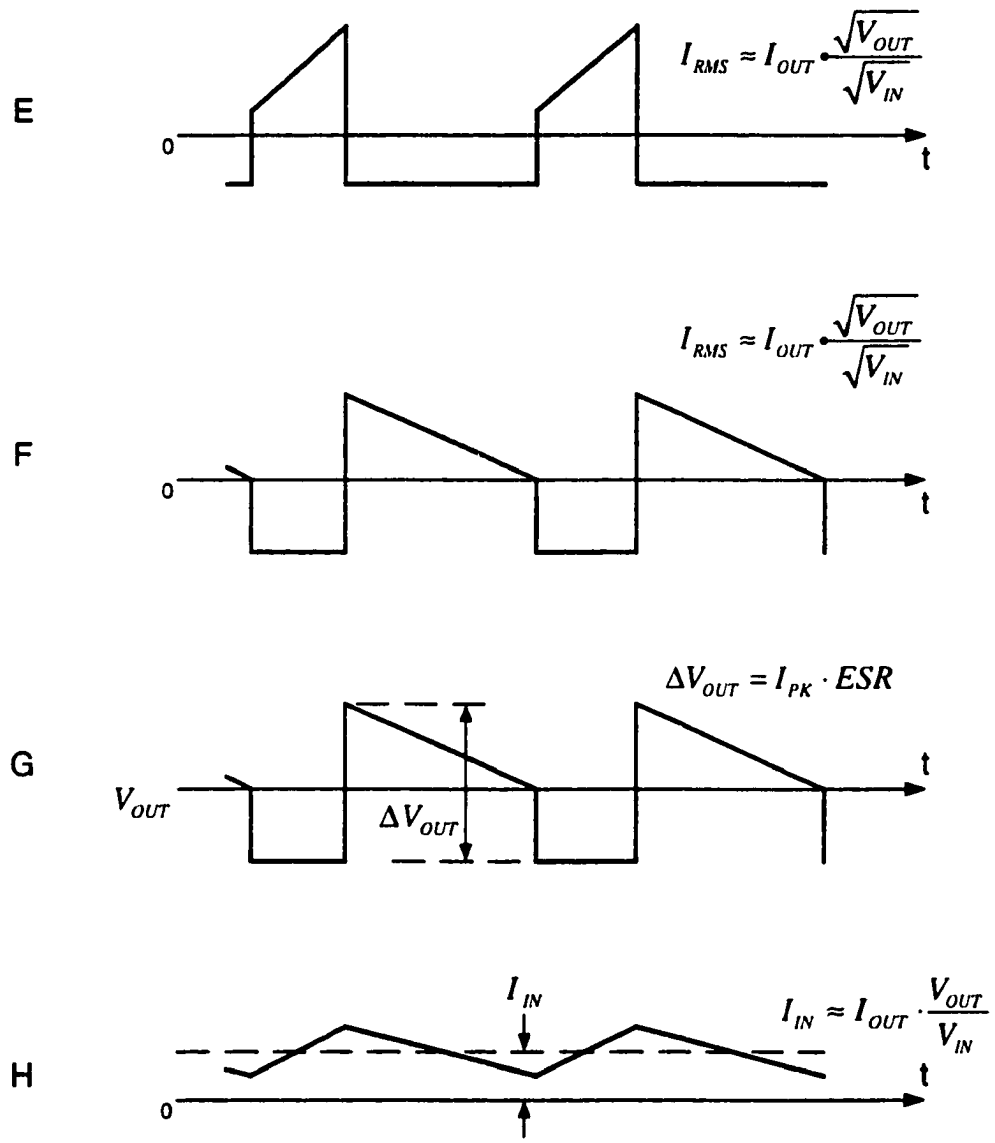

Fig. 2.24 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

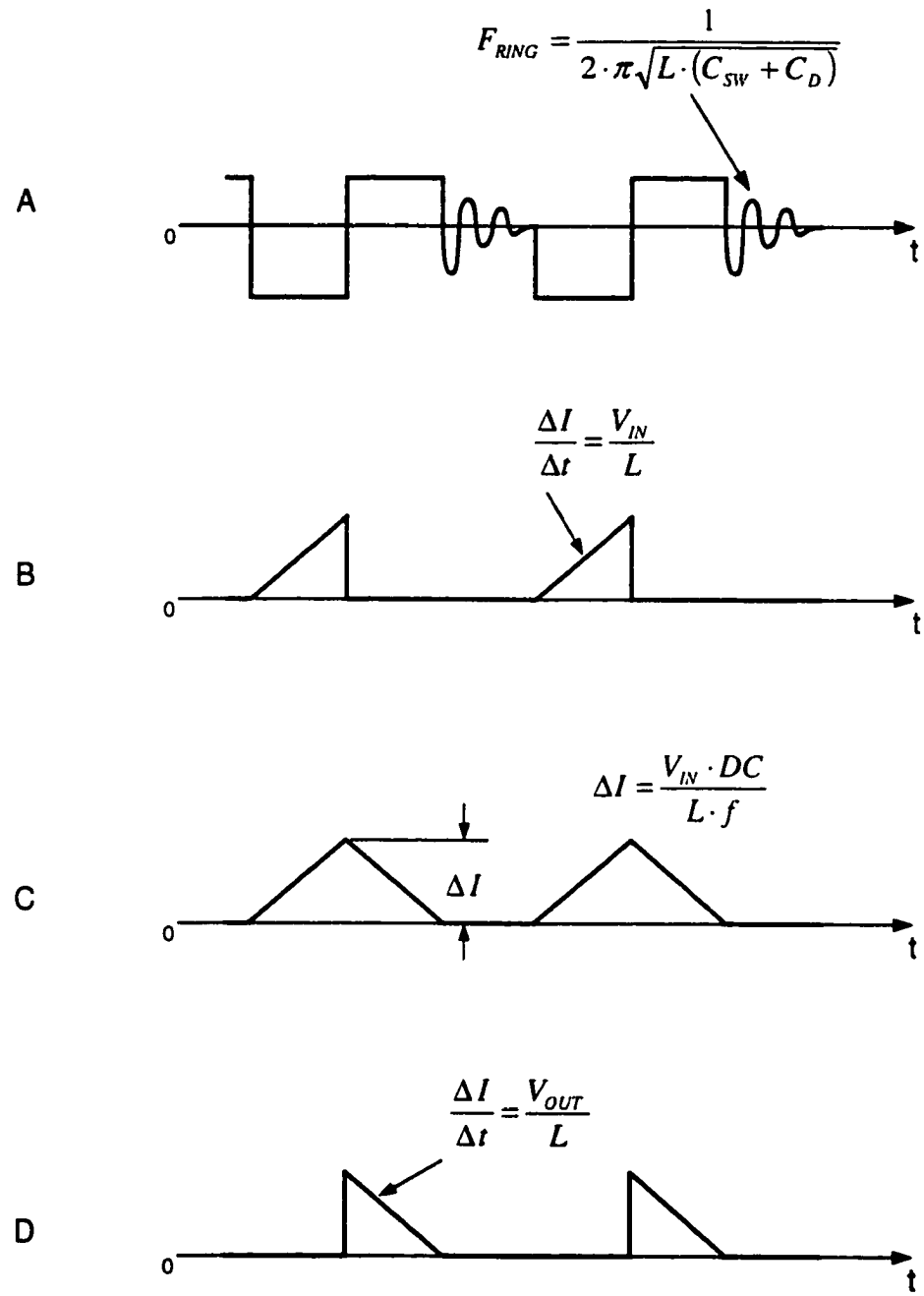

Fig. 2.25 Negative Buck-Boost Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) IL, inductor current. D) ID, diode current.

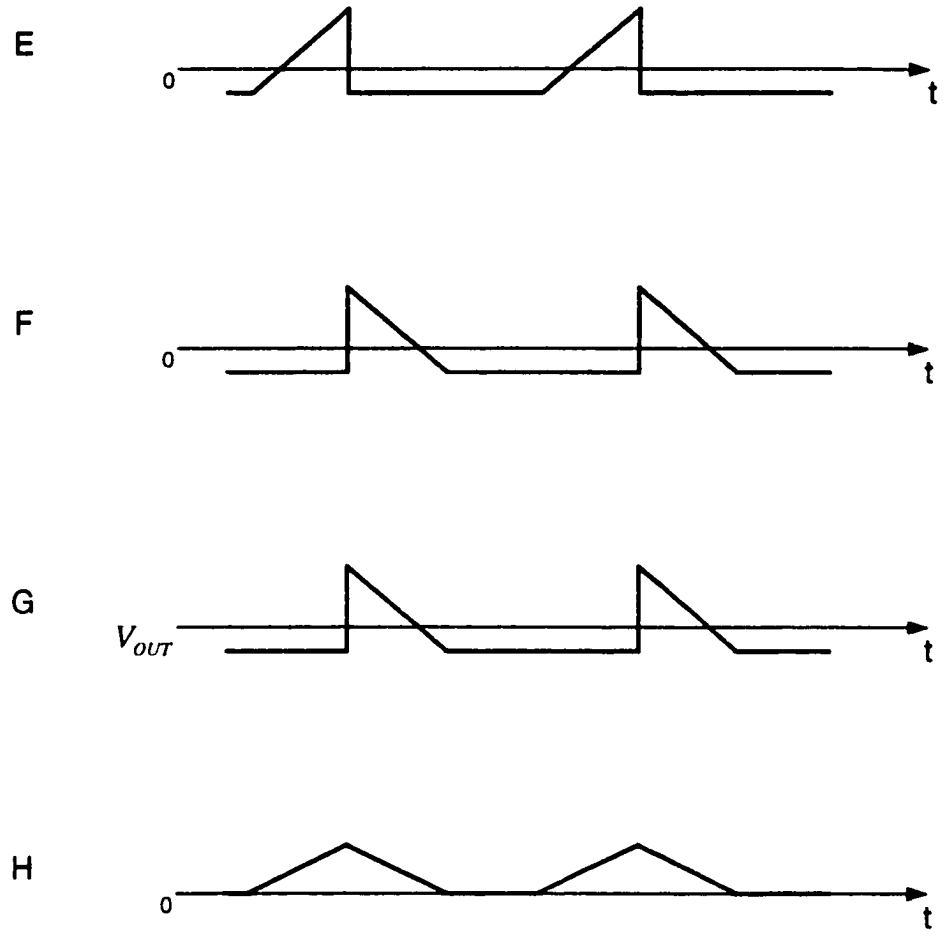

Fig. 2.25 Cont'd. E) IC1, input capacitor current. F) IC2, output capacitor current. G) ΔV_{OUT}, output ripple voltage. H) I_{IN}, input ripple current with filter.

2.6 Flyback Converters

Flyback converters can have multiple outputs, which can be higher or lower than the input voltage and of either the same or the opposite polarity as the input voltage. Flyback converters (Fig. 2.26) require a transformer, which is generally not an off-the-shelf component, transformers are bulky and are not favorable in the design of portable equipment.

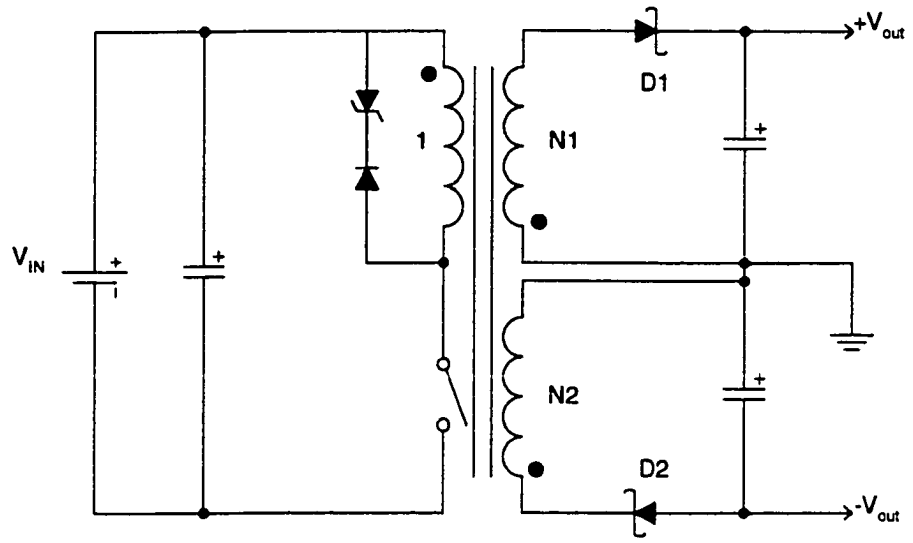

Fig. 2.26 Flyback converter

Flyback converters use a transformer to transfer energy from the input to the output. During the switch-on time, energy builds up in the transformer's core because of increasing current in the primary winding. At this time the polarity of the output winding is such that D1 and D2 are reverse biased. When the switch opens, the stored energy is transferred to the secondary winding and current is delivered to the load. The turns ratio of the transformer can be adjusted for "optimum" power transfer from input to output, taking peak switch current and peak switch voltage limitations into account.

Flyback converters have relatively "noisy" input and outputs and both of the input and output currents have large AC components in them.

2.6.1 Flyback Circuit Operation

A basic flyback converter, along with its current and voltage waveforms, is shown in Fig. 2.27. The circuit operation is as follows: switch S1 opens and closes at a rate dependent upon the oscillator frequency. When the switch turns on, the V_{SW} node is pulled to ground. Trace A is the V_{SW} node voltage waveform, and Trace B shows the switch current waveform. While the switch is on, current flows from the input through the primary and into the switch. After the initial jump, the primary current (Trace E) rises linearly during this period. The change in inductor current, or ripple (ΔI), is determined by the voltage applied across the inductor, its inductance, and the switch-on time.

During this time, energy is being stored in the transformer's core as the magnetic field builds up. The output diode(s) are reverse biased and no energy is transferred to the load during this interval.

When the switch opens, energy is no longer fed into the transformer, and as a result, the magnetic field begins to collapse. The collapsing magnetic field reverses the voltage across the transformer's windings. During this interval the switch node voltage (V_{SW}) rises to a potential above the input voltage, the secondary forward biases the rectifier diode (D1), and the transformer's energy is transferred to the output.

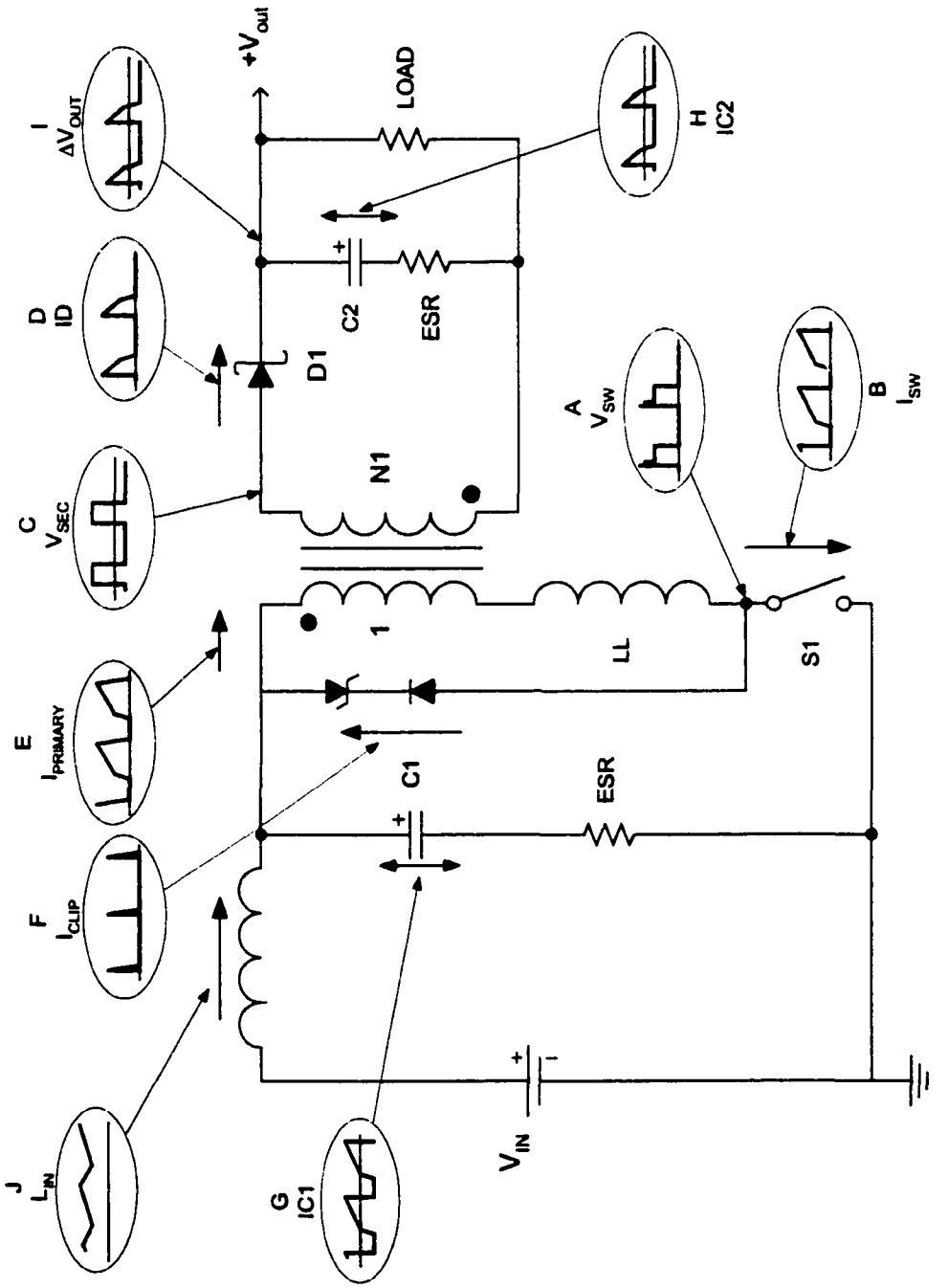

Fig. 2.27 Flyback Converter with its Voltage and Current Waveforms

The transformer is not an ideal component, so not all the energy stored in the core is transferred to the secondary winding. The energy left in the primary winding leakage inductance causes a spike on the leading edge of the switch node voltage (Trace A). The series zener/diode network clamps the V_{SW} node, providing a current path for the leakage inductance spike (Trace F). Once the leakage inductance current has fallen to zero, the V_{SW} node voltage settles to the normal flyback voltage potential, which is equal to the output voltage divided by the turns ratio (N) plus input voltage.

The filter capacitors provide a low impedance path for the AC component of the input and diode currents. The input capacitor's current waveform (Trace G) is the same as the switch current (Trace B), except that the capacitor has no DC component. The input capacitor RMS ripple current depends on the input voltage, load current, and transformer turns ratio. An input filter capacitor is essential for the proper operation of the circuit. It absorbs the current pulses inherent in a buck converter. Without an input filter capacitor close to the buck circuit, this ripple current in conjunction with lead and printed circuit trace inductances, could cause enough ripple voltage to produce erratic operation.

The output filter capacitor current waveform (Trace H) is the same as the rectifier diode current waveform (Trace D), less the DC component. Its RMS ripple current value depends on the input voltage, load current, and transformer turns ratio. In the flyback topology, the output filter capacitor can be under severe current stress at high output currents. This is because the transformer provides current to the output capacitor in pulses. The peak-to-peak output capacitor ripple current is 1/N times the primary current.

For turns ratios less than one, the output capacitor's ripple current increases significantly. For example, if N = 1/3 and the primary peak current is 1A, the secondary peak current is 3A and the output capacitor RMS ripple current would be approximately 1.5A RMS. Two or more capacitors connected in parallel can be used to handle the current.

Current and voltage waveforms of a continuous mode basic flyback converter are shown in Fig. 2.28. While Fig. 2.29 shows the waveforms of a discontinuous mode. Continuous mode operation is described next in detail. It is preferred to discontinuous mode because it maximizes the available output power for a given converter. The difference between the two is in the characteristics of the transformer's current. If the transformer's current falls to zero during the switch-off time, the converter operates in the discontinuous mode, as shown in Trace D. Continuous mode implies that the secondary winding is still carrying some current when the switch turns on, and the current never falls to zero. The discontinuous mode waveforms are lower in amplitude than the continuous mode waveforms because a fixed primary inductance value was assumed. With smaller primary inductance values, the discontinuous peak current will be considerably higher. Most designs "go discontinuous " when the output is lightly loaded.

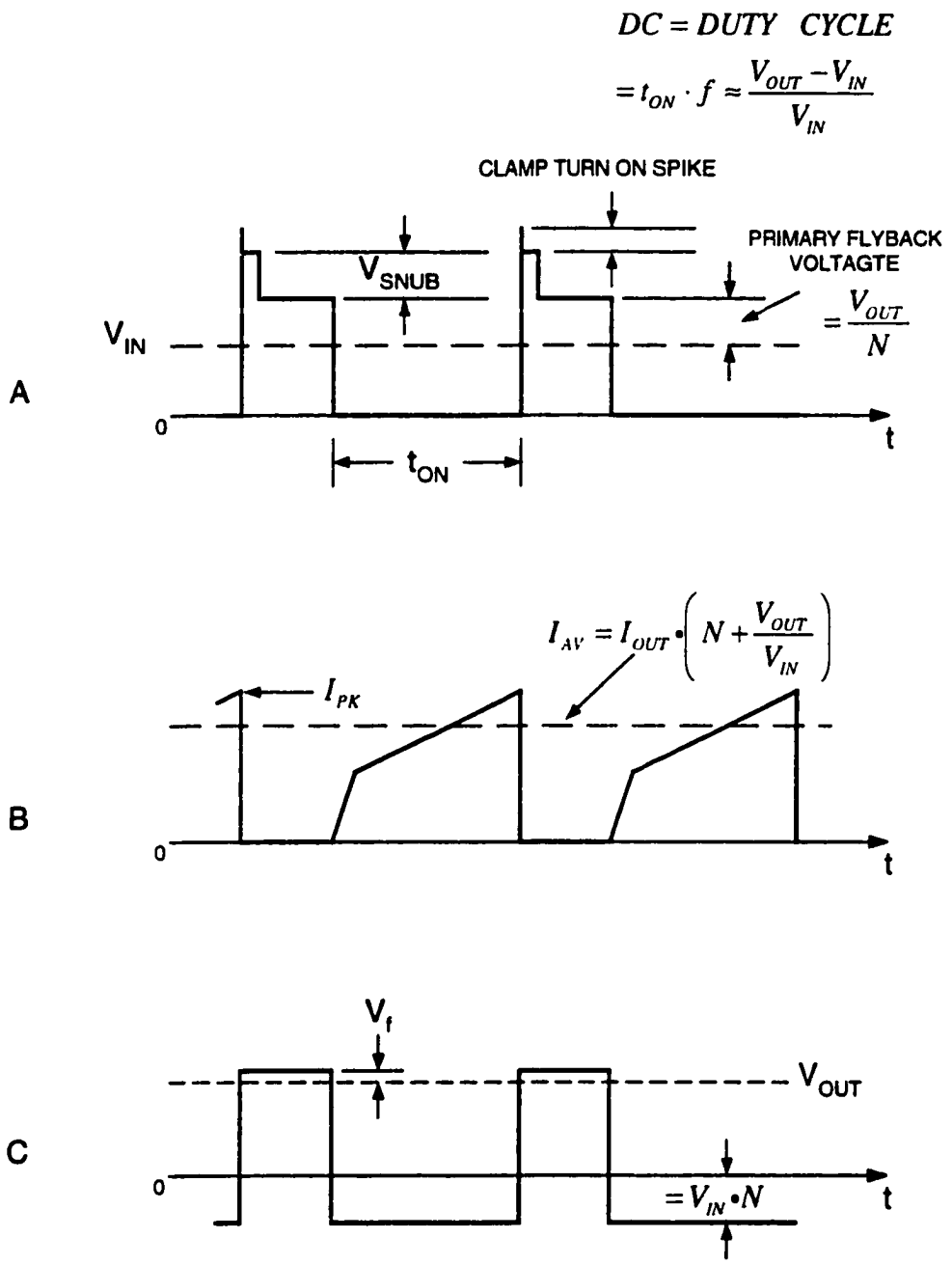

Fig. 2.28 Flyback Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) V_{SEC}, secondary voltage.

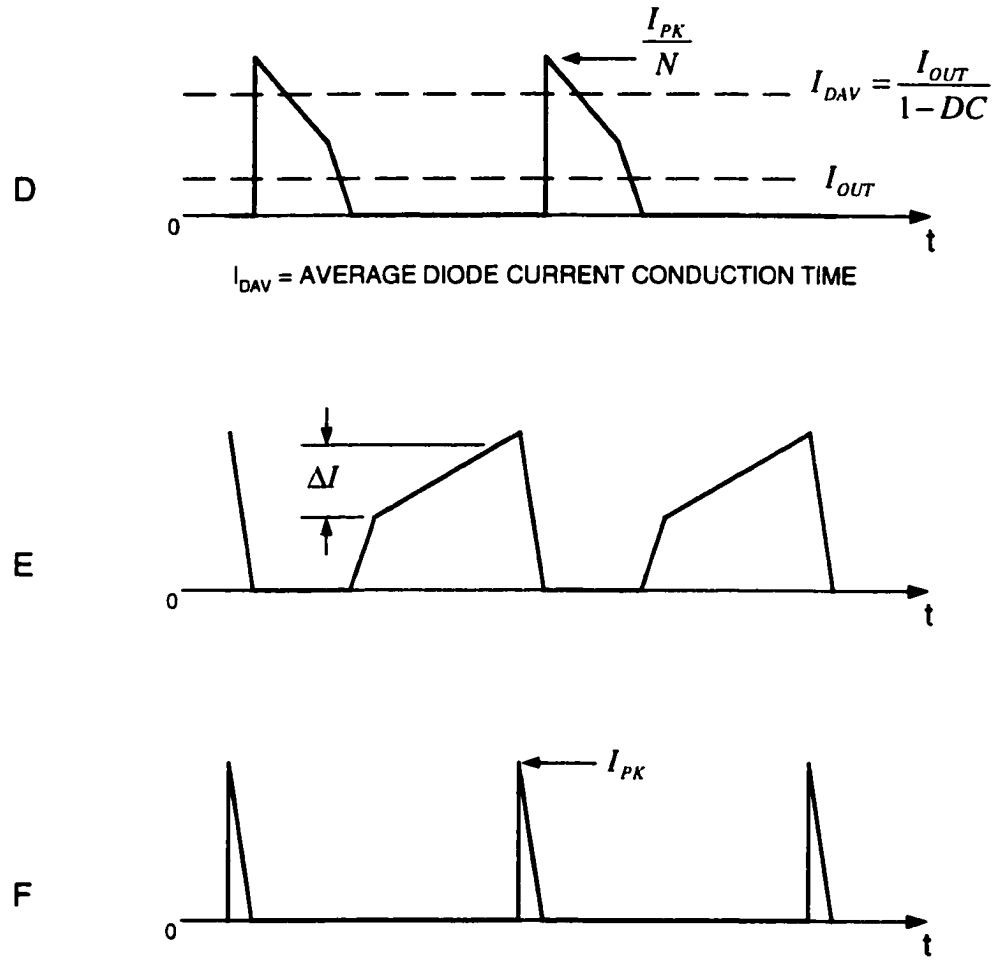

Fig. 2.28 Cont'd. D) $I_{SECONDARY}$, output diode and secondary current. E) $I_{PRIMARY}$, primary current. F) I_{CLIP}, clipper current.

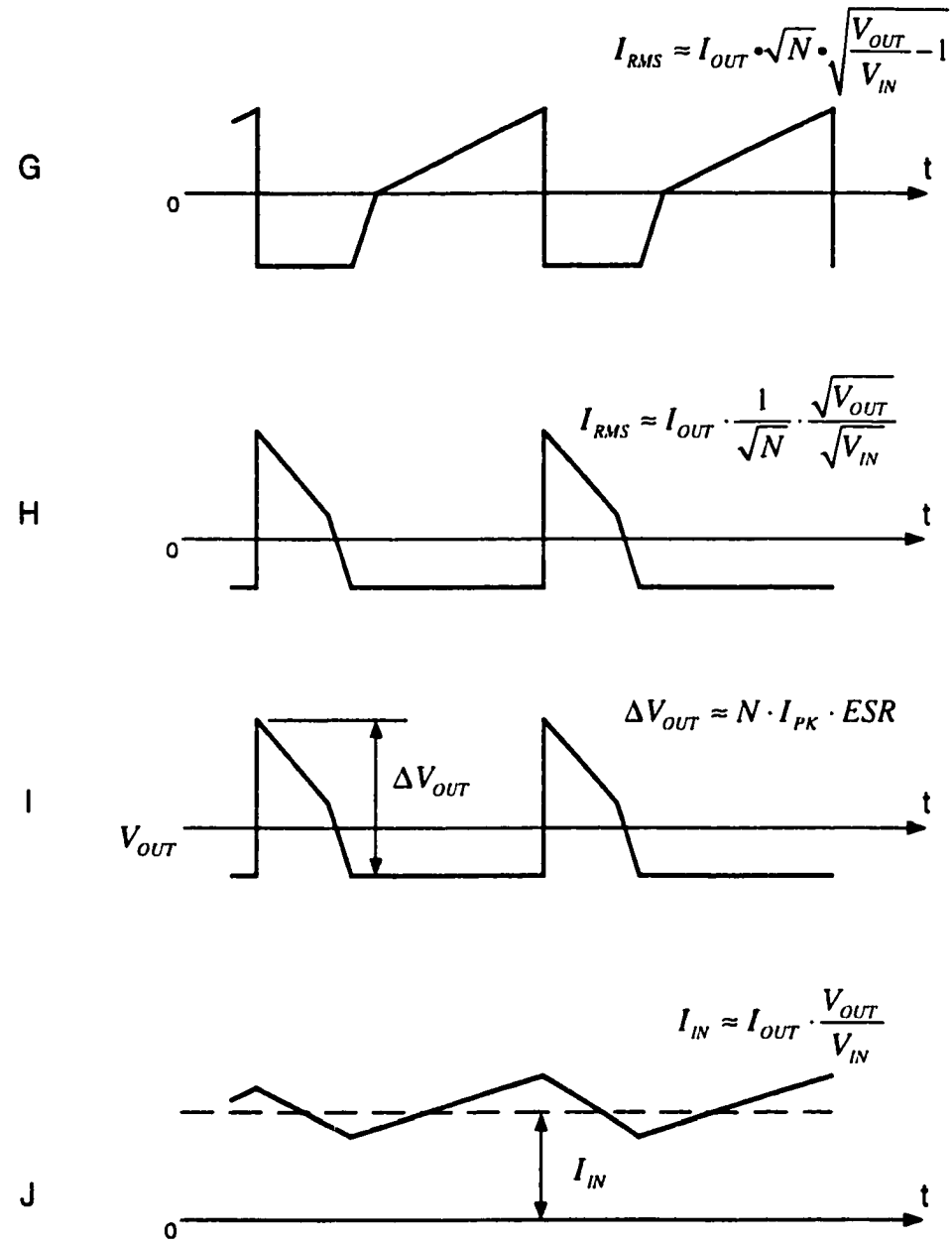

Fig. 2.28 Cont'd. G) IC1, input capacitor current. H) IC2, output capacitor current. I) ΔV_{OUT}, output ripple voltage. J) I_{IN}, input ripple current with filter.

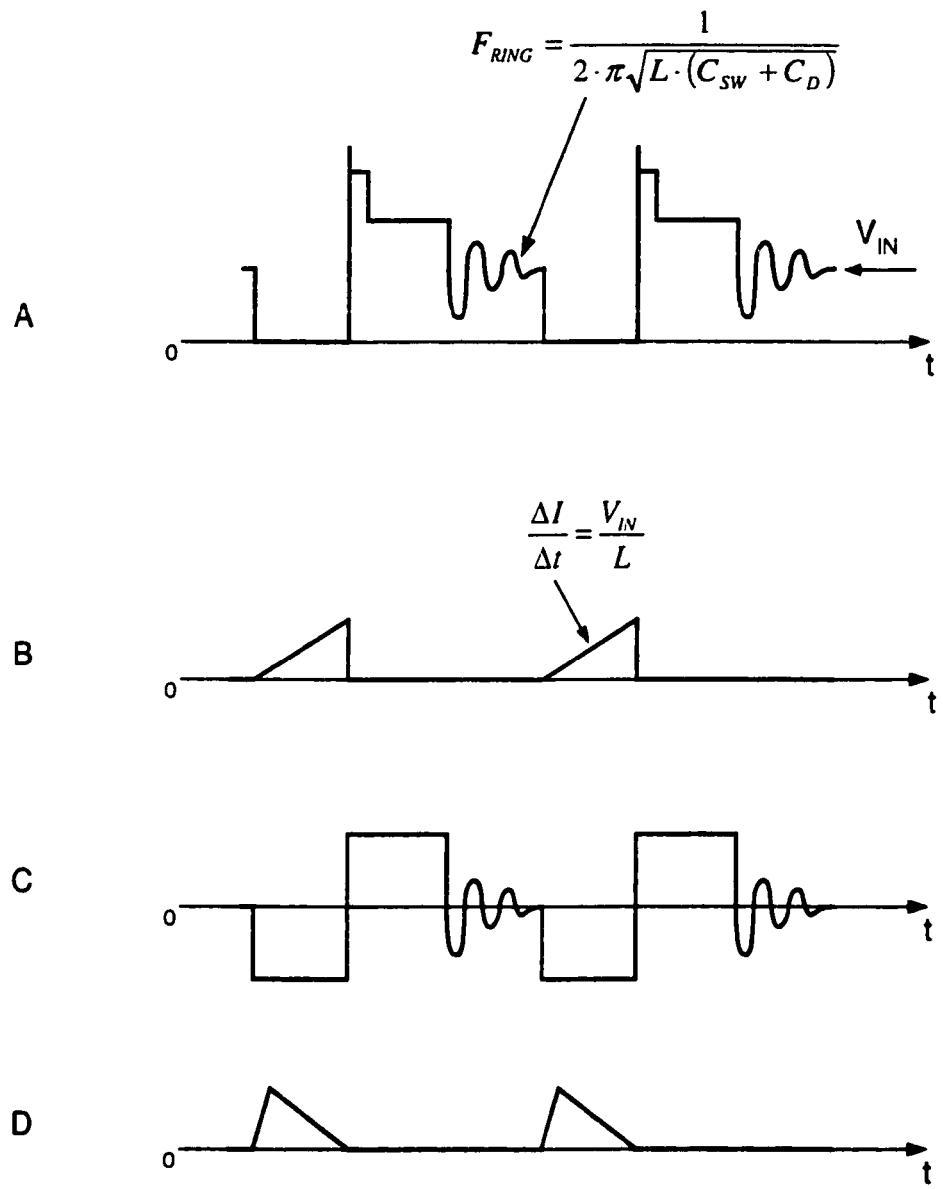

Fig. 2.29 Flyback Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) V_{SEC}, secondary voltage. D) $I_{SECONDARY}$, output diode and secondary current.

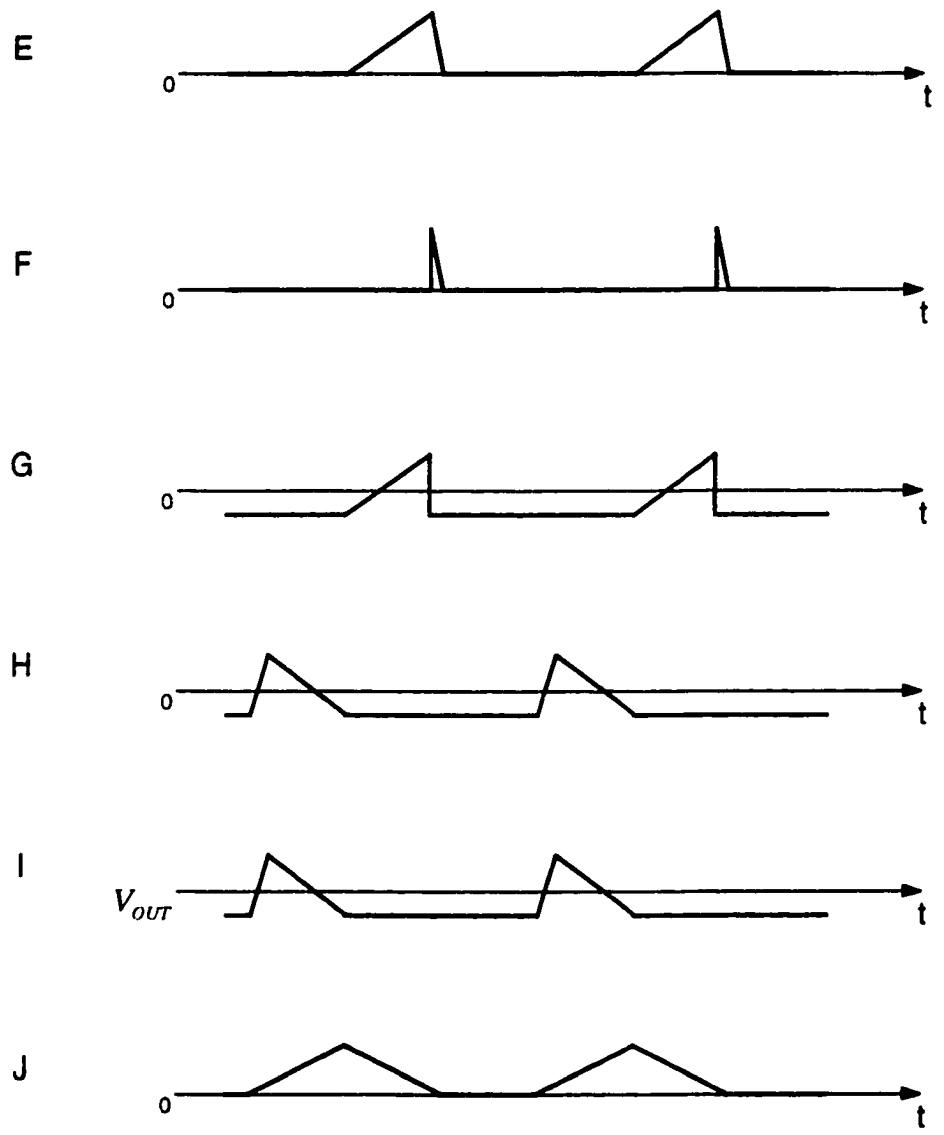

Fig. 2.29 Cont'd. E) $I_{PRIMARY}$, primary current. F) I_{CLIP}, clipper current. G) IC1, input capacitor current. H) IC2, output capacitor current. I) ΔV_{OUT}, output ripple voltage. J) I_{IN}, input ripple current with filter.

Switch Node Voltage: Fig. 2.28A, the voltage here switches between ground and a voltage equal to the output voltage divided by the turns ratio, plus the input voltage. The zener voltage must be chosen wisely, as it must limit the peak V_{SW} node voltage to less than the maximum voltage rating of the switch. And the zener can dissipate excessive

heat if the voltage rating is too low. Once the leakage inductance is dropped to zero, the switch node voltage settles to its normal flyback potential. The narrow spike at the arising edge of the waveform is caused by the transformer leakage inductance. The switch node is the major source of electric field radiation, so it should not be routed near sensitive nodes in the converter circuit. Trace widths to the switch, diode, and inductor must be wide enough to handle the high currents, but the areas should be minimized to avoid excess coupling or radiation.

Switch Current: Fig. 2.28B, the switch current steps from zero to an average value (I_{AV}) that depends on the output current, turns ratio and input and output voltages. The slew rate is very high, so connections between the switch and other adjacent circuit elements must be short to prevent unwanted voltage spikes and parasitic resonances.

Secondary Voltage: Fig. 2.28C, the voltage here switches between a diode drop above the output voltage and a value equal to the turns ratio times the input voltage ($N \times V_{IN}$). With high turns ratio (>5) the transformer's leakage conductance may cause the secondary voltage to swing significantly higher (in this case, more negative) than the equation predicts. The worst case diode reverse voltage occurs at the maximum input voltage. It should be verified that the diode's maximum reverse voltage is not exceeded at this operating point.

Diode/Secondary Current: Fig. 2.28D, the diode current switches from zero to an average value (I_{DAV}) approximately equal to output current divided by one minus the duty cycle (DC).

Primary Current: Fig. 2.28E, the average primary current depends upon the output current, duty cycle, and turns ratio (N), and fluctuates with input and output voltage variations. Peak-to-Peak ripple current (ΔI) is determined by the primary conductance value, switching frequency, and turns ratio (N), but also changes with input voltage. Smaller inductance values result in higher ripple currents and increased core loss and output ripple voltage. Larger inductance values reduce these effects, but usually result in a physically larger transformer.

Clipper Current: Fig. 2.28F, the clipper current is caused by the leakage inductance of the transformer. Its peak amplitude is equal to the peak switch current prior to turn off and the duration of the pulse depends on both switch current and the difference between the flyback voltage and zener voltage.

Input Capacitor Ripple Current: Fig. 2.28G, the peak-to-peak value of the input capacitor current is equal to peak switch current. The RMS ripple current depends on the ratio of the output to input voltage and turns ratio (N).

Output Capacitor Current: Fig. 2.28H, the peak-to-peak value of the output capacitor ripple current is equal to peak diode current. The RMS current depends on the input voltage, load current, and transformer turns ratio.

Output Ripple Voltage: Fig. 2.28I, the output ripple voltage is a function of the output current and the ESR of the output capacitor. The capacitive reactance is assumed to be a dead short at switching frequencies, leaving the ESR as the only impedance. This simplifying assumption does not take into account the inductance of the output capacitor. Capacitor inductance is important because it determines the amplitude of narrow spikes

that appear superimposed on the calculated ripple voltage. These spikes are the result of the fast edges on the current pulses delivered to the output capacitor through the diode. A current slew rate of 10^8A/sec will create 1V spikes 10ns-100ns wide for a capacitor inductance of 0.01μH. these spikes normally eliminated at the load by parasitic inductance in the lines and by the load bypass capacitors. This effect can be greatly enhanced by inserting a small ferrite bead in the output line. These spikes can be completely eliminated if an additional LC output filter is added.

Input Current: Fig. 2.28J, input current normally appears as a moderate amount of ripple superimposed on average DC level because the input capacitor absorbs most of the AC ripple current created by the switching operation. L_p is the equivalent parasitic inductance of the input lines, which aids the filtering action. Ripple current and the input lines is one cause of conducted EMI, so the magnitude of this ripple is important.

2.7 Tapped-Inductor Converters

The tapped-inductor topology (Fig. 2.30) uses a tapped–inductor to increase output current above the maximum current rating of the switch. It accomplishes this at the expense of increased switch voltage during the switch-off time. When the input-output differential is high, there is a significant increase in available output power over the basic buck circuit.

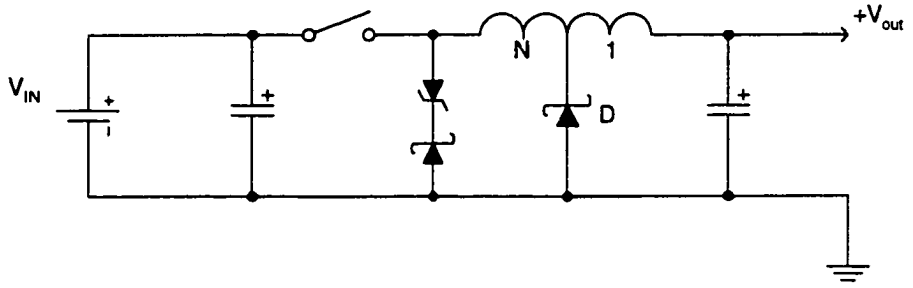

Fig. 2.30 Tapped-Inductor converter

During the switch-on time, the diode(D) is reversed biased and the input provides energy to the load and to the inductor. When the switch turns off, current flows only in the output section of the inductor, label "1" through the diode and into the load. Energy conservation in the inductor requires that the current in section "1" increase above switch current by a ratio of (N+1):1, where "N" is the turn's ratio, resulting in a dramatic increase in the output current delivered to the load.

Tapped-Inductor converters have relatively "noisy" input and "quit" outputs, the basic topology is similar to that of the buck topology. Again a tapped inductor is used which is usually not an off the shelf product.

2.7.1 Tapped-Inductor Circuit Operation

A basic tapped-inductor converter, along with its current and voltage waveforms, is shown in Fig. 2.31. The circuit operation is as follows: switch S1 opens and closes at a rate dependent upon the oscillator frequency. When the switch turns on, the V_{SW} node is pulled to the input voltage. Trace A is the V_{SW} node voltage waveform, and Trace B shows the switch current waveform. While the switch is on, current flows from the input

through the switch and the inductor, and into the load. The in inductor current (Trace D) rises linearly during this period. The change in inductor current, or ripple (ΔI), is determined by the voltage applied across the inductor, its inductance, and the switch-on time.

When the switch opens, current flowing through the inductor forces the voltage on the switch node to drop until D1 becomes forward biased (Trace E), providing a path for the inductor current. Ideally, during this interval the inductor current only flows through the section labeled "1", through the diode and into the output. Energy conservation in the inductor requires the current increases to a ratio of (N + 1):1 which dramatically increases the output current being delivered to the load during this period. To illustrate this effect, if the inductor current prior to turn-off is equal to 1A and N = 3, then current delivered to the output during switch-off time is (3 + 1) 1A = 4A. This jump in the "1" winding can be seen in the inductor current waveform (Trace D).

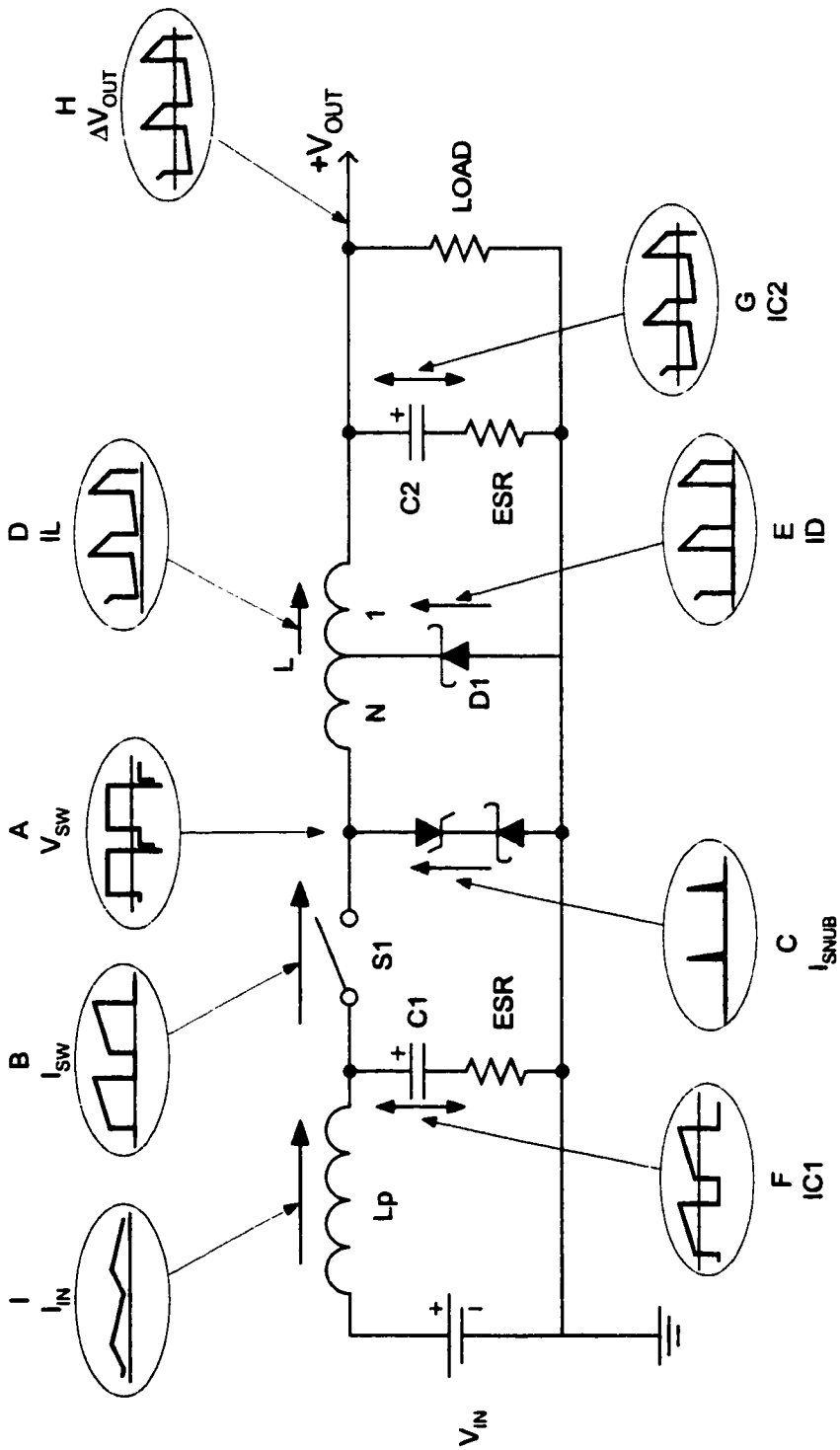

Fig. 2.31 Tapped-Inductor Converter with its Voltage and Current Waveforms

Because the inductor is not an ideal component, not all the energy stored in the core is transferred to the "1" winding. The energy left in the "N" winding resulting from the inductor's leakage inductance causes an overvoltage spike on the falling edge of the switch node voltage (Trace A). The series zener/diode network clamps the V_{SW} node, providing a current path for the leakage inductance spike (Trace C). Once the leakage inductance current has fallen to zero, the V_{SW} node voltage settles to a negative potential equal to the turns ratio (N) times the output voltage.

The filter capacitors provide a low impedance path for the AC component of the input and diode currents. The input capacitor's current waveform (Trace F) is the same as the switch current (Trace B), except that the capacitor has no DC component. The input capacitor RMS ripple current is approximately equal to 0.25 times the output current for N = 3. An input filter capacitor is essential for the proper operation of the circuit. It absorbs the current pulses inherent in a buck converter. Without an input filter capacitor close to the buck circuit, this ripple current in conjunction with lead and printed circuit trace inductances, could cause enough ripple voltage to produce erratic operation.

The output filter capacitor current waveform (Trace G) is the same as the inductor current less the DC component. Its RMS ripple current value is approximately 0.4 times the output current for N = 3. The output capacitor's RMS ripple current is significantly higher for this architecture compared to the basic buck circuit and therefore requires a physically larger output capacitor.

Current and voltage waveforms of a continuous mode basic tapped-inductor converter are shown in Fig. 2.32. While Fig. 2.33 shows the waveforms of a discontinuous mode.

Continuous mode operation is described next in detail. It is preferred to discontinuous mode because it maximizes the available output power for a given converter.

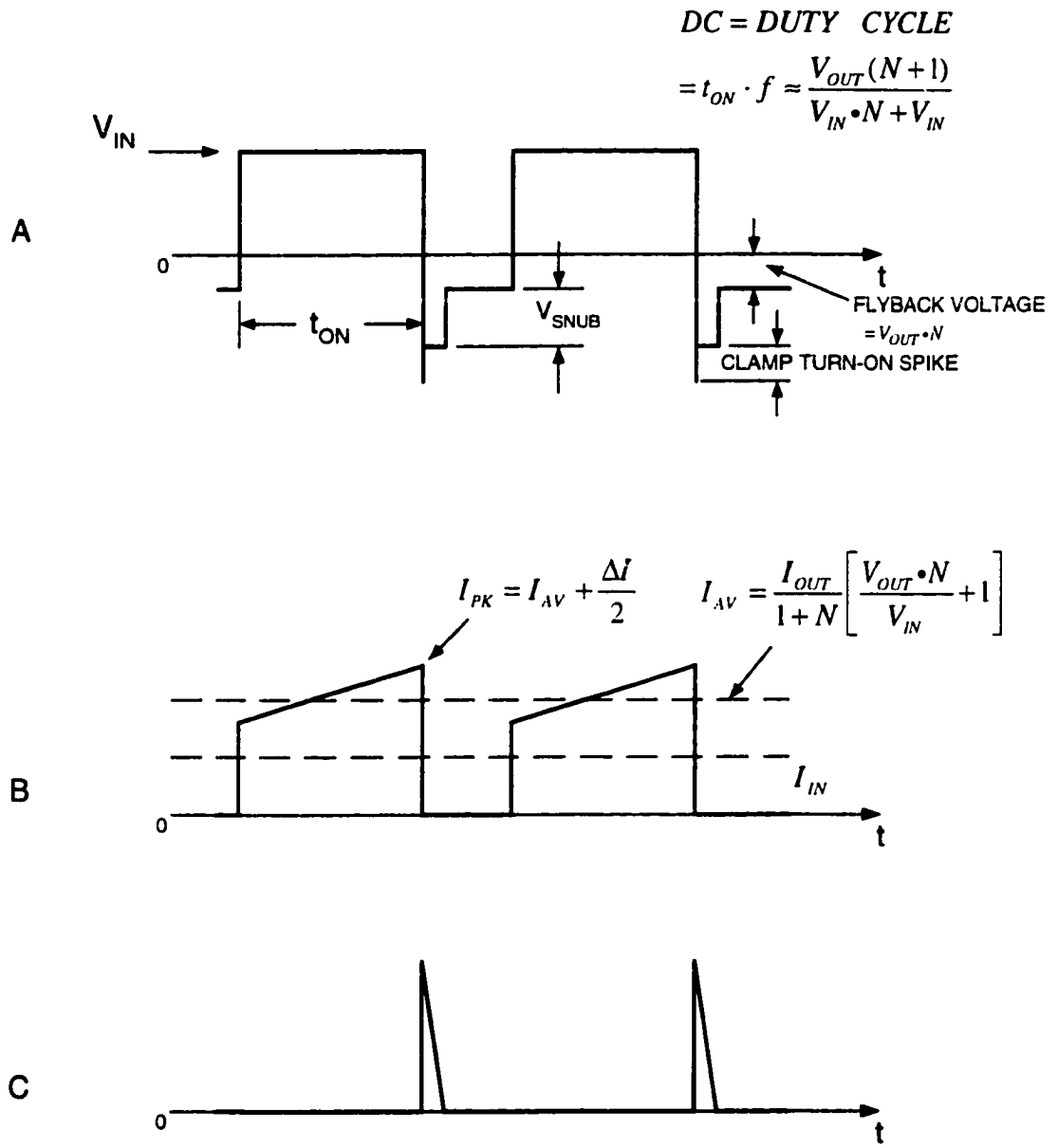

Fig. 2.32 Tapped-Inductor Converter Waveforms. Continuos Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) I_{SNUB}, snubber current.

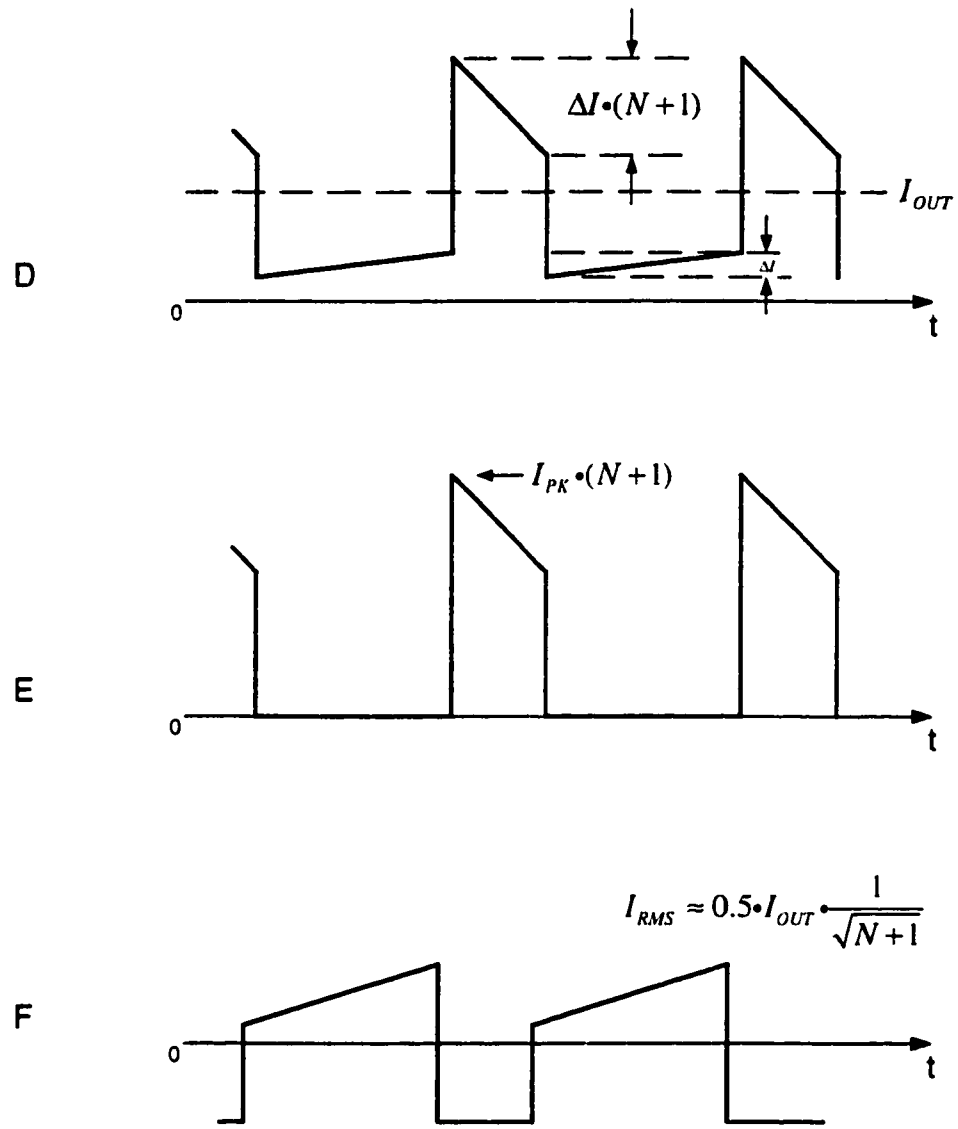

Fig. 2.32 Cont'd. D) IL, inductor "1" current with filter. E) ID, diode current. F) IC1, input capacitor current.

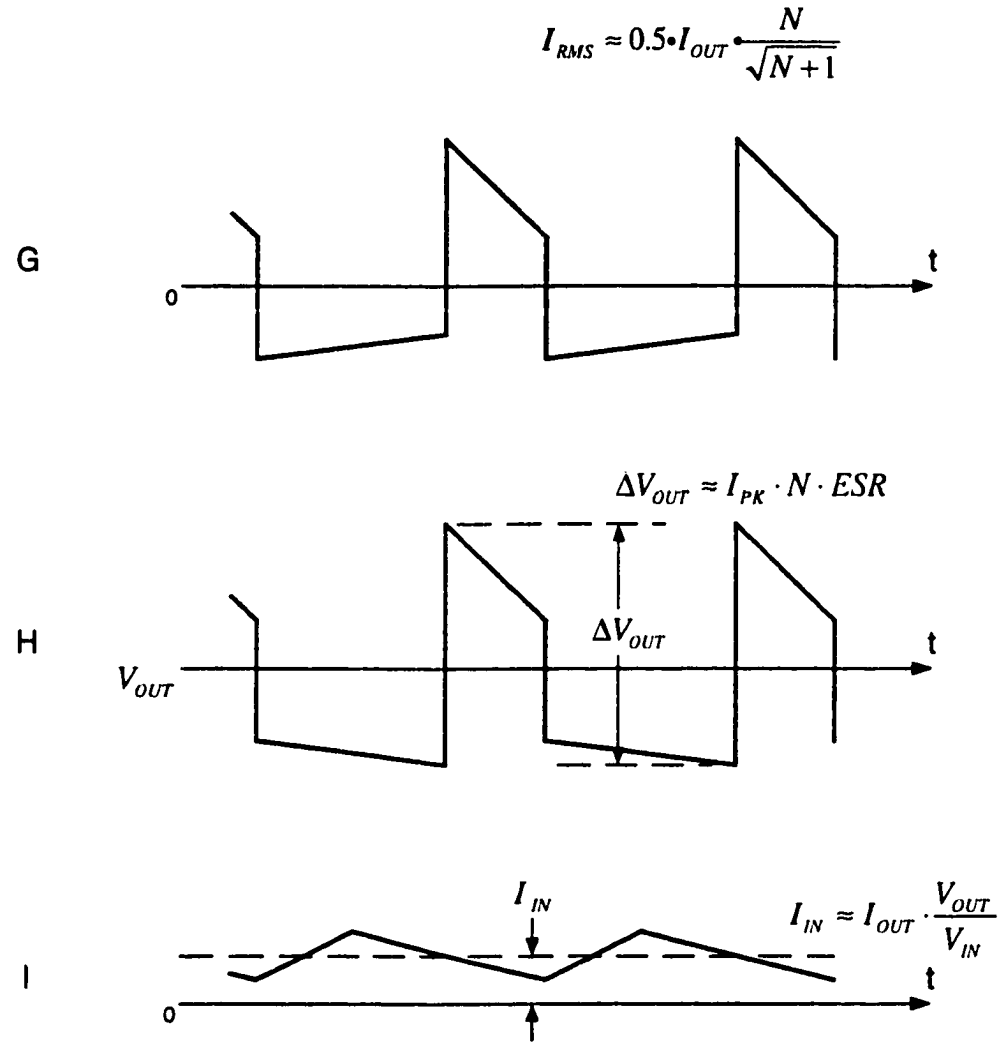

Fig. 2.32 Cont'd. G) IC2, output capacitor current. H) ΔV_{OUT}, output ripple voltage. I) I_{IN}, input ripple current with filter.

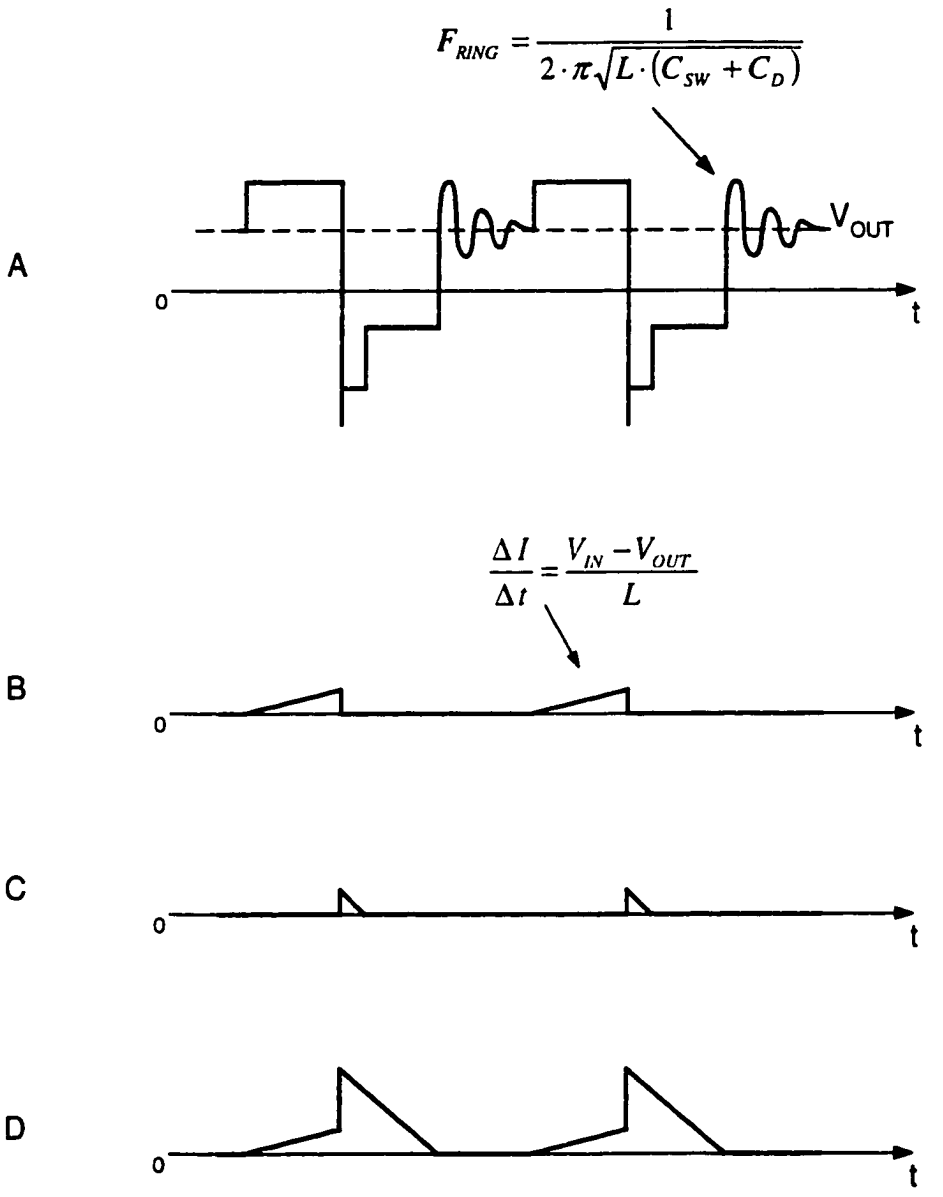

Fig. 2.33 Tapped-Inductor Converter Waveforms. Discontinuous Mode. A) V_{SW}, switch node to ground voltage. B) I_{SW}, switch current. C) I_{SNUB}, snubber current. D) IL, inductor "1" current with filter.

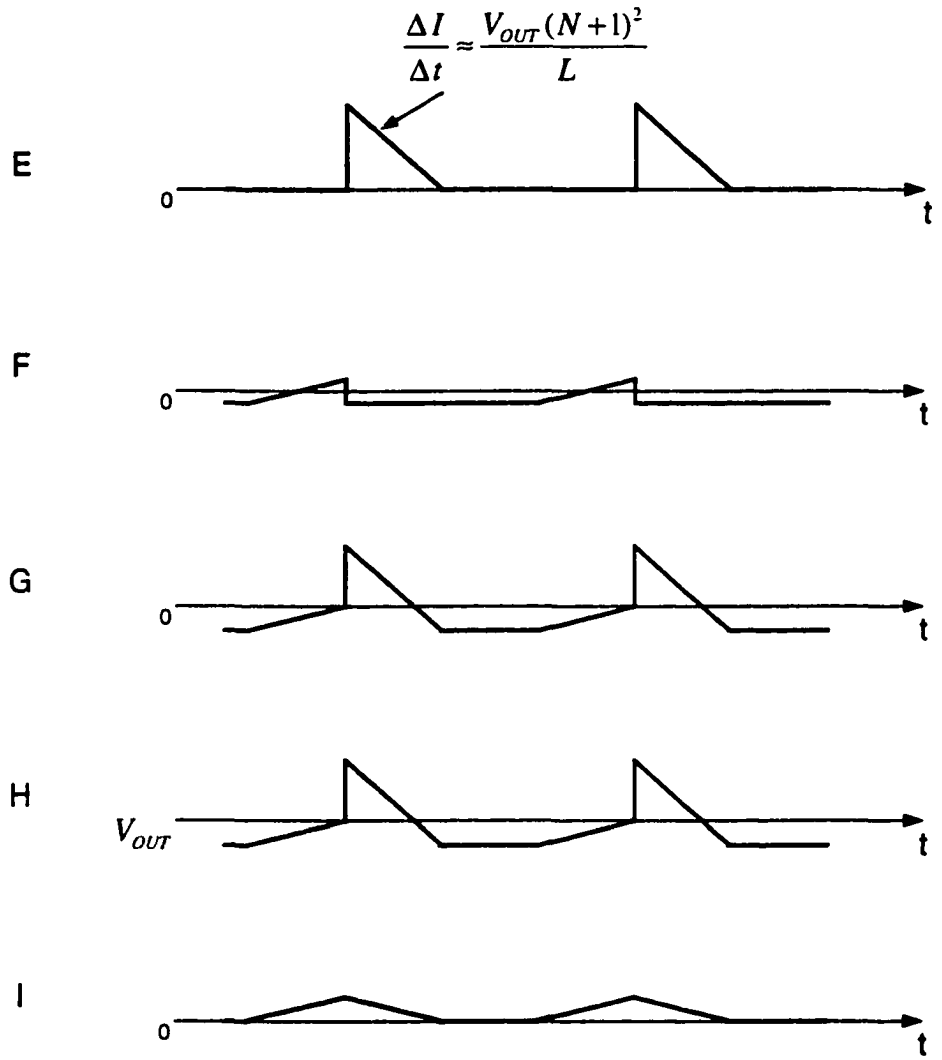

Fig. 2.33 Cont'd. E) ID, diode current. F) IC1, input capacitor current. G) IC2, output capacitor current. H) ΔV_{OUT}, output ripple voltage. I) I_{IN}, input ripple current with filter.

Switch Node Voltage: Fig. 2.32A, the voltage here switches between the input voltage (V_{IN}) and to a potential below ground set by the output voltage times the turns ratio. The overvoltage spike is caused by the inductor's leakage inductance and is clamped by the zener/diode network. The zener voltage must be chosen wisely, as it must limit the negative peak V_{SW} node voltage to less than destructive levels. Excessive heat dissipation will result if its voltage rating is too low. The switch node is the major source of electric field radiation, so it should not be routed near sensitive nodes in the converter circuit. Trace widths to the switch, diode, and inductor must be wide enough to handle the high currents, but the areas should be minimized to avoid excess coupling or radiation.

Switch Current: Fig. 2.32B, the switch current steps from zero to an average value of approximately 0.4 times the output current when the input voltage is 4 times the output voltage and N = 3. The slew rate is very high, so connections between the switch and other adjacent circuit elements must be short to prevent unwanted voltage spikes and parasitic resonances.

Clipper Current: Fig. 2.32C, the clipper current is caused by the leakage inductance of the tapped inductor. Its peak amplitude is equal to the peak switch current prior to turn off and the duration of the pulse depends on both switch current and the difference between the flyback voltage ($V_{OUT} \times N$)and the zener voltage.

Inductor "1" Current: Fig. 2.32D, the average current through the inductor section "1" is equal to the output current. Peak-to-Peak ripple current (ΔI) is determined by the inductance conductance value, switching frequency, and turns ratio (N), but also changes

with input voltage. Smaller inductance values result in higher ripple currents and increased core loss and output ripple voltage. Larger inductance values reduce these effects, but usually result in a physically larger coil.

Diode Current: Fig. 2.32E, the diode current switches from zero to a value approximately twice the output current for N = 3. In most applications the average diode current will be slightly less the load current.

Input Capacitor Ripple Current: Fig. 2.32F, the peak-to-peak value of the input capacitor current is equal to peak switch current. The RMS ripple current is approximately 0.25 times the output current for N = 3.

Output Capacitor Current: Fig. 2.32G, the peak-to-peak value of the output capacitor ripple current is equal to peak switch current multiplied by the turns ratio. The RMS current is approximately 0.75 times the output current for N = 3.

Output Ripple Voltage: Fig. 2.32H, the output ripple voltage is a function of the output current and the ESR of the output capacitor. The capacitive reactance is assumed to be a dead short at switching frequencies, leaving the ESR as the only impedance.

Input Current: Fig. 2.28J, input current normally appears as a moderate amount of ripple superimposed on average DC level because the input capacitor absorbs most of the AC ripple current created by the switching operation. L_p is the equivalent parasitic inductance of the input lines, which aids the filtering action. Ripple current and the input lines is one cause of conducted EMI, so the magnitude of this ripple is important.

2.8 Switched Capacitor Converters.

Switched capacitor converters can perform voltage doubling, tripling and inverting or a mix of the above, they provide voltages that are opposite or of the same polarity as the input voltage. A capacitor instead of an inductor or a transformer provides the means for transferring the charge between the input and the output, the capacitor electric field rather than the inductor magnetic field is the intermediate energy storage medium.

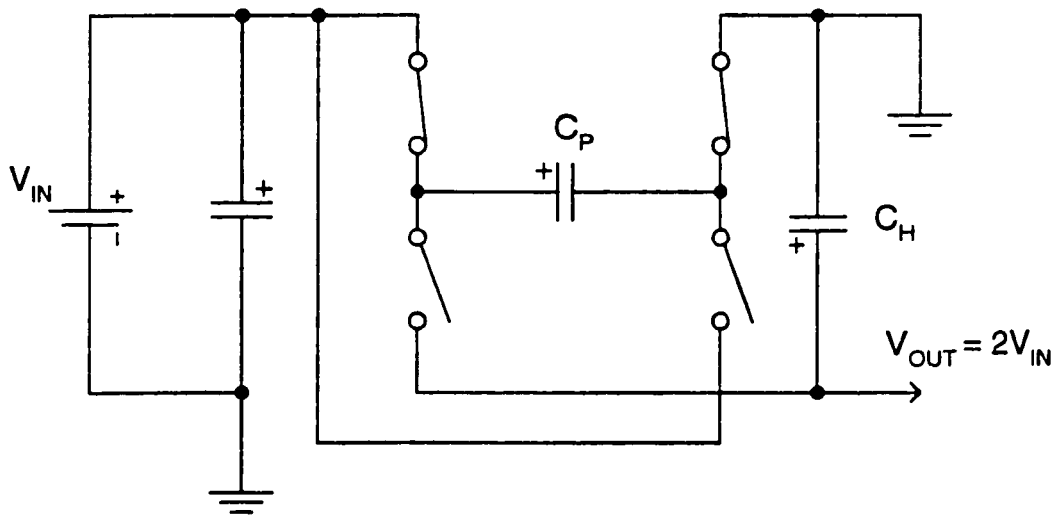

Fig. 2.34 Switched Capacitor Converter, Doubler configuration

In a voltage doubler configuration (Fig. 2.34), the upper set of switches are closed in the first half of the clock cycle, and the pump capacitor (C_P) is charged to a value close to the supply voltage, in the other half of the cycle, C_P is connected across the hold capacitor C_H such that the negative plate is connected to the supply voltage, C_H is charged to up to twice the supply voltage.

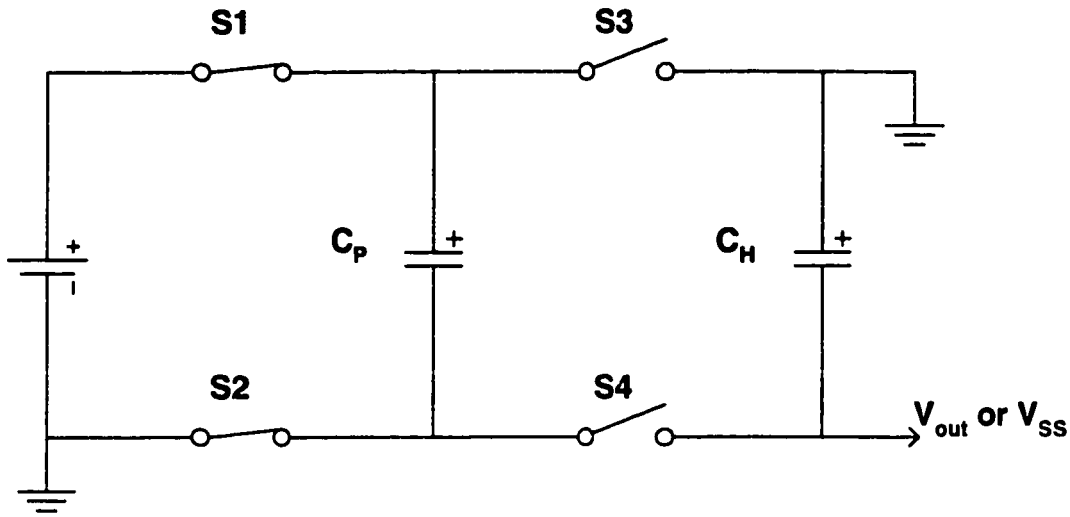

Fig. 2.35 Positive to Negative Switched Capacitor Converter

In an inverter configuration (Fig. 2.35), the circuits functions the same except that the positive plate of C_P is connected to ground rather than the negative plate being connected to the supply voltage in the doubler. In both configurations, as the clock is running, charge is "pumped" through the C_P and is accumulated at the hold capacitor C_H.

For triplers and negative doublers, more capacitors are used and are switched in the same manner where they get charged and then are cascaded, and a voltage that is higher in magnitude than the supply voltage is obtained.

Switched capacitor converters are favored in integrated circuit designs over inductor or transformer based converters. Among the favorable features is that there are no excessive values of voltages being applied to the switches. Capacitors impede instantaneous changes in voltages, but they allow instantaneous changes in current values, and that is a

disadvantage of this topology. Noise in the form of current spikes, exists at both the input and the output port, so they are considered to be noisy at the input and at the output.

This topology is a popular one for low power applications where the load is below 1W. The negative biasing in GaAs integrated circuits, typically consumes less than 10mA at 5V, so at 50mW switched capacitor converters make good candidates, low power capability and high conversion efficiency, combined with the low profile of ceramic capacitors had made switched capacitor converters a popular choice in battery operated equipment.

In the next chapter, the switched capacitor topology waveforms are presented in details.

2.9 Other Topologies

The previous sections covered the most common converter topologies. There are several others that are also widely used. Among those are; resonant, Cuk and Sepic converters.

3 CHAPTER III

Switched Capacitor Technique

3.1 Introduction

The process targeted for the fabrication of GaAs DC/DC converters [1], has high quality capacitors and resistors. The inductors have moderate quality factors in the order of 8-12 at 1GHz. The process has high power (up to 250 mA/mm at 0.5um gate length) depletion mode MESFET's and lower current devices can be achieved through the use of longer gate length MESFET's. The switched capacitor topology is a good candidate for this process. Large values of on-chip inductors are not practical and off-chip inductors are also large in size with a lot of EMI emissions.

Lower current device can be used to build the oscillator while higher current devices can be used for the switches. Coupling capacitors have to be used to drive the depletion mode MESFET's since the gates are non-insulating.

3.2 GaAs implementation of a switched capacitor topology

The circuit shown in Fig. 3.1 depicts a switched capacitor circuit design that was fabricated in GaAs IC technology [6], [7], [10]. In this design D-MESFET's along with resistors and capacitors are fabricated on the same chip. Fig. 3.1 is a GaAs circuit implementation of the topology shown in Fig. 2.35. M5 and M7 are S1 and S2 respectively and M6 and M8 are S3 and S4 respectively. M1, M2, M3 and M4 comprise a multivibrator (oscillator) that generates two clock signals that are 180° out of phase.

R1, R2, C1 and C2 set the oscillation frequency. C_{C1}, C_{C2} and C_{C3} are on-chip coupling capacitors. C_P is the "pump" capacitor that transfers the charge from the supply to the "hold" capacitor C_H. Both C_P and C_H are external capacitors. V_{GEN} is the supply voltage and (V_{OUT} or V_{SS}) is the output negative voltage.

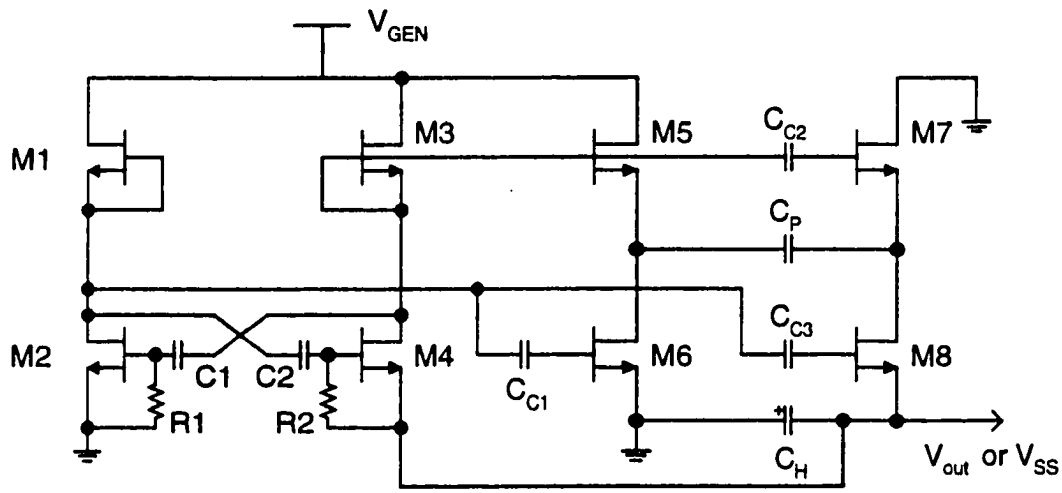

Fig. 3.1 A GaAs switched capacitor DC to DC converter.

A bootstrap connection between VSS and the source of M4 helps in the oscillator start up since it creates asymmetrical oscillator circuitry. The bootstrap also helps maintain a large voltage swing in the circuit which is crucial to the converter efficiency. Large voltage swings ensure proper switching of the FET's in the circuit. Inadequate voltage swings partially turn the switches on and off, and that creates an overlap condition which severely affects the converter efficiency. An overlap condition occurs when two transistors are ON at the same time such that a path is created from the supply or Vout to

ground. If M5 and M6 are ON at the same time, an overlap condition is created, the same applies for M7 and M8.

M6, M7 and M8 are capacitively coupled to the oscillator section to maintain proper DC bias. The DC bias on M6, M7 and M8 is maintained by the clamping action of the parasitic gate diodes and the capacitors C_{C1}, C_{C2} and C_{C3}. The clamping action of the diodes causes V_{GS} of M6, M7 and M8 to swing from +0.5 to a negative voltage. Also, the peak to peak value of V_{GS6} and V_{GS8} is equal to the voltage swing on the drain of M2, and the peak to peak value of V_{GS7} is equal to that of the voltage swing on the drain of M4.

The circuit shows that the gate of M5 need not be capacitively coupled to the oscillator. Direct coupling is possible because M5 can have the same DC level that exists on the drain of M4, while still ensuring that it turns on and off synchronously with M6.

3.3 Oscillator Frequency

The oscillator frequency has to be predictable from design and process parameters. The oscillator acts as a noise source when this circuit is used in a system, so the frequency allocation has to be set by design. In an amplifier like those used in cellular phones, the oscillator causes a spur around the carrier frequency. That spur can fall over an adjacent channel, or it can fall in the receiving channel.

In order to derive an analytical solution for the oscillator frequency, we need to closely examine the oscillator waveforms.

Fig. 3.2 shows the voltage waveform at the gate of M2. At steady state, M2 and M4 are switching on and off alternatively. When M4 turns on, the drain voltage collapses to be close to the source voltage, Vout, and that change in voltage is capacitively coupled to the gate of M2, which in turn, turns it off. M2 remains off as long as the gate to source voltage is lower than the threshold voltage, V_T, which is negative for depletion mode MESFET's. The gate voltage of M2 starts to rise with a time constant equal to R_1C_1, and when VG_2 reaches the threshold voltage, M2 turns on. The resulting collapse in the drain voltage of M2, is capacitively coupled to the gate of M4, which turns M4 off, and the cycle continues.

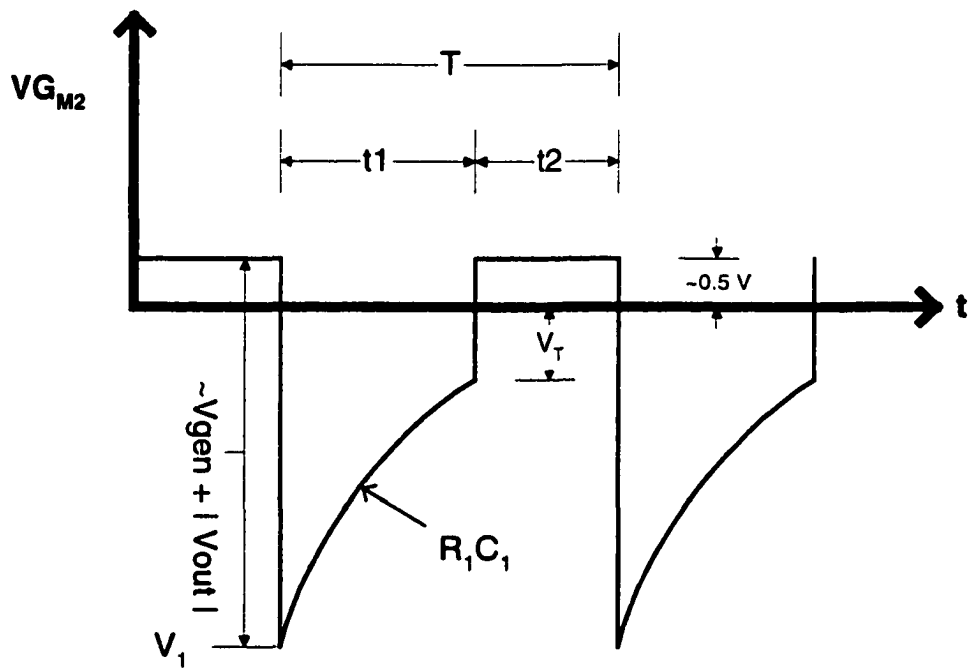

Fig. 3.2 Voltage waveform at the gate of M2.

In the next section we are going to develop a closed from solution for the oscillator frequency.

Due to the capacitive coupling between the drain of M4 and the gate of M2 and assuming that

$$C_1 >> (C_{GS} + C_{GD})_{M2} \tag{3.1}$$

Where CGS and CGD are the gate-to-source and gate-to-drain capacitance of M2 respectively, the gate voltage of M2 (VG_{M2}) is level shifted by a value equal to the magnitude of the peak-to-peak value of VD4. Right after the voltage drop, the gate voltage starts rising in time with a time constant of R_1C_1.

Thus:

$$V(t) = V_1 e^{-t/R_1C_1} \tag{3.2}$$

Assuming that the negative pulse occurs at t=0, then:

$$V(t_1) = V_1 e^{-t_1/R_1C_1} = V_T \tag{3.3}$$

where V_T is the MESFET's threshold voltage, which has a negative value for depletion mode MESFET's as shown in Fig. 3.2. In this analysis however, V_T is treated as a positive number.

rearranging

$$e^{-t_1/R_1C_1} = \frac{V_T}{V_1} \tag{3.4}$$

$$t_1 / R_1C_1 = -\ln(\frac{V_T}{V_1}) = \ln(\frac{V_1}{V_T}) \tag{3.5}$$

and solving for t_1:

$$t_1 = R_1 C_1 \ln(\frac{V_1}{V_T}) \tag{3.6}$$

where $V_1 \approx V_{gen} + |V_{out}| - 0.5$

The same analysis applies to t_2, such that

$$t_2 = R_2 C_2 \ln(\frac{V_2}{V_T}) \tag{3.7}$$

where $V_2 \approx V_{gen} - 0.5$

if T is the total period

$$T = t_1 + t_2 \tag{3.8}$$

the oscillator frequency

$$f_{osc} = \frac{1}{R_1 C_1 \ln(\frac{V_1}{V_T}) + R_2 C_2 \ln(\frac{V_2}{V_T})} \tag{3.9}$$

in order to get 50% duty cycle

$$t_1 = t_2 \tag{3.10}$$

also under light load

$$V_{out} = V_{gen} \tag{3.11}$$

and for values of $V_{gen} >> 0.5V$ and 50% duty cycle

$$t_1 = R_1 C_1 \ln(\frac{2V_{gen}}{V_T}) = t_2 = R_2 C_2 \ln(\frac{V_{gen}}{V_T}) \tag{3.12}$$

$$\frac{R_1 C_1}{R_2 C_2} = \frac{\ln(\frac{V_{gen}}{V_T})}{\ln(\frac{2V_{gen}}{V_T})} \tag{3.13}$$

for C1=C2:

$$R_1 = R_2 \bullet \left[\frac{\ln(\frac{V_{gen}}{V_T})}{\ln(\frac{2V_{gen}}{V_T})} \right] \tag{3.14}$$

For V_T=0.3V, V_{gen}=5V, R_l=155K, C_l=4pF, 50% duty cycle and under light load

$$f_{osc} = \frac{1}{2 \cdot 155 \cdot 10^3 \times 4 \cdot 10^{-12} \times \ln(\frac{5+5-0.5}{0.3})} \approx 233KHz \qquad (3.15)$$

The oscillator frequency varies with load and with the supply voltage. As the load current increases, the output voltage drops, thus reducing the swing, V1 shown in Fig. 3.2. This causes the oscillator frequency to increase. Similarly, lower supply voltage causes the oscillator frequency to increase.

3.4 Output Resistance

In order to calculate the output resistance, the circuit is analyzed in sections. First let us derive the equivalent resistance of the switched capacitor shown in Fig. 3.3. The circuit is analyzed from a charge perspective [8], [9]. Since the switches are controlled by a pair of non-overlapping clocks, C is charged to V1 and then to V2 during each clock period, therefore the change in charge over one clock period, ΔQ that is transferred from V1 into V2 is

$$\Delta Q = C(V1 - V2) \qquad (3.16)$$

but, the average dc current flowing from V1 to V2 is

$$I_{eq} = \Delta Q / T \qquad (3.17)$$

where T is the period and is the reciprocal of the switching frequency F

$$I_{eq} = \frac{C(V1-V2)}{T} = FC(V1-V2) \tag{3.18}$$

$$R_{eq} = \frac{(V1-V2)}{I_{eq}} = \frac{1}{FC} \tag{3.19}$$

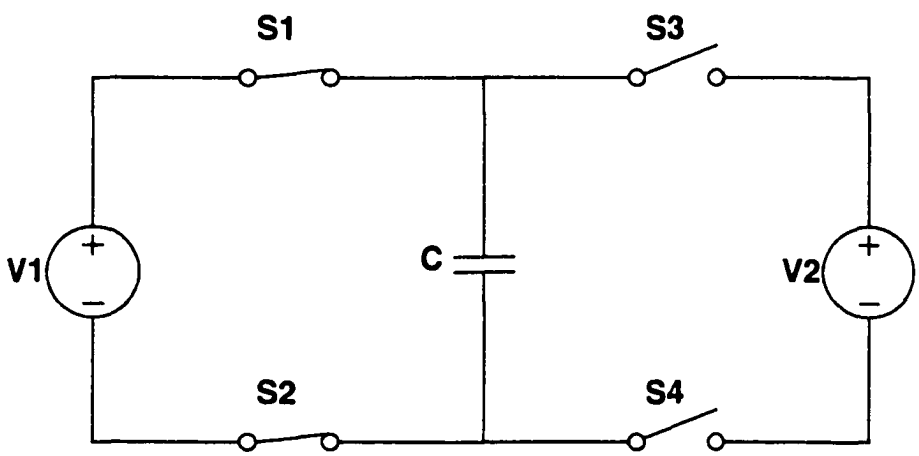

Fig. 3.3 Switched Capacitor equivalent impedance calculation.

Next, we include the effect of the ON resistance of the switches and the capacitors equivalent series resistance (ESR).

Fig. 3.4 and Fig. 3.5 show the steady state equivalent circuits of the switched capacitor converter of Fig. 3.3. In phase one, the load current is supplied by the hold capacitor C_H, and in phase two, the load current is supplied by the pump capacitor C_P. In addition to supplying the load current in phase two, C_P is also replenishing the charge lost by C_H in phase one, so the average current that is delivered by C_P is twice the load current as

shown in Fig. 3.5. Cp has to supply twice the load current in phase two, and that is why it draws twice the load current in phase one.

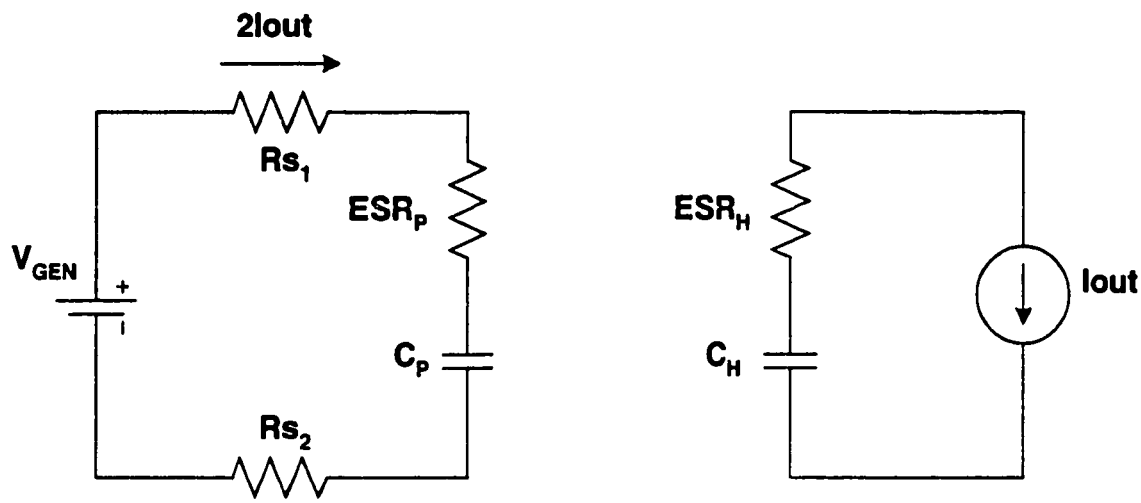

Fig. 3.4 Phase one of the operation of the switched capacitor converter.

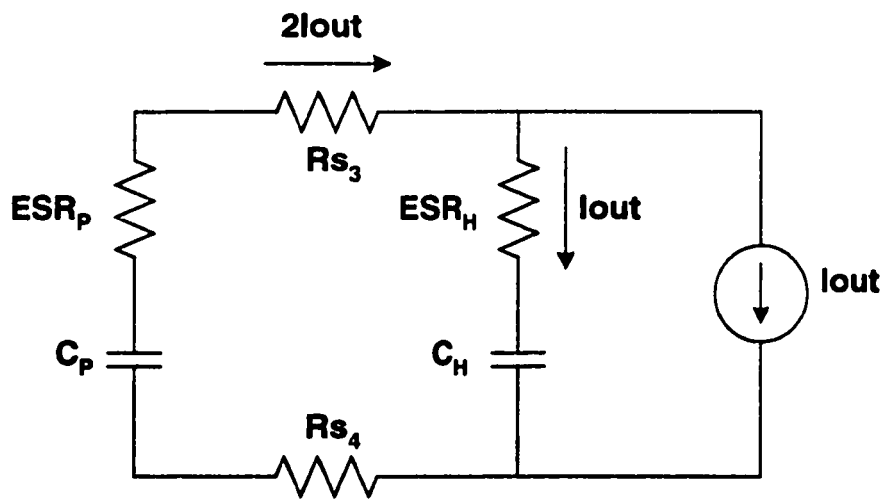

Fig. 3.5 Phase two of the operation of the switched capacitor converter.

Now that we have the equivalent circuits and the resistive components, the power loss is calculated as:

The power dissipated in phase one is

$$P_{lost1} = I^2 \cdot R = (2 \cdot Iout)^2 (Rs_1 + Rs_2 + ESR_P) + Iout^2 (ESR_H) \quad (3.20)$$

$$P_{lost2} = I^2 \cdot R = (2 \cdot Iout)^2 (Rs_3 + Rs_4 + ESR_P) + Iout^2 (ESR_H) \quad (3.21)$$

$$P_{lost} = \frac{P_{lost1} + P_{lost2}}{2} \quad (3.22)$$

assuming that the switches are identical and have an ON resistance of Rs then

$$P_{lost} = I^2 \cdot R = (Iout)^2 (8Rs + 4ESR_P + ESR_H) \quad (3.23)$$

The output resistance has two terms, one term from the contribution of the lossy components and the other is from the equivalent resistance of the switched capacitor thus

$$R_{out} = 8Rs + 4ESR_P + ESR_H + \frac{1}{FC_P} \tag{3.24}$$

This result is important in the design of switched capacitor converters. It shows the contribution of the various circuit components to the output resistance. C_P contributes more to the output resistance than C_H does. But, C_H has a larger effect on the output ripple. The choice of capacitors is crucial to the performance of switched capacitor DC-DC converters. Size, ESR and the reactive impedance Xc has to be taken into consideration.

The circuit fabricated had an oscillator frequency of about 250KHz, a pump capacitor C_P of 0.1uF and the ON resistance of the MESFET's is about 4 Ω. ESR_P is in the order of 1Ω, ESR_H is in the order of 0.1Ω. Calculating the output resistance using these values yields:

$$R_{out} = 32 + 4 + 0.1 + 40 \approx 76\Omega \tag{3.25}$$

Choosing a larger C_P yields a lower output resistance, and choosing a larger C_H yields a slightly lower output resistance.

3.5 Energy and power loss during capacitor charging

In this section we examine the energy loss during a charge sharing between two capacitors. Fig. 3.6 shows two capacitors C1 and C2 with initial voltages V1 and V2 respectively. The capacitors are disconnected and can be connected together via the switches S1 and S2.

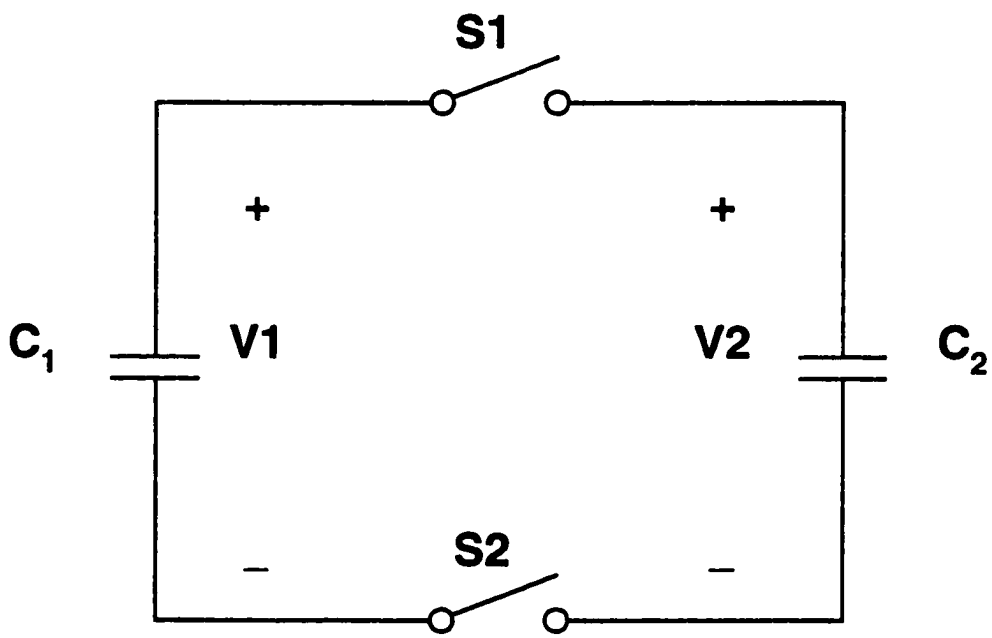

Fig. 3.6 The two capacitors are initially disconnected.

The energy in the system is given by:

$$E_B = \frac{C_1 \cdot V_1^2 + C_2 V_2^2}{2} \tag{3.26}$$

Fig. 3.7 shows the system with the switched closed. The charge on the capacitors plates will be redistributed such that the resultant voltage across the two capacitors is the same.

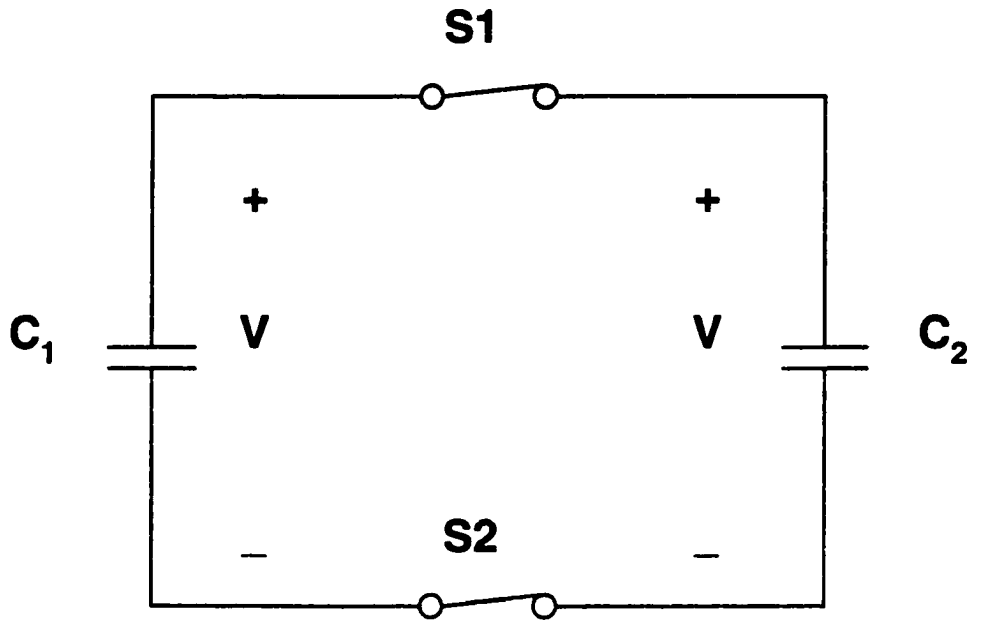

Fig. 3.7 The switches are close, C_1 and C_2 share the same voltage, V.

Conservation of charge principle applies, where the total charge in the system before and after the switches are closed is the same. The total charge in the system before the switches are closed is given by:

$$Q = C_1 \cdot V_1 + C_2 V_2 \tag{3.27}$$

After the switches are closed, the two capacitors share the same voltage and the total charge is the same as before:

$$Q = (C_1 + C_2) \cdot V \tag{3.28}$$

solving for V

$$V = \frac{C_1 \cdot V_1 + C_2 V_2}{(C_1 + C_2)} \tag{3.29}$$

And the system energy after the switches are closed is:

$$E_A = \frac{C_1 + C_2}{2}\left[\frac{C_1 \cdot V_1 + C_2 V_2}{C_1 + C_2}\right]^2 \tag{3.30}$$

If we define the energy transfer efficiency to be

$$\eta = \frac{E_A}{E_B} \tag{3.31}$$

By rearranging and expanding the terms

$$\eta = \frac{C_1^{\,2}V_1^{\,2} + 2C_1V_1C_2V_2 + C_2^{\,2}V_2^{\,2}}{C_1^{\,2}V_1^{\,2} + C_1C_2V_2^{\,2} + C_1C_2V_1^{\,2} + C_2^{\,2}V_2^{\,2}} \tag{3.32}$$

divide both the numerator and denominator by $C_1^{\,2}V_1^{\,2}$

$$\eta = \frac{1 + 2\frac{C_2}{C_1}\frac{V_2}{V_1} + \left(\frac{C_2}{C_1}\right)^2\left(\frac{V_2}{V_1}\right)^2}{1 + \frac{C_2}{C_1}\left(\frac{V_2}{V_1}\right)^2 + \frac{C_2}{C_1} + \left(\frac{C_2}{C_1}\right)^2\left(\frac{V_2}{V_1}\right)^2} \tag{3.33}$$

If we define

$$r_C \overset{\Delta}{=} \frac{C_2}{C_1} \tag{3.34}$$

and

$$r_V \overset{\Delta}{=} \frac{V_2}{V_1} \tag{3.35}$$

then

$$\eta = \frac{1 + 2r_C r_V + r_C{}^2 r_V{}^2}{1 + r_C r_V{}^2 + r_C + r_C{}^2 r_V{}^2} \tag{3.36}$$

Combine the terms in the numerator and add and subtract $2r_C r_V$ in the denominator, we get

$$\eta = \frac{(1 + r_C r_V)^2}{1 + 2r_C r_V + r_C{}^2 r_V{}^2 + r_C - 2r_C r_V + r_C r_V{}^2} \tag{3.37}$$

combine the terms in the denominator

$$\eta = \frac{(1 + r_C r_V)^2}{(1 + r_C r_V)^2 + r_C (1 - r_V)^2} \tag{3.38}$$

compact

$$\eta = \frac{1}{1 + a} \tag{3.39}$$

where

$$a = r_C \left(\frac{1 - r_V}{1 + r_C r_V} \right)^2 \tag{3.40}$$

The energy transfer efficiency is close to 100% if "a" is very small. This happens if $V_2 \cong V_1$, or if r_C is too small or too large. It is the current flow that causes a loss in energy which is transmitted as an electromagnetic energy. Systems that use switched capacitors to transfer energy exhibit higher losses at startup, where the capacitors are

initially discharged. They also exhibit loss in the transferred energy under high load conditions, where the capacitors lose most of their charge per cycle causing larger voltage drops.

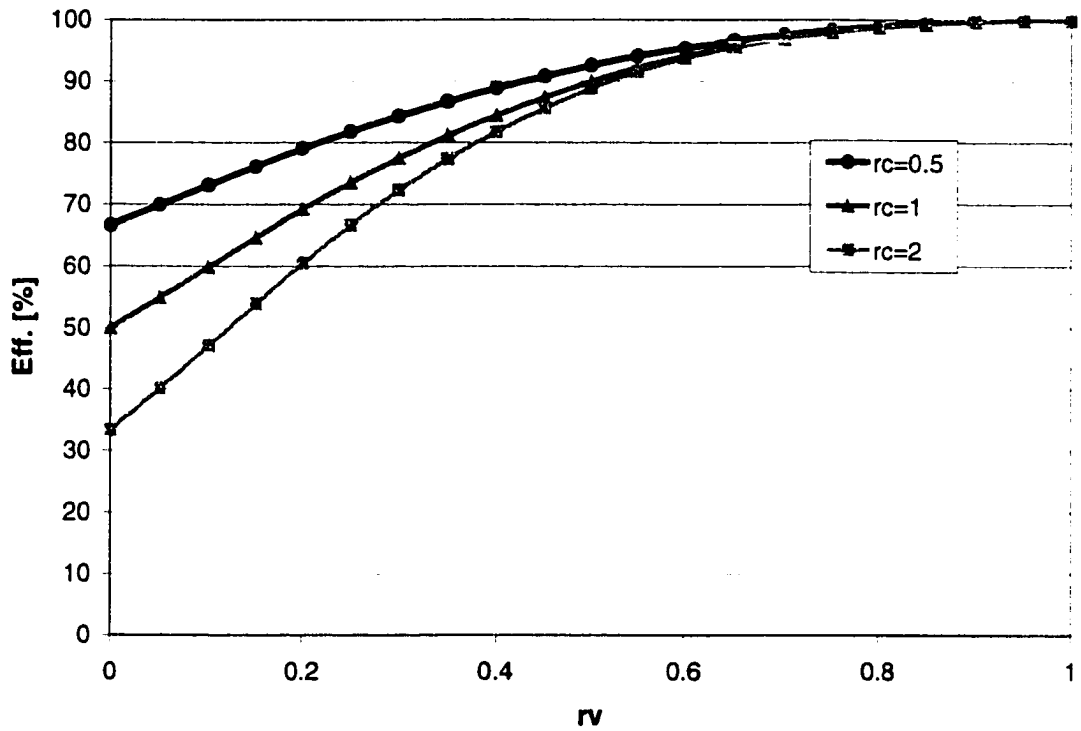

Fig. 3.8 Energy transfer efficiency as a function of r_V.

In Fig. 3.8, three graphs representing the energy transfer efficiency as a function of r_V are displayed. They are for r_C =0.5, 1 and 2. The efficiency approaches 100% for all cases when r_V is close to unity. It can also be seen that transfer efficiency is higher for smaller values of rc. Which means that C2 should be smaller than C1. But, in most practical cases, C2 is the load capacitor and C1 is the charge or "pump" capacitor, and the load capacitor is made larger to reduce the ripple effect.

Next we examine the power lost in a switched capacitor that is connected to ground. But before we derive the formula for that configuration, we will look at a simplified case. Fig. 3.9 shows a schematic where current leaks through a branch connected between VDD and ground. The power dissipated through that branch is given by:

$$P = I_D \cdot V_{DD} \tag{3.41}$$

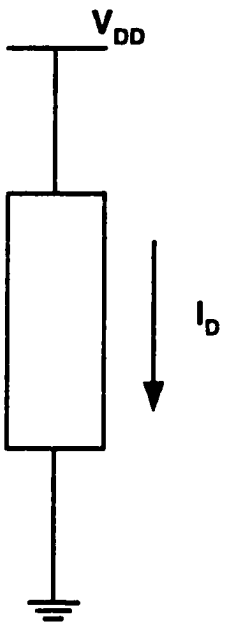

Fig. 3.9 Schematic showing the current leaking through a branch connected to ground.

The current flowing through the capacitor connected to ground is considered a leakage current and is lost. The path to ground is considered a dynamic path rather than a static path. In static paths the current has a constant value over time and the connection is established at all times. Fig. 3.10 shows a dynamic path configuration, where Φ_1 and Φ_2 are non-overlapping clocks as shown in Fig. 3.11, each of these clocks have a period of

T. The non-overlapping clocks make sure that there is no direct continuous path to ground. If such a condition exists, a infinitely large current flows between the supply and the ground. That is assuming that the supply has zero output impedance.

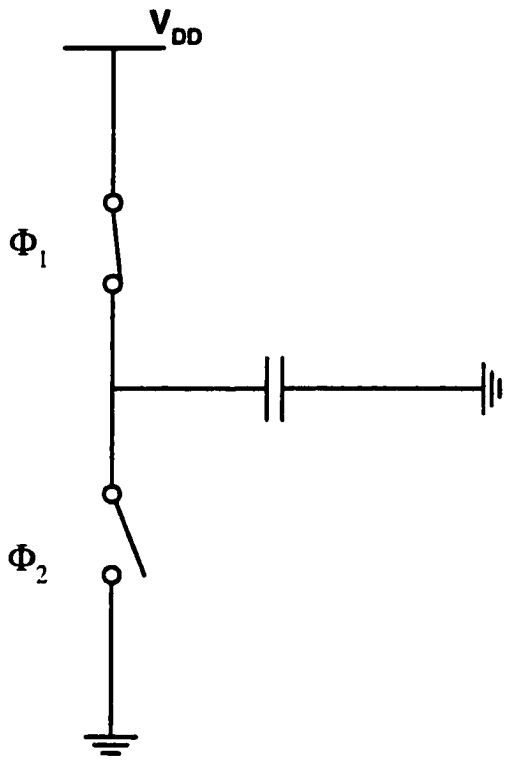

Fig. 3.10 Switched capacitor connected to ground.

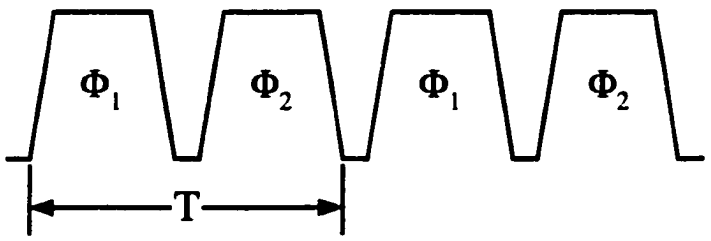

Fig. 3.11 Diagram showing the non-overlapping clocks.

The equivalent impedance of the capacitor is given by Eq. (3.19). and is repeated here:

$$R_{eq} = \frac{T}{C} = \frac{1}{FC} \tag{3.42}$$

and the leakage current is given by

$$I_D = \frac{V_{DD}}{R_{eq}} = FCV_{DD} \tag{3.43}$$

The power dissipated through the capacitor

$$P = FCV_{DD}^{2} \tag{3.44}$$

3.6 Results

The circuit fabricated is shown in Fig. 3.12, it is about 700um on a side. The large MESFET's are the output ones. Two V_{gen} bond pads are used to accommodate bonding arrangements for different applications. This circuit is used in different products, and millions have been produced. Several design and layout revisions were made to optimize the performance and reliability.

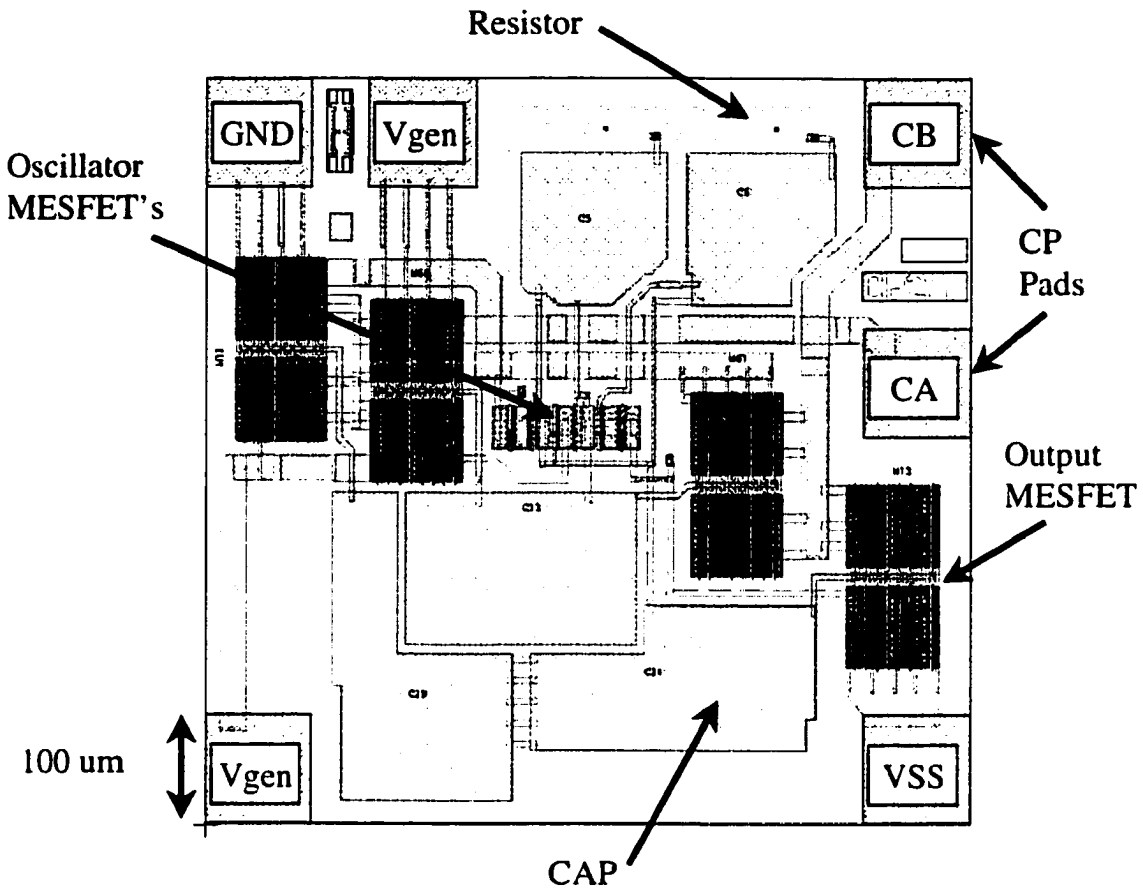

Fig. 3.12 Die microphotograph.

Fig. 3.13 shows the output voltage vs. output current. The circuit supplies a load current up to 40mA and runs off a supply voltage that ranges between 2V and 10V. At no load, the output voltage is close in magnitude to the supply voltage as seen in Fig. 3.13. The open circuit voltage conversion efficiency is higher than 99% for most of the operating supply range as shown in Fig. 3.14. It drops at the low end because the oscillator does not generate enough voltage swing to prevent the overlap condition explained earlier. At the higher end, the efficiency drops, because the voltage levels in the circuit approach the breakdown regions of the MESFET's.

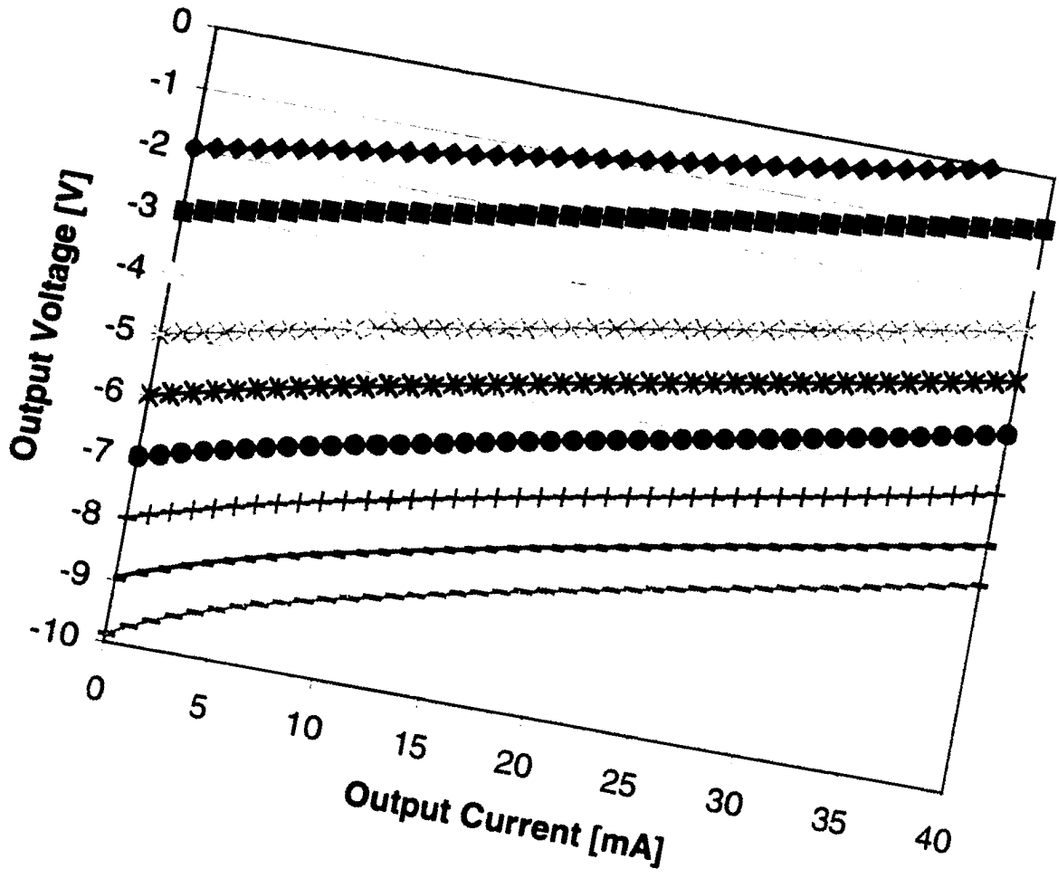

Fig. 3.13 Output Voltage vs. Output Current, Vgen = 2V to 10V.

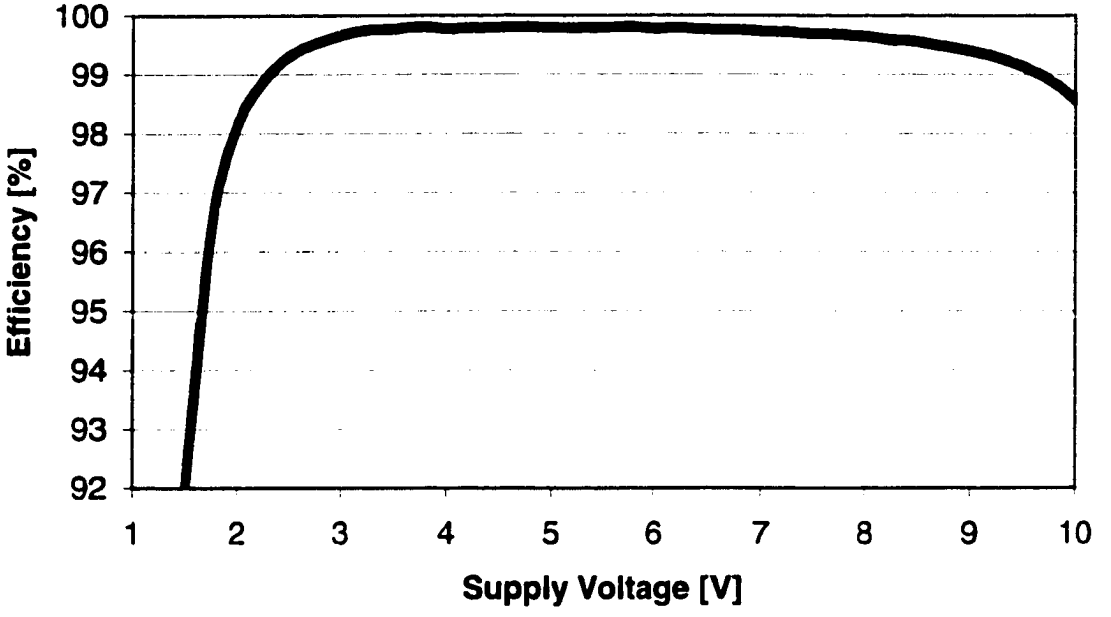

Fig. 3.14 Open Circuit Voltage Conversion Efficiency vs. Supply Voltage.

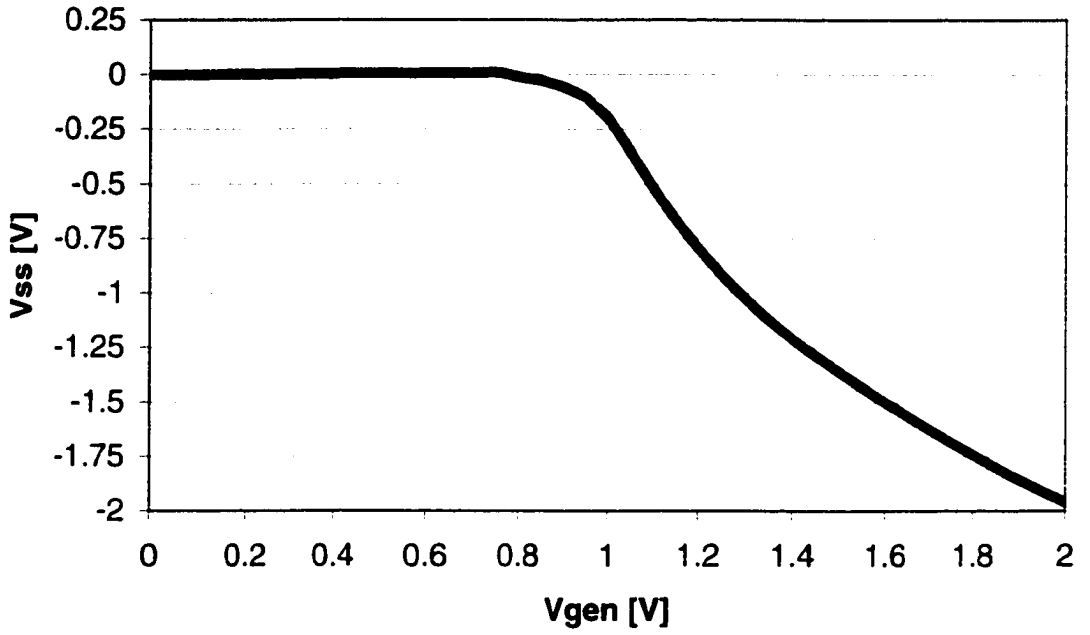

Fig. 3.15 Output Voltage vs. Supply Voltage, Iss=0mA.

Fig. 3.15 shows where the circuit starts to function as a converter, and that is at about 1V. Yet both, open circuit voltage conversion efficiency Fig. 3.14 and power conversion efficiency

Fig. 3.16 Power Conversion Efficiency, Vgen = 5V. are low below 2V. Among the factors affecting the power conversion efficiency are; power consumed by the oscillator, power dissipated by the output MESFET's (M5, M6, M7 and M8) and the Ohmic losses in the resistors.

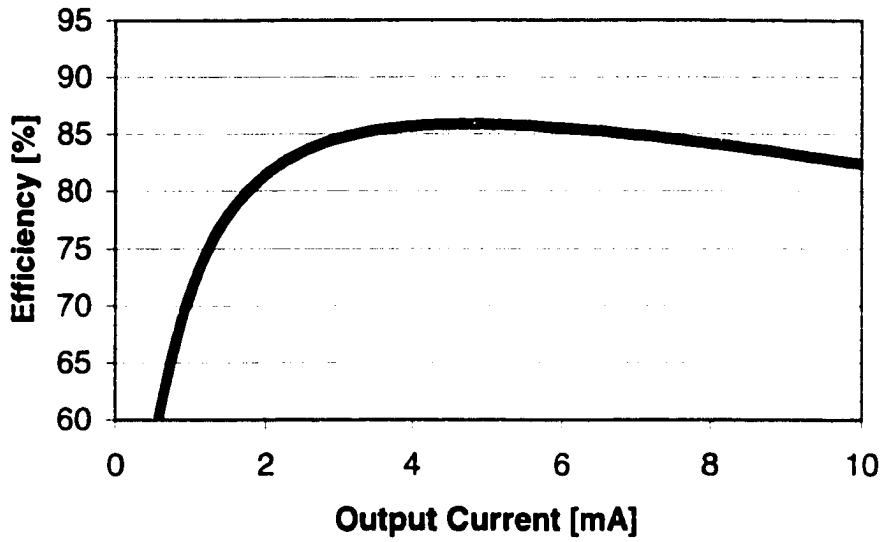

Fig. 3.16 Power Conversion Efficiency, Vgen = 5V.

Output resistance vs. supply voltage is shown in Fig. 3.17, the graph shows that the output resistance decreases as the supply voltage decreases, that is because the oscillating frequency is increasing, and as shown in Eq. (3.24) the output resistance decreases. Fig. 3.18 shows that the output resistance has less dependence on the load current.

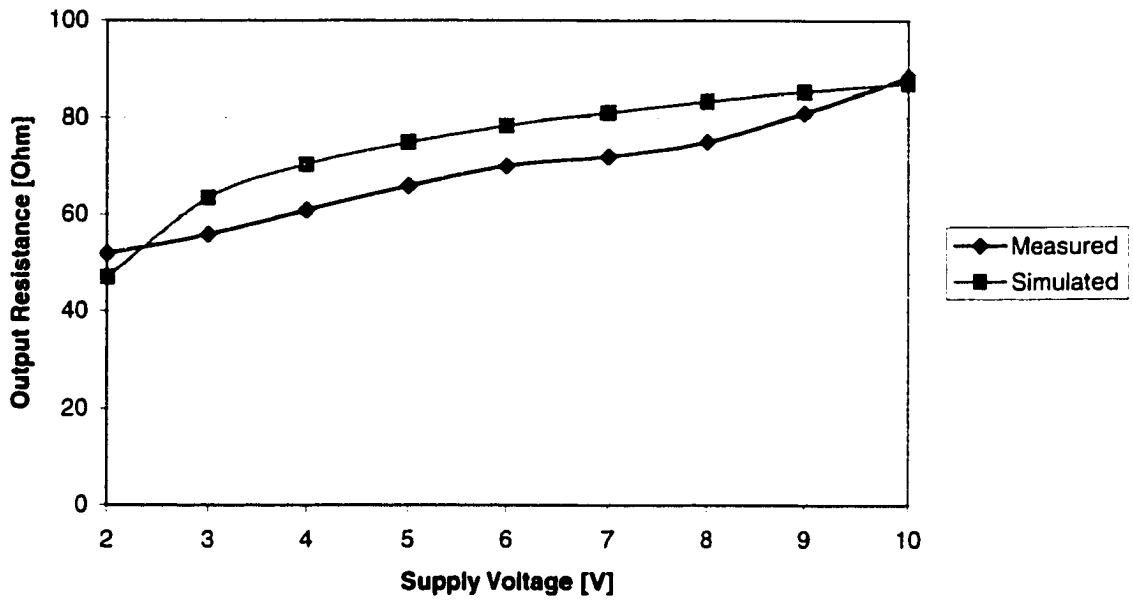

Fig. 3.17 Output Resistance vs. Supply Voltage, Iss = 10 mA.

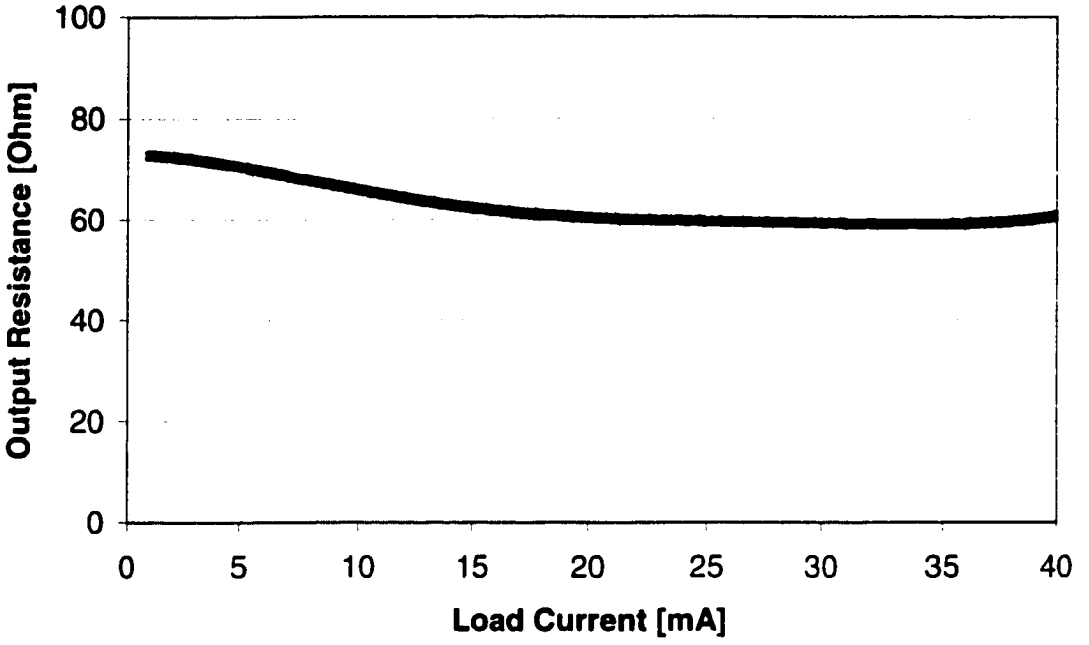

Fig. 3.18 Output Resistance vs. Load Current, Vgen = 5V.

3.7 Start-up Current

This circuit is built with depletion mode MESFET's which are devices that are normally ON. This causes a problem at startup where no negative voltage is available in the circuit. All the MESFET's are fully ON and a low impedance path is created between ground and both the supply voltage and the output voltage. When the circuit is running at steady state and at no load, it draws less than 1mA, but at startup it can draw up to 200mA. M1, M2, M3 and M4 are small width, long gate MESFET's to reduce startup

current and the current consumed under normal operation. M5, M6, M7 and M8 must be made with large width, short gate length MESFET's to get low output resistance. This results in large startup currents. Fig. 3.19 shows simulation results of supply current at startup. As the negative voltage is established, the magnitude of the current pulses decreases.

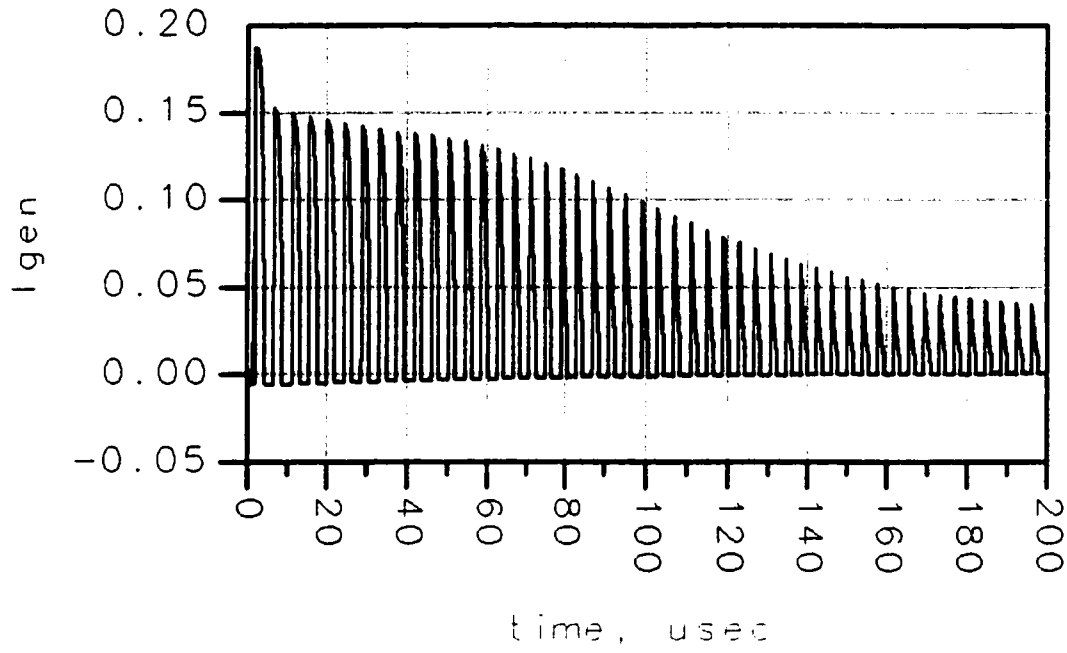

Fig. 3.19 Simulation of startup current.

In most portable applications, the DC to DC converter is shut down in standby mode, and since this circuit does not have a shut down feature, an external switch is needed. That switch has to be able to handle the startup current of 200mA and still provide a minimum of 1V to the circuit for the oscillator to start up. The maximum ON resistance of the external switch is calculated as follows:

$$R_{ext} = \frac{V_{gen} - 1V}{200mA} \tag{3.45}$$

For a 5V supply, R_{ext} should be no larger than 20Ω, a factor of safety should be added to allow for process or temperature variations.

3.8 Reliability

High start up currents can lead to reliability problems. Interconnects in integrated circuits have a certain current carrying capability. Fig. 3.20 shows the layout of the converter at an early phase in the design process, the circuit uses two levels of interconnects, metal1 (m1) and metal2(m2) with a current carrying capability of 7ma/μm and 25 ma/μm respectively. Where (μm) refers to the metal trace width. The interconnects where not wide enough. The circuit had reliability problems, where some of the traces would burn up. That results from large currents flowing through under-designed interconnects.

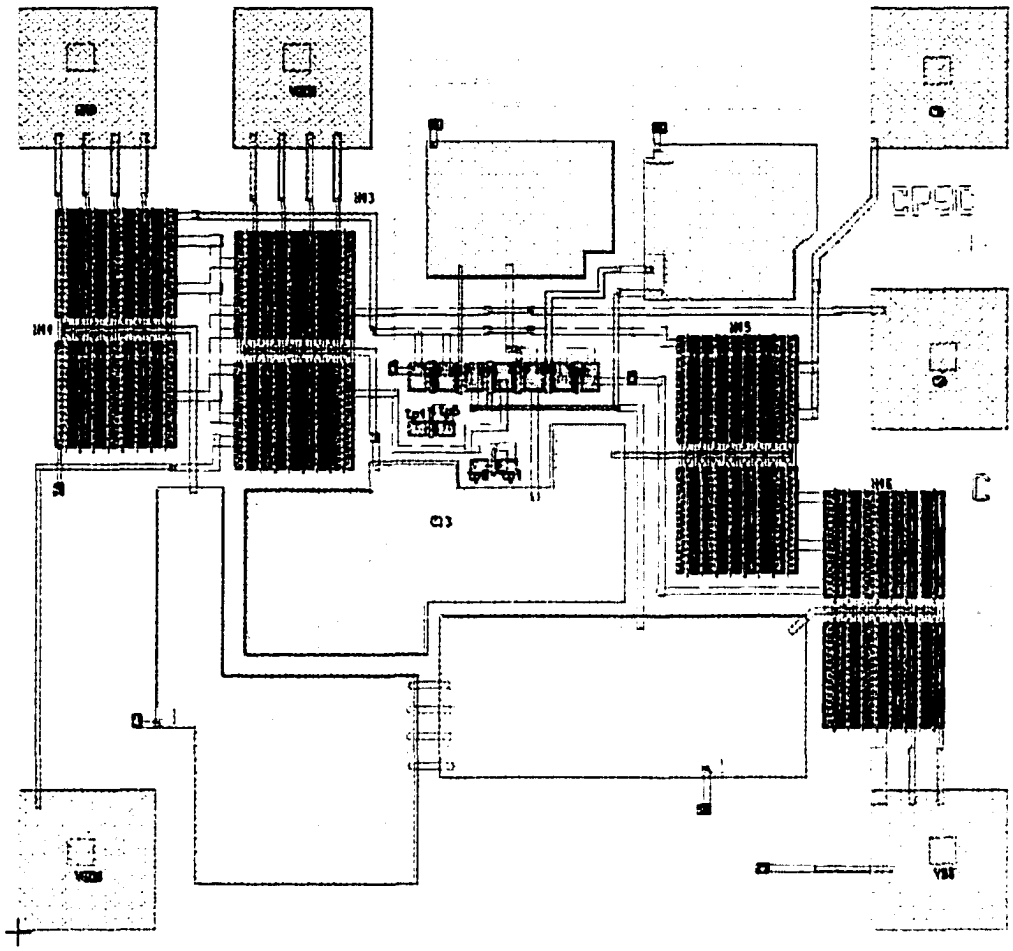

Fig. 3.20 Die microphotograph of an earlier layout.

The startup current of about 200mA flows through the trace shown in Fig. 3.21, that trace is marginally under-designed, and some units failed. They all would fail at the point shown in Fig. 3.21. That is where m1 and m2 are connected through a via, and it acts as a bottleneck for the current flow.

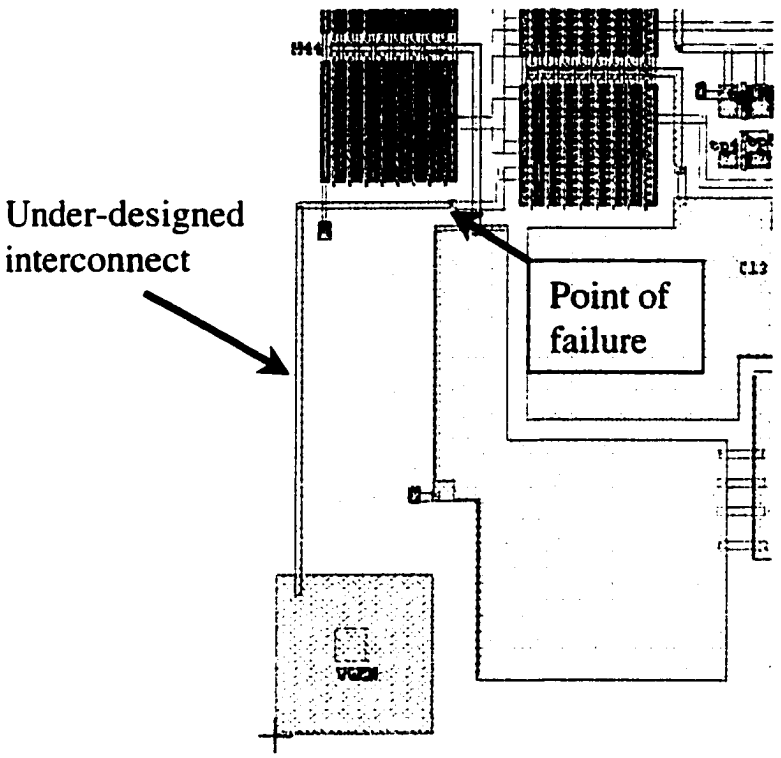

Fig. 3.21 Trace in the layout where the circuit failed.

To alleviate this problem, the layout was re-designed such that the currents can flow without allowing the Ohmic losses to heat up traces and melt them. The new layout shown in Fig. 3.22 and repeated here from section 3.6 for illustration, proved to be resistant to such failure mechanism.

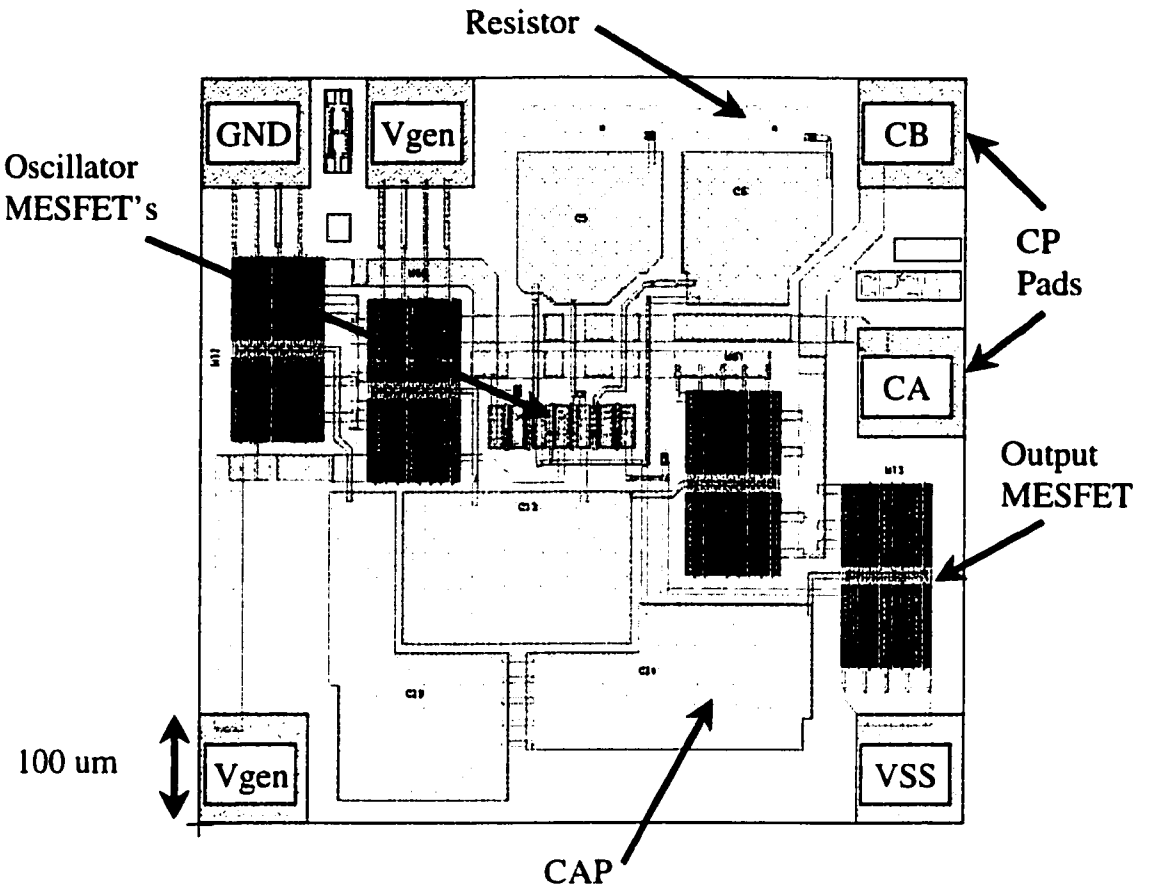

Fig. 3.22 Die layout with wider interconnects.

4 CHAPTER IV

Microwave DC/DC Converter

4.1 Introduction

In this chapter, a new DC/DC converter design is introduced. The specs are derived from the performance specs of the switched capacitor DC/DC converter.

The switched capacitor converter introduced in chapter 3 has some advantages and disadvantages. Among the advantages is the high power conversion efficiency (Fig. 3.16) which is in the upper eighties for most of the operating range. The switching losses are reasonable, due to the fact that the switching frequency is not high enough to cause the switching losses to be larger than the transferred power.

Next, we will discuss the disadvantages or shortcomings of the switched capacitor converter running at 250 kHz.

4.1.1 Size

The circuit that was measured in the previous chapter had a die size of about $0.5mm^2$. Three external capacitors are used, one for line filtering of 1 μF, another for the pump capacitor of 0.1 μF, and a third of 1 μF for the hold capacitor at the output. Ceramic capacitors are used over electrolytic or Tantalums because they have a higher resonance frequency and they are not polarized. Polarized capacitors tend to have larger ESR values at higher frequencies due to the rapid flow of pulsating current, that is impeded by

the chemical bonds that are formed and take time to break and form in the other direction. Ceramic capacitors do not have that problem.

To select reliable ceramic chip capacitors that have a good tolerances over temperature, 10% or less from –30 to +85 degrees Celsius, and have a voltage rating that is higher than 15 V. Case sizes of 0603 and 0805 for the of 0.1 μF of 1 μF respectively are used. 0603 footprints occupy a space of 1.16 mm^2. While 0805 footprints occupy a space of 2.58mm^2. Assuming no space is wasted for the interconnects between the die and the capacitors, a total area of 6.8 mm^2 is needed for the switched capacitor DC/DC converter. While this solution is small considering the converters that run at frequencies below 100 kHz or those that use external inductors, it is still large especially in portable equipment or hand-held devices in particular.

4.1.2 Noise

There are two issues related to the noise performance of this converter. First is the level of signals. The input current pulses and the output voltage ripple is large. And they also have a lot of harmonics due to the non-linear nature of the waveforms. Second , is the frequency allocation of the oscillator frequency. All switching converters act as noise sources in the systems they are used in. In this case, the converter acts as a noise source at 250 kHz and its harmonic frequencies. If the converter is being used in a narrow band system like a cellular system, where one example could be a channel width of 30 kHz in the 900MHz range, the 250 kHz signal can be filtered out and the system can be designed with immunity to the interfering signals. On the other hand, if the converter is being used in a broadband system, where the signals of interest range from DC or close to it, to

above 1GHz, then it becomes very difficult to use any converter that runs at frequencies below 1GHz. It is difficult to filter out an in-band noise source. One such broadband system is the fiber optic system, where the transmitted digital pulses occupy the spectrum from DC to 1GHz, or higher depending on the system architecture. GaAs transimpedance amplifiers are widely used in such systems due to their high sensitivity and wide bandwidth. A negative voltage is often needed for these circuits, and the negative source has to have extremely low ripple values. That is a major challenge. Transimpedance amplifiers follow a photodetector that converts an optical signal into an electrical signal. The electrical signal levels are usually very low, and a small interfering noise signal, can overwhelm the original signal.

4.1.3 Low Voltage Operation

The switch capacitor topology will convert an input voltage to an output voltage of the same or inverted polarity, but the magnitude of the output signal is always lower than the input signal. That is if no cascading or additional boost stages are used. This limits the output voltage to values that are less than the supply voltage. Under load, the output voltage drops even further below the input voltage level.

The trend for the hand-held devices, is to operate at lower battery voltage, that is to maximize the operating time by reducing the power dissipation. The switching losses decrease with decreasing supply voltage, and the switching speed increases at the same time. That trend puts a burden on the power supply circuits, that have to run off lower supply voltages, yet still deliver output voltages that are comparable or higher than the input voltages. Since the switch capacitor converter produces an output voltage that is

smaller in magnitude than the input voltage, it is not a good candidate for low voltage applications.

4.1.4 Process Requirements

The GaAs implementation of the switched capacitor circuit shown in Fig. 3.1, uses two different device sizes. Long-gate length (4 μm) MESFET's are used for the oscillator section; M1, M2, M3 and M4. And standard gate length (0.5 μm) MESFET's for the switching section; M5, M6, M7 and M8. The long-gate MESFET's dissipates little power to keep the overall efficiency high. Yet the switching MESFET's are high current device to ensure small ON resistance.

The fact that we have two different device sizes on the same circuit produces a problem during manufacturing. One type of active devices is usually monitored during manufacturing to ensure the process is within the specification. In this case, the standard (0.5 μm) MESFET's are monitored. And the long-gate device are left unmonitored. The process is centered around the nominal devices, and the non-standard device usually end up with a large variation in their electrical characteristics, since these values are not used in a closed loop during manufacturing. That results in circuits that have lower yields.

4.2 Design Approach

The design challenge in this case, is to design an efficient DC/DC converter, such that it small in size, has low noise contribution, runs at low voltages and can be fabricated with high yield. All that has to be done in a depletion mode MESFET technology.

Increasing the switching frequency allows us to use smaller active and passive components. Since "current" is the charge transferred in unit time, smaller charges can be transferred at higher frequencies to yield the same current. But, designing a converter at high frequency causes the converter to have higher switching losses and thus reducing the overall power conversion efficiency.

As for the noise contribution, one possible solution is to design the oscillator to run at frequencies that are outside the communications band of interest. And in the case of 1GHz broadband circuits, the oscillator frequency has to be at least at 4GHz or higher for good noise immunity. Again, operating at such high frequencies causes the converter to be inefficient due to high switching losses.

Switch capacitor topology is not a good candidate for low voltage operation, yet the boost topology is. So, the circuit to be designed should take advantage of the boost mechanism if it were to produce an output voltage that is higher in magnitude than the supply voltage.

Since different device types on the same chip causes the manufacturing yield to drop, the new circuit should include a small mix of device types.

The main challenge is accomplish all of the above while maintaining high power conversion efficiency.

Fig. 4.1 shows a generic block diagram of a switching DC/DC converter. An AC voltage is generated from a DC voltage, the AC voltage is then rectified to generate a negative or

positive DC voltage. In this chapter, we are going to design a converter with an oscillator that runs at frequencies that range from 4 GHz to 10 GHz.

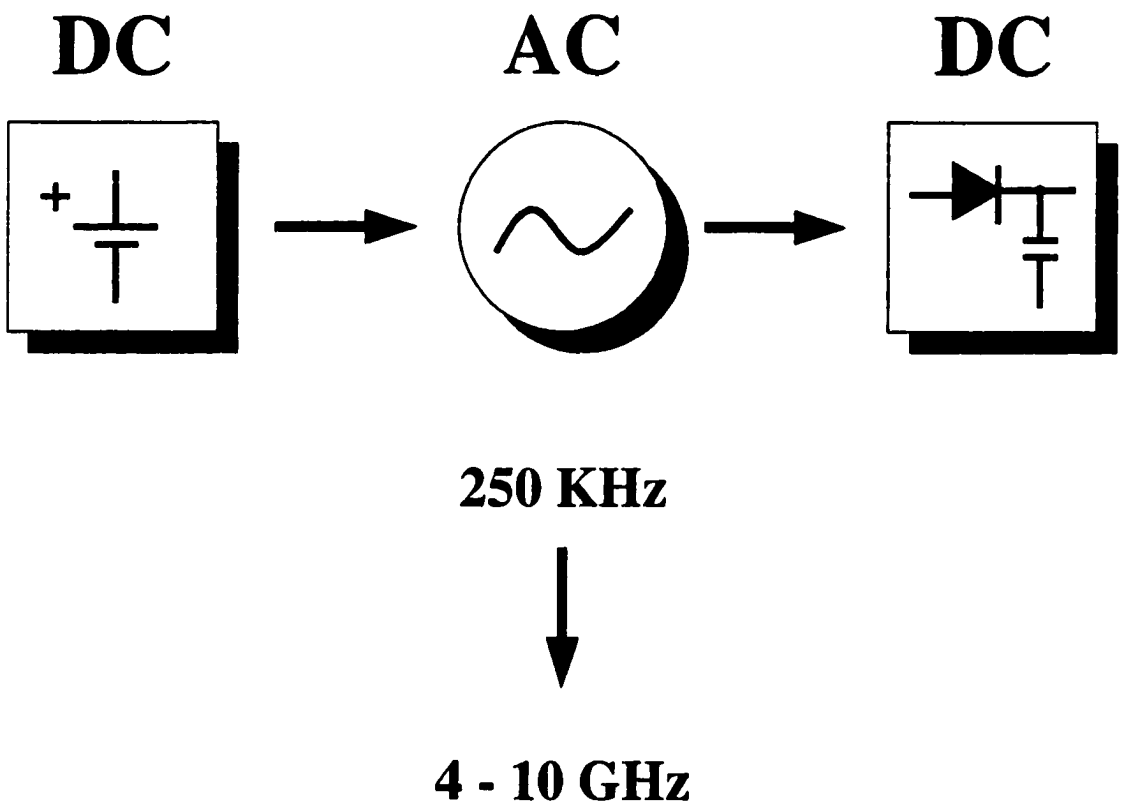

Fig. 4.1 Generic block diagram of a switching DC/DC converter.

The oscillator section in the GaAs switched capacitor converter is shown in Fig. 4.2, the oscillator frequency is set by the RC constants as described in chapter 2. This is a differential design, and it has strong startup characteristics, as compared to a single ended oscillator. It also provides two signals that are 180° out of phase to control the rectifier section. We are going to continue to use this topology for the higher frequency oscillator.

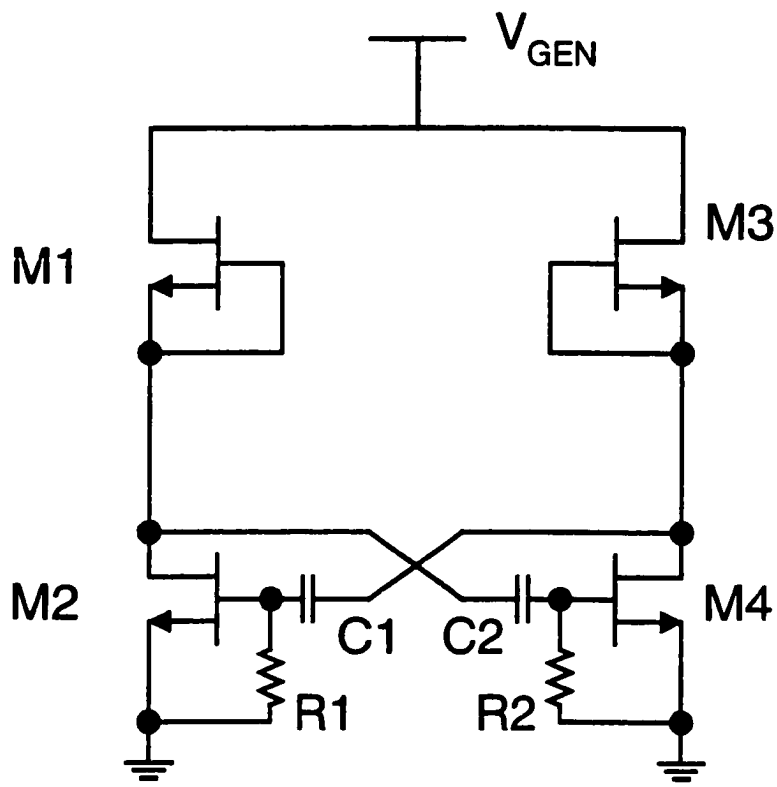

Fig. 4.2 Oscillator section of the switched capacitor converter.

In order to reduce the power dissipated in the oscillator, we need to reduce the number of active components and resistors where possible. We can replace the active loads with inductors, and remove the resistors. By doing so, we get the schematic shown in Fig. 4.3.

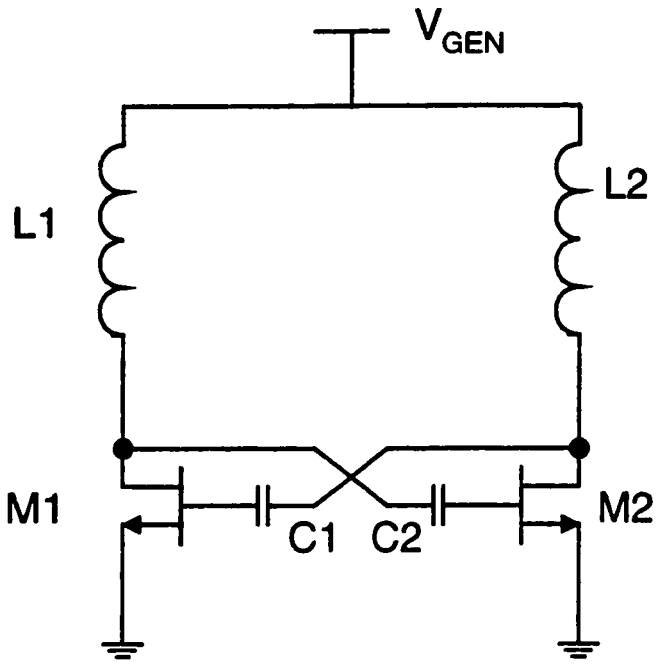

Fig. 4.3 Efficient, high frequency, differential oscillator.

The oscillator frequency is governed by the inductors L1 and L2, capacitors C1 and C2 and the gate-source and drain-source capacitances of M1 and M2.

Fig. 4.4 shows the drain voltage waveform of M1 in Fig. 4.3, while Fig. 4.5 shows the drain voltage waveform of M2. These are generated with the following values; L1 = L2 = 2 nH. C1 = C2 = 4pF. M1 and M2 are MESFET's where each has two (100 μm) gate fingers. The supply voltage is 3V.

The two waveforms are 180° out of phase. Each waveform has a DC average of 3V. If the waveform is a pure sinusoidal signal, the peak would approach 6V, which is twice the

supply voltage. The bottom of the waveform approaches the ground voltage when the MESFET is turned on.

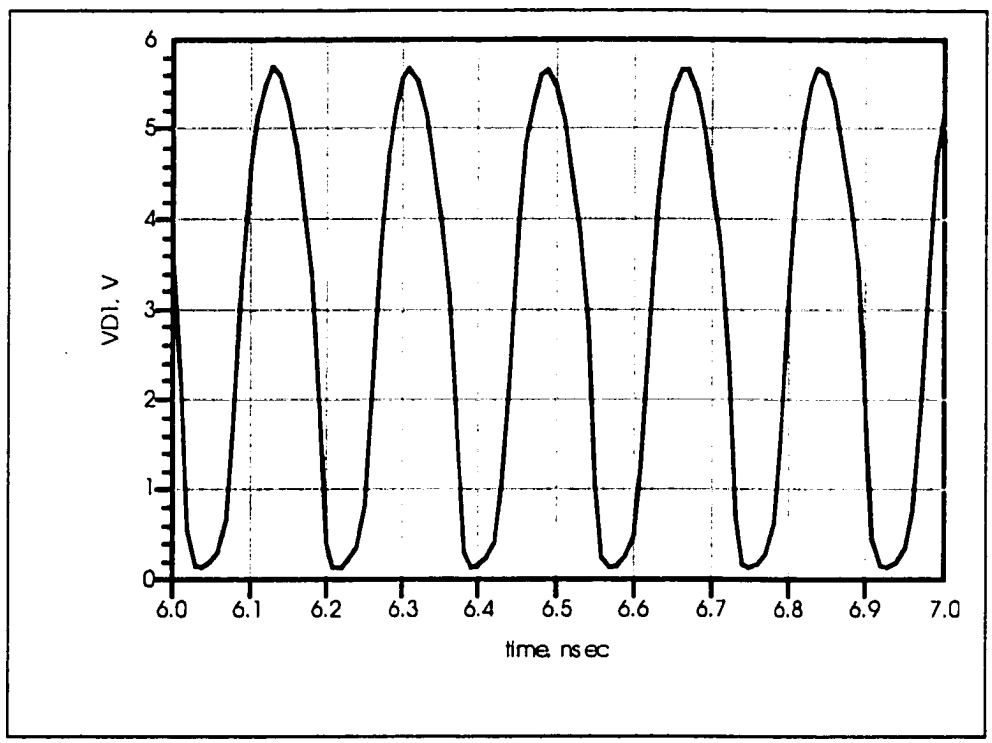

Fig. 4.4 Drain voltage waveform of M1.

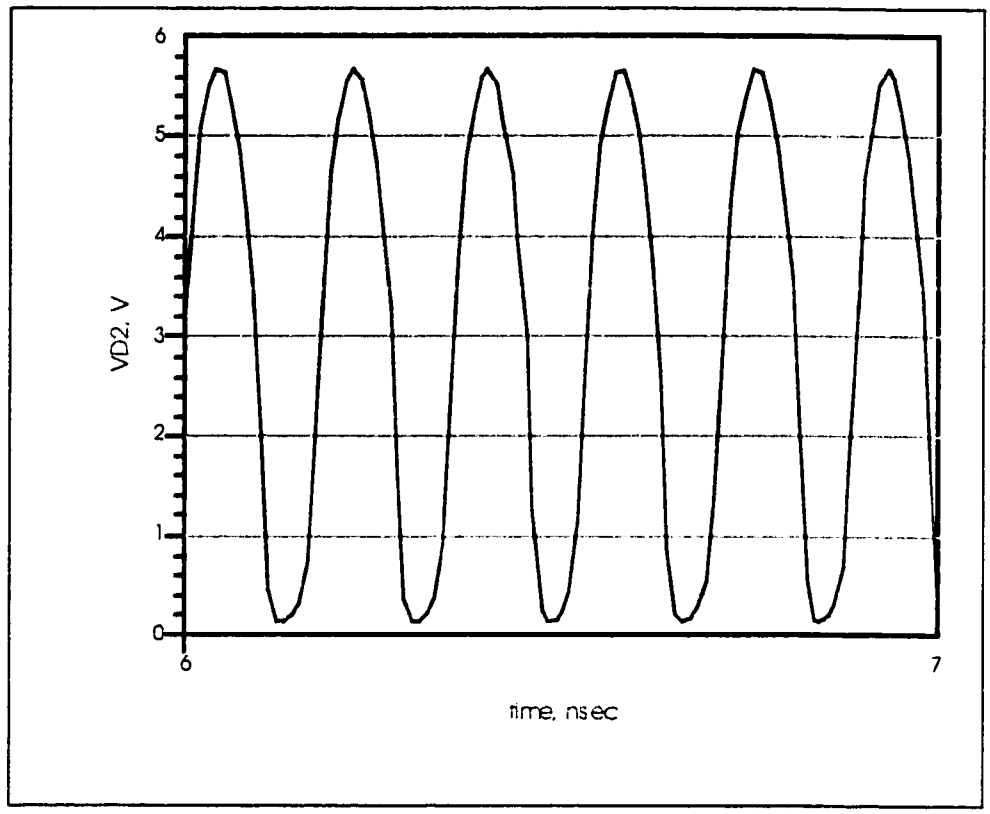

Fig. 4.5 Drain voltage waveform of M2.

The spectrum of the drain voltage waveform is shown in Fig. 4.6. The oscillator frequency is about 5.7 GHz. The frequency changes slightly with temperature and with process variations.

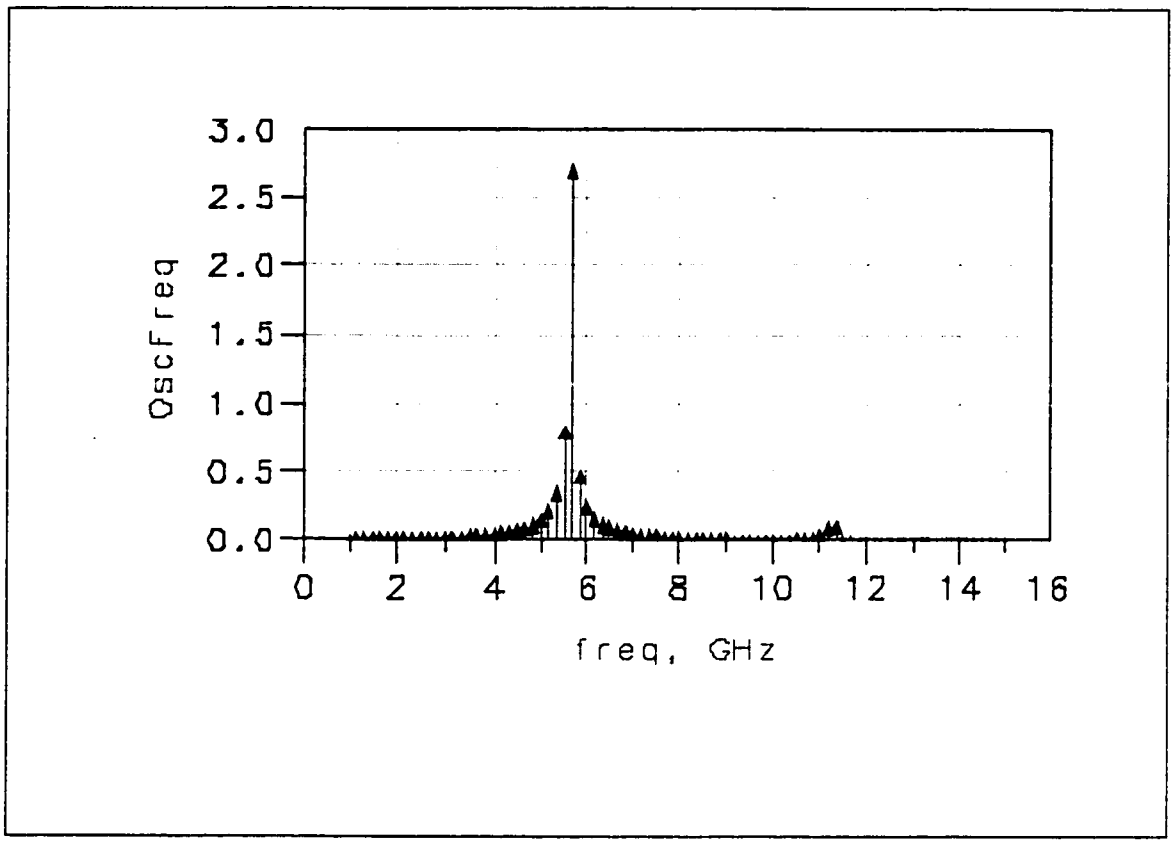

Fig. 4.6 Spectrum of the drain voltage waveform, VD1.

One major difference between the oscillator used in the switched capacitor circuit in Fig. 3.1, and the one in Fig. 4.3, is the drain voltage swing. The maximum swing in the former does not exceed the supply voltage, yet the swing in the latter is close to twice the supply voltage. Instead of using this large voltage swing to drive the gates of the MESFET's in the rectifier section, we are going to rectify this voltage swing itself to obtain a larger output voltage. In this case, the oscillator has to be strong enough to supply the load. In Fig. 3.1, the oscillator section delivered enough power to power the gates of the MESFET's in the rectifier circuit. In this case, the oscillator has to deliver enough power to support the load current.

Fig. 4.7 shows a rectifier circuit added to the microwave oscillator. The circuit has two sections, one operating at each end of the oscillator, this enables to the circuit to deliver higher current and enhances the power conversion efficiency.

The coupling capacitor C5 ensures that the AC voltage swing is delivered to the anode of D3, the diode in return clamps the voltage wing above 0.7V, forcing the lower peak to go negative. The boundary condition at the drain is that the lower peak is clamped to ground, and the new boundary condition at the diode, is that the upper peak is clamped at one diode drop above ground. This is shown in Fig. 4.8.

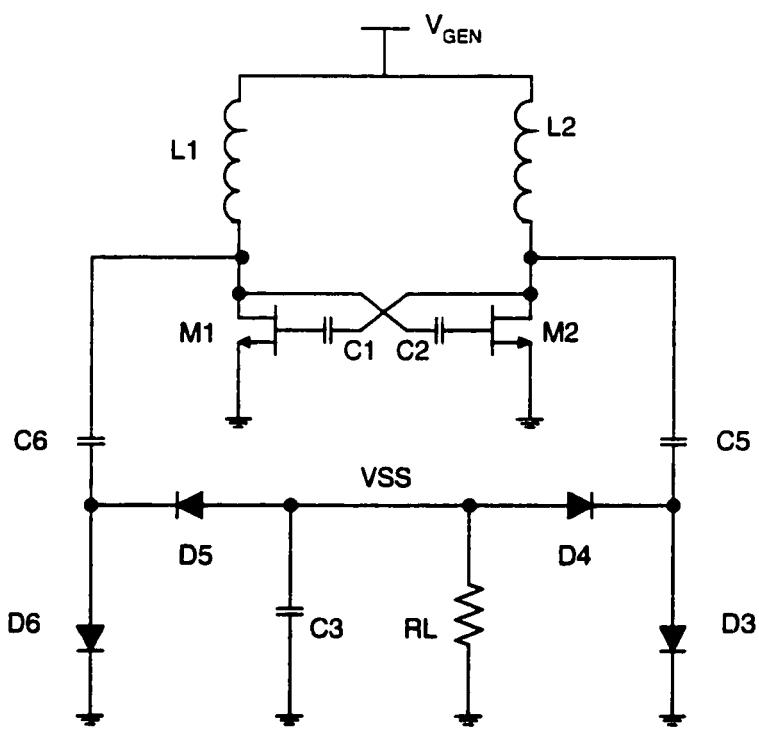

Fig. 4.7 Microwave oscillator with a dual rectifier circuit.

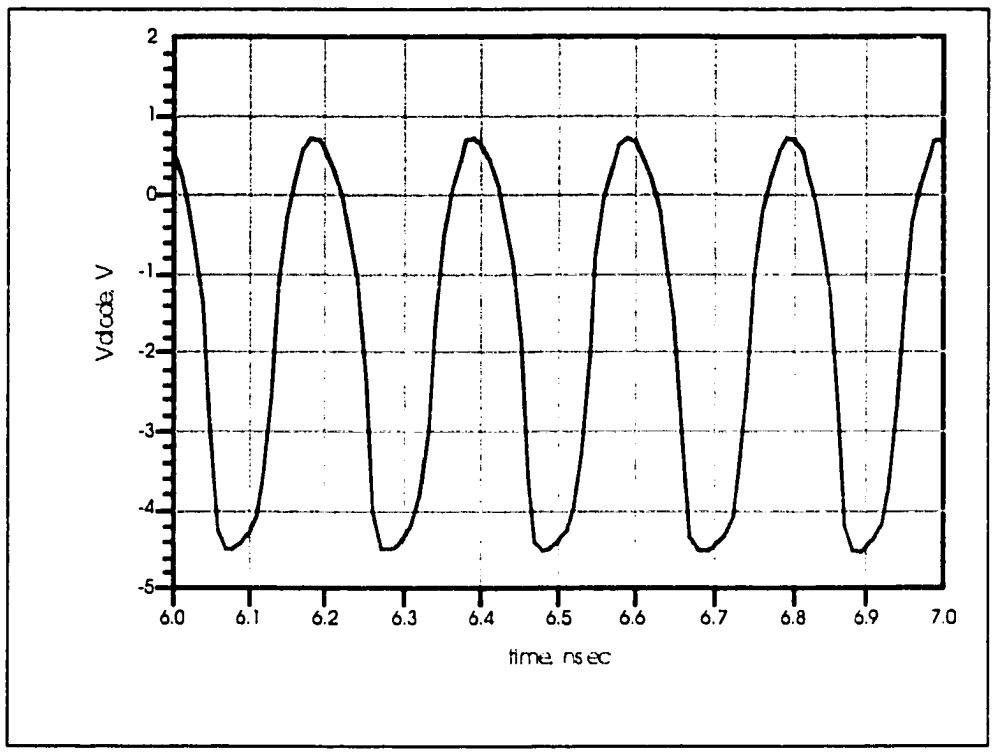

Fig. 4.8 Anode voltage of D3.

D4, D5 and C3 act as a negative peak detector, and generate the negative voltage VSS.

Removing resistors from the circuit and replacing the active loads with inductors, reduces the power dissipation. To further improve the efficiency of this circuit, we look for ways to reduce the number of components, while maintaining the functionality. Close examination of Fig. 4.7, and substituting the MESFET model shown in Fig. 1.4, reveals an interesting symmetry. The drain of M2 is connected to C5, which is connected to D3 that is connected to ground. But, the drain of M2 is also connected to C1, which is

connected to ground through the parasitic diode of M1 (Fig. 4.9). That means, the waveform at the anode of D3 is similar to that at the gate of M1 (Fig. 4.10).

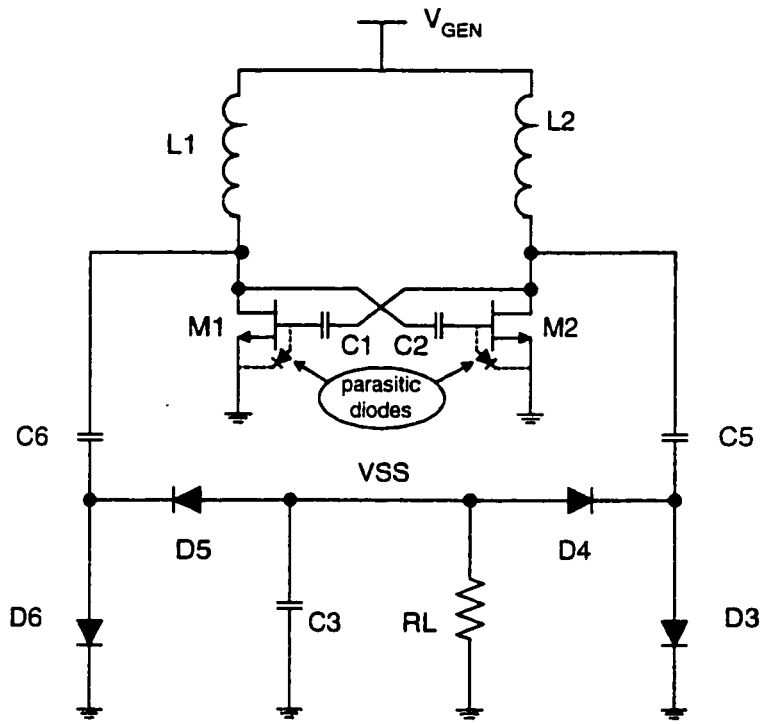

Fig. 4.9 Gate-source parasitic diodes.

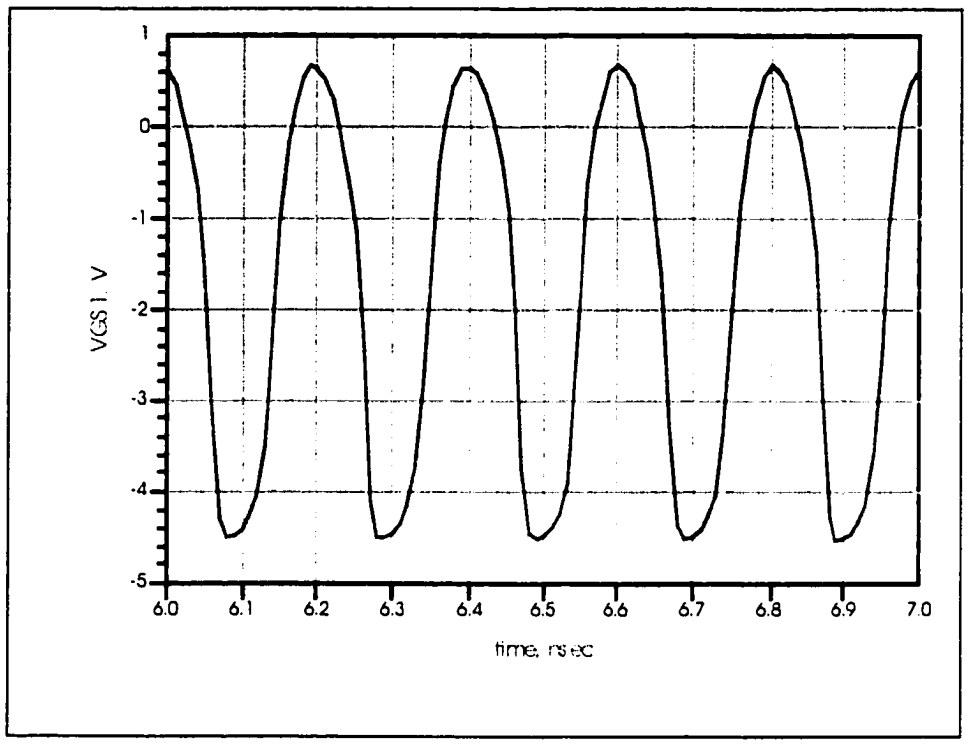

Fig. 4.10 Gate-source voltage of M1.

Fig. 4.11 shows the reduced component count microwave DC/DC converter. C1, C2 and the gate-source parasitic diodes of M1 and M2 replace C5, C6, D3 and D6. Fig. 4.12 shows the output voltage at no load VSS.

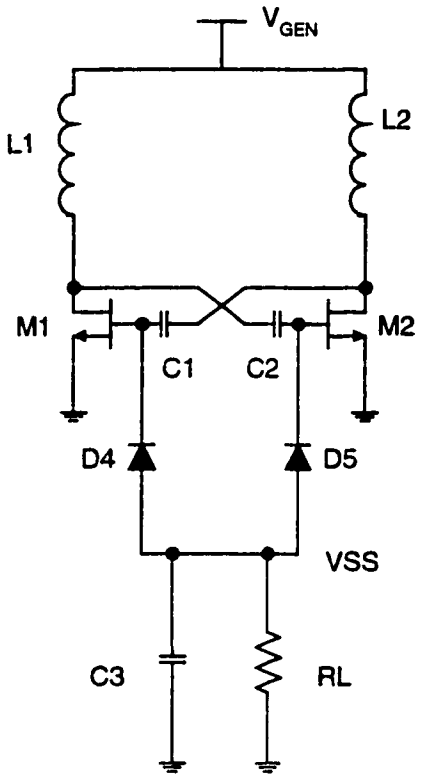

Fig. 4.11 Reduced component count MWDCDC converter.

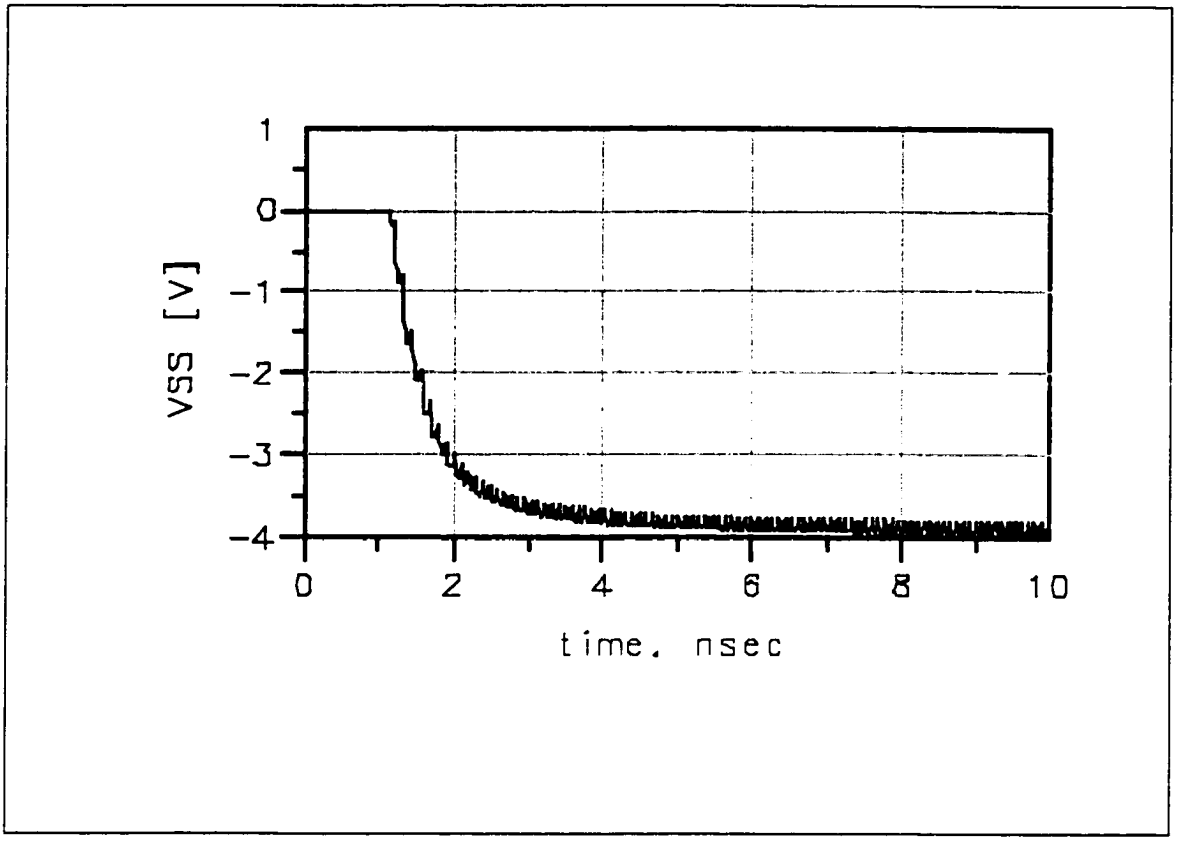

Fig. 4.12 Output voltage of the MWDCDC converter, VSS.

4.3 Results

The circuit was built with different inductor sizes and in different processes. Fig. 4.13, Fig. 4.14 and Fig. 4.15 show the output voltage vs. the output current for different inductor sizes. Each graph shows the output voltage for a range of supply voltages [2V-6V]. The oscillator frequency changes slightly with load current and supply voltage, but for the circuits measured, it is about 4GHz when 4nH inductors are used for L1 and L2. It is about 6GHz when 2nH are used and finally it is about 9GHz for 1nH inductors. Circuits with larger inductors can support higher load currents as seen in the three graphs. The no-load output voltage is higher in magnitude than the supple voltage. The output impedance ranges from about 300Ω to about 600Ω, depending on the supply voltage and the size of the passive and active components used. The circuit can be resized for higher or lower output impedance, but the lower the output impedance, the larger the devices used, and hence the lower the oscillator frequency. The power conversion efficiency peaks up at 30% to 40% for optimized circuits with known loads.

Fig. 4.16, Fig. 4.17 and Fig. 4.18 show the die layout for the circuits measured. VB1 and VB2 are two test points connected to the gates of M1 and M2 through a resistor. These points were left unconnected when performing the measurements. Multiple ground and supply bond pads are used to reduce the bond wire inductance. An on-chip line capacitor is connected between supply and ground to provide a path for the AC currents.

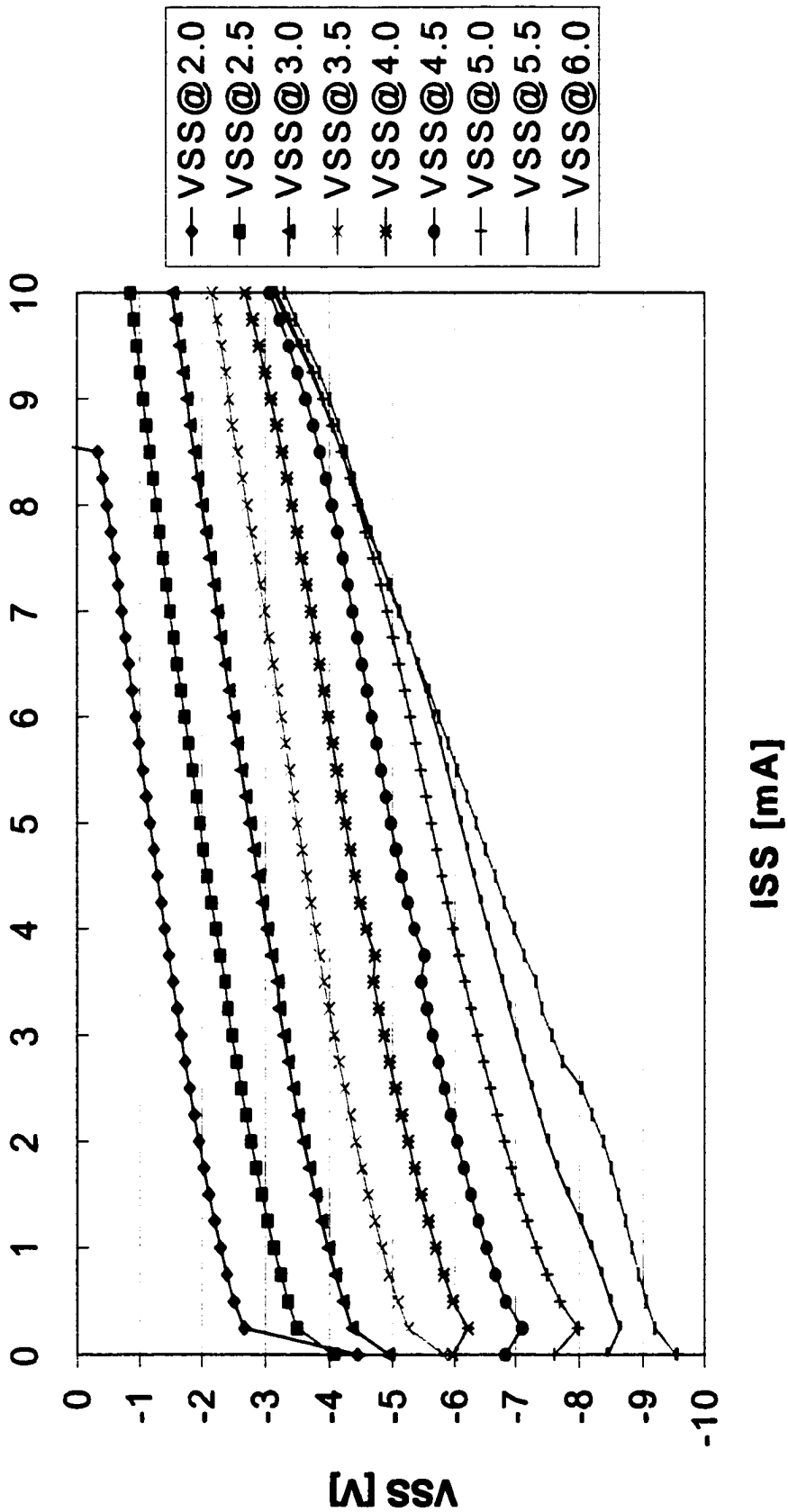

Fig. 4.13 VSS vs. ISS for L = 4nH, F_{osc} = 4GHz.

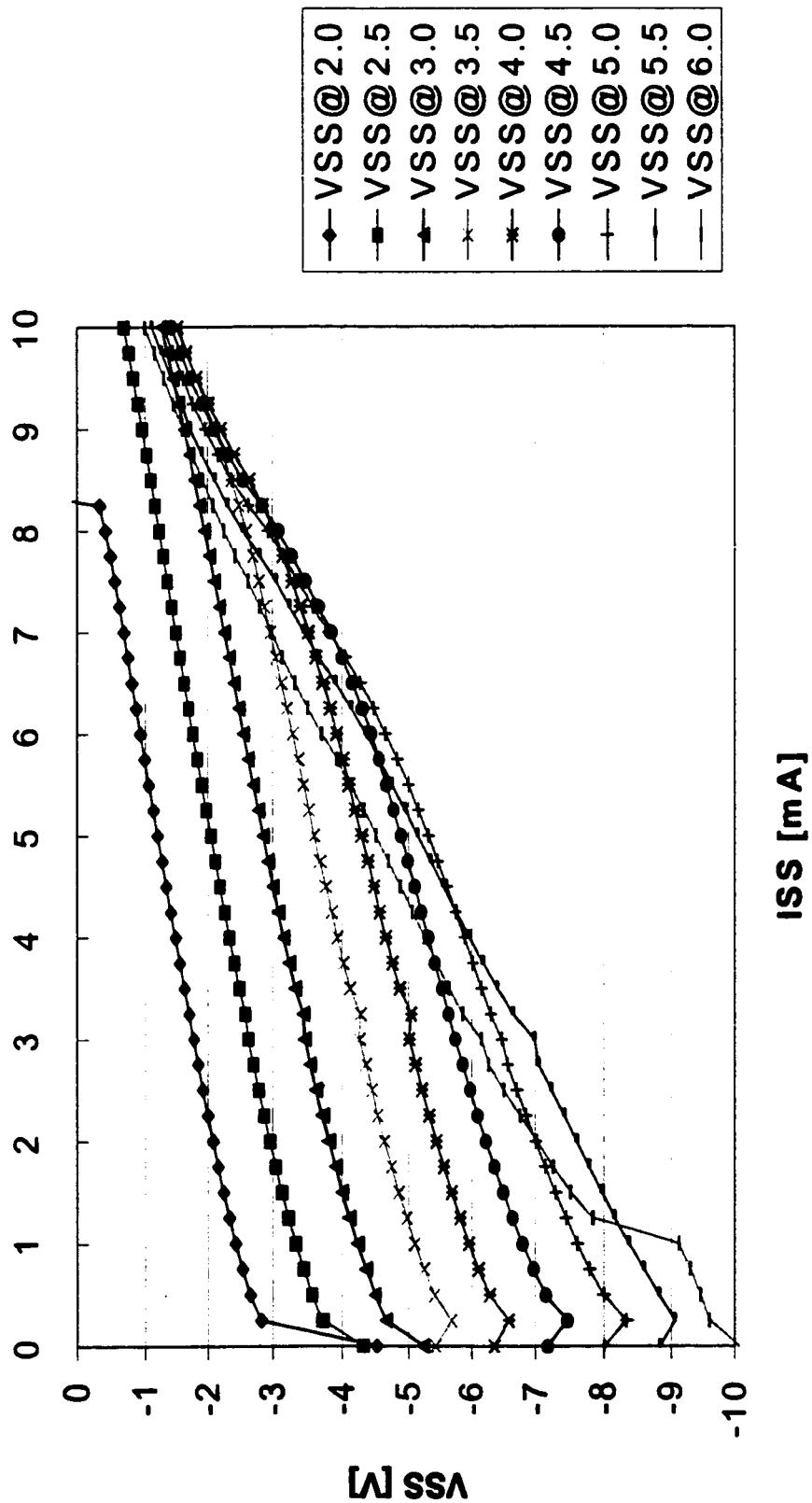

Fig. 4.14 VSS vs. ISS for L = 2nH, F_{osc} = 6GHz.

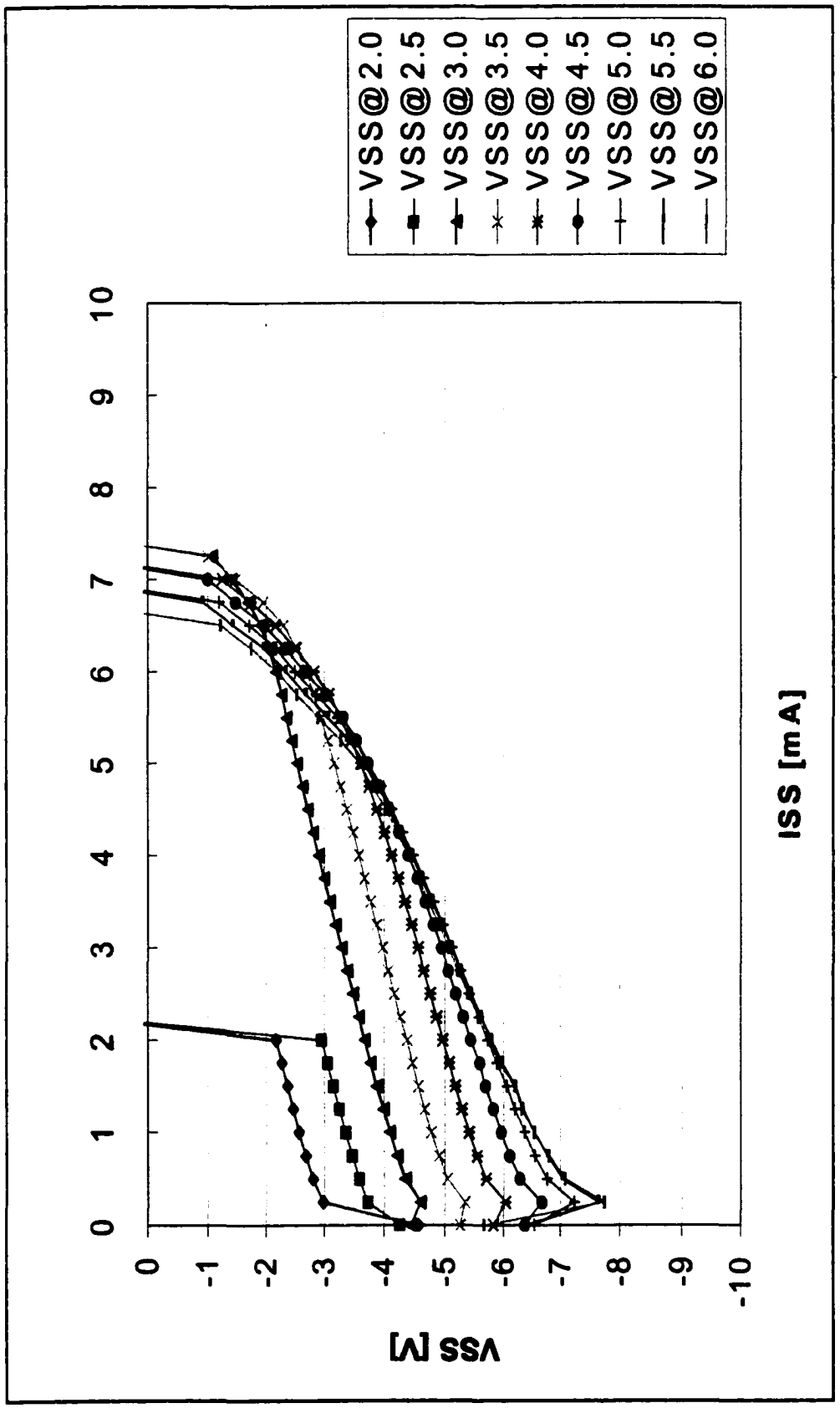

Fig. 4.15 VSS vs. ISS for L = 1nH, F_{osc} = 9GHz.

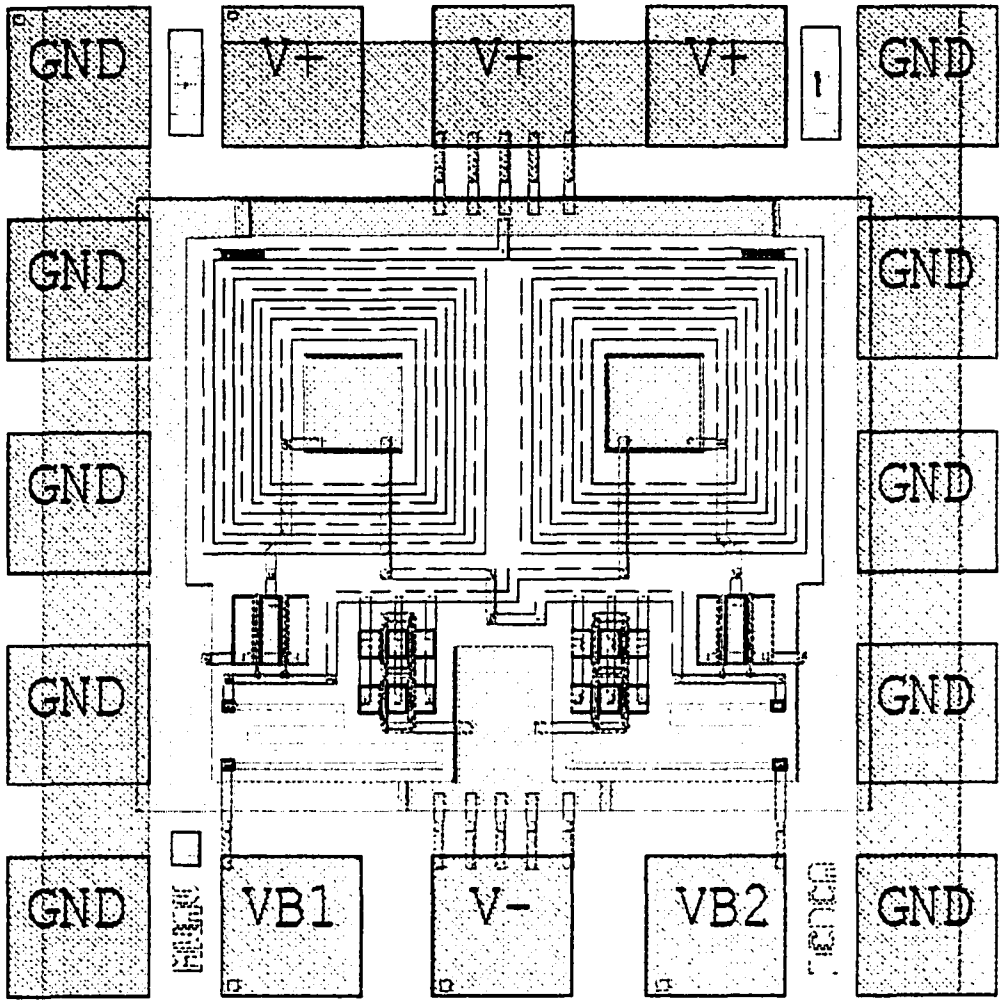

Fig. 4.16 Die layout of the 4nH Microwave DC/DC converter.

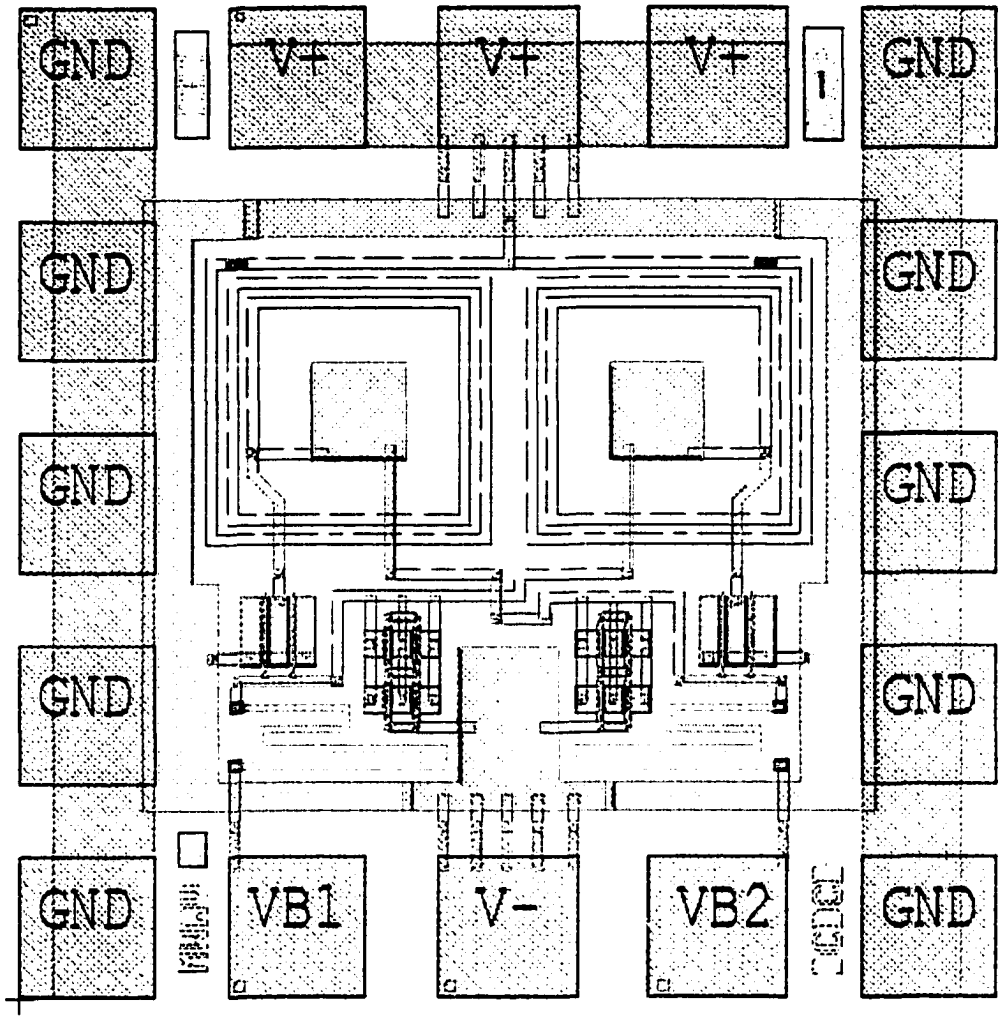

Fig. 4.17 Die layout of the 2nH Microwave DC/DC converter.

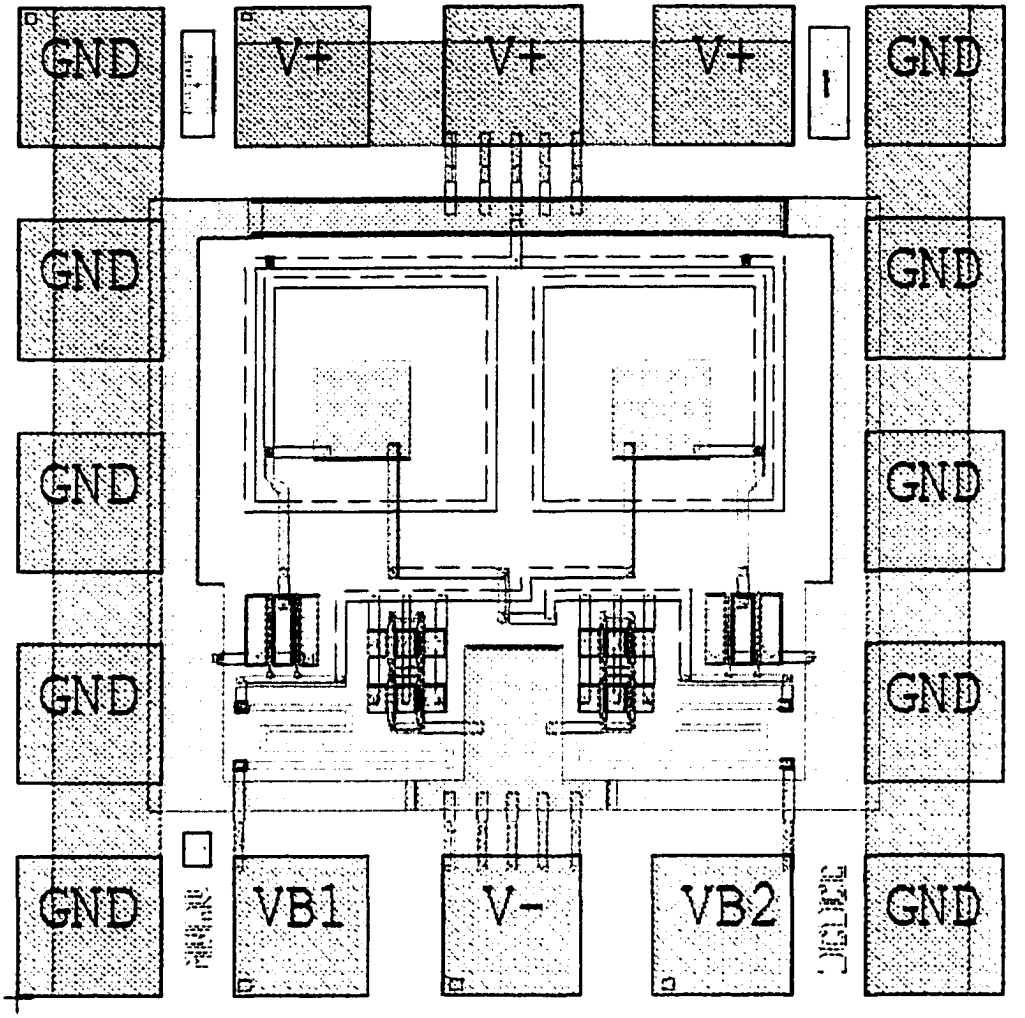

Fig. 4.18 Die layout of the 1nH Microwave DC/DC converter.

The circuit has all necessary components on chip and no external parts are needed, the size of the die without the bondpads can be as small is $0.2mm^2$, that is a savings of over 97% compared to the switched capacitor DC/DC converter presented in chapter III. Fig. 4.19 shows a graphical comparison between the two circuits and the external components associated with them.

The noise contribution of this circuit is minimal due to the fact that the oscillator frequency is above 4Ghz, which puts it well outside the communications band for most applications. This design is a differential one, and hence the input line and the output line have frequency components at twice the oscillator frequency. A 6GHz oscillator will have spurious at the 12GHz, which puts it well outside the communications band of the applications. Since the oscillator signals are closer to sinusoidal waveforms, than square, they have less harmonic content, and hence are less interfering with the rest of the system.

The devices used are of nominal values in terms of feature size, all transistors are of 0.5 um gate-length, which is similar to the process control monitor (PCM) ones. There is no mix of different feature sizes, and that makes it easier to process and have higher production yields.

The circuit produces an output voltage that is higher in magnitude than the supply voltage for low load currents. That makes it ideal for low voltage applications.

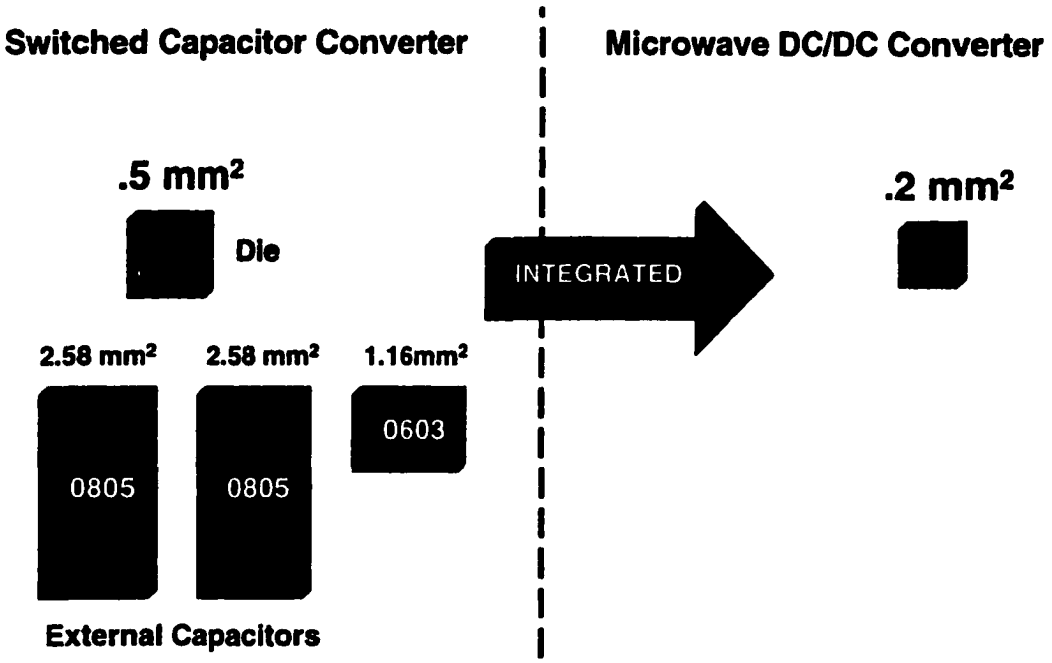

Fig. 4.19 Space savings of the MWDCDC converter as compared to the switched capacitor converter.

5 CHAPTER V

Applications

5.1 Introduction

The two DC/DC converters presented in chapter III and IV, were built in a depletion mode MESFET technology. They were then used in a variety of applications ranging from GaAs wireless power amplifiers, to GaAs transimpedance amplifiers. In this chapter, we are going to present some of these applications.

5.2 GaAs Wireless Power Amplifiers

Wireless power amplifiers are mainly narrow band amplifiers, they are found in handsets and in base stations. GaAs power amplifiers made with depletion mode MESFET's require negative voltage for biasing and shut down as explained in chapter I.

High efficiency power amplifiers in handsets translate to longer talk time. Class B or class C amplifiers deliver higher efficiency amplification. 20dB to 30dB of amplification are typical gain numbers. In order to deliver such gain, the transistors have to be large in size. Two or three stages are used with a final stage periphery in the order of 12mm or more. Such large devices are practically short circuits when they are biased ON. If they are powered up, without the presence of the negative voltage, they would short circuit the battery and get damaged. For that reason, a PASS transistor is used as a switch. The switch is turned on, only after the negative voltage is established, and is turned off before the negative voltage is removed. The PASS transistor is also turned off for power down

to prevent the leakage current through the GaAs power amplifier. In some applications, the DC/DC converter itself needs a PASS transistor, but that transistor is much smaller in size compared to the one needed for the PA.

Fig. 5.1 shows a typical arrangement of a GaAs power amplifier with its associated circuitry. A sequencing circuit does the job of monitoring the negative voltage and turning the PASS transistor ON when the negative voltage reaches a certain value. Typically, the DC/DC converter and the sequencing circuit are implemented in silicon. Both of the switched capacitor, and the microwave DC/DC converter were used to provide the negative voltage for a GaAs power amplifier.

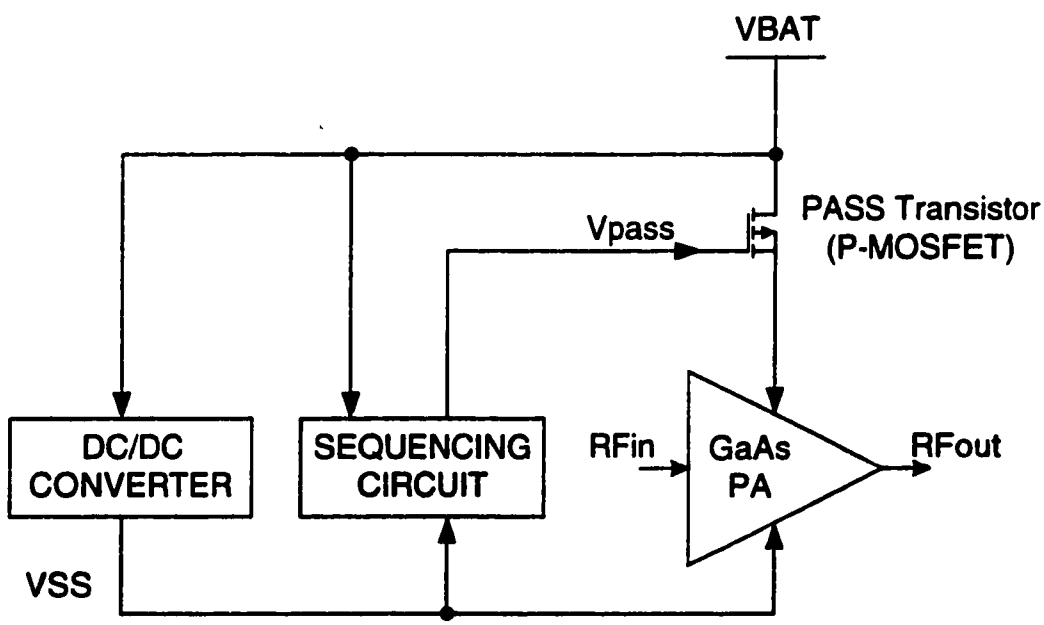

Fig. 5.1 GaAs PA with the associated circuitry; DC/DC converter, Sequencing circuit and a PASS transistor.

5.2.1 Sequencing Circuit

For higher level of integration, a sequencing circuit need to be built in the same GaAs process as the DC/DC converter. Fig. 5.2, shows a circuit that was integrated with both the switched capacitor and the microwave DC/DC converter.

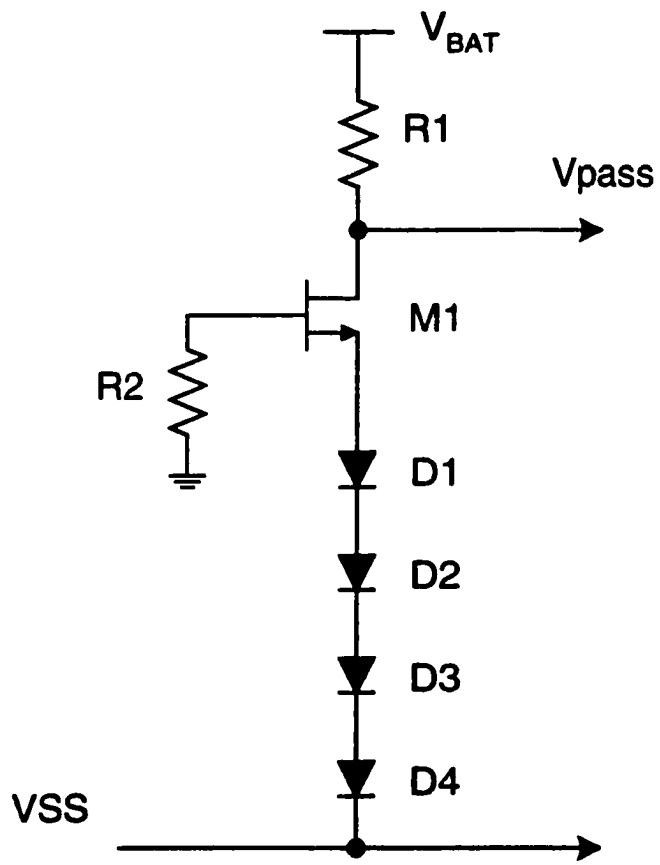

Fig. 5.2 GaAs sequencing circuit.

Fig. 5.3 shows the voltage (Vpass) when simulated with the rest of the microwave DC/DC converter. The following values were used for simulation: R1 = R2 = 2kΩ, total width (W_{M1} = 200μm), gate length (L_{M1} = 0.5μm). D1 through D4 were simulated and

fabricated as diode-configured MESFET's, where the drain and the source are tied together, all had a gate length of 0.5μm and a total width of 100μm.

When VSS is zero, M1 is OFF. And Vpass is pulled up by the pull-up resistor (R1) to the battery voltage (VBAT), this ensures that the PASS transistor is turned off, thus protecting the PA from large currents that can be destructive. And it keeps the leakage current down in standby mode.

It is not intuitive, why M1 is OFF when VSS is zero. The reasoning goes as follows: if M1 is ON, then the gate-source voltage is higher than the pinch off voltage (-0.7V). The drain current of M1 is going through the series of diodes, and that means that the voltage across each diode is about 0.7V. Now, if we add the diode voltage drops starting from VSS, and ending at the source voltage of M1, they add up to 2.8V. So, the source voltage of M1 has to have a positive voltage of 2.8V. But, since the gate voltage of M1 is tied to ground, it can not have a potential higher than 0V! That means that M1 in this case has a maximum gate-source voltage of –2.8V, which is lower than –0.7V, and M1 has to be OFF. So, when VSS is zero, M1 is OFF.

As VSS becomes negative, the source voltage of M1 follows, and at one point it approaches –0.7, at which M1 starts to conduct, and current starts to flow through R1, the voltage drop across R1 increases, and Vpass starts dropping. When Vpass drops low enough, the PASS transistor turns on.

When the DC/DC converter is turned off, VSS collapses, and as it is approaching zero potential, the same sequence happens in reverse, where the PASS transistor is first turned off, then M1 turns off. Thus, the PASS transistor is ON, only in the presence of VSS.

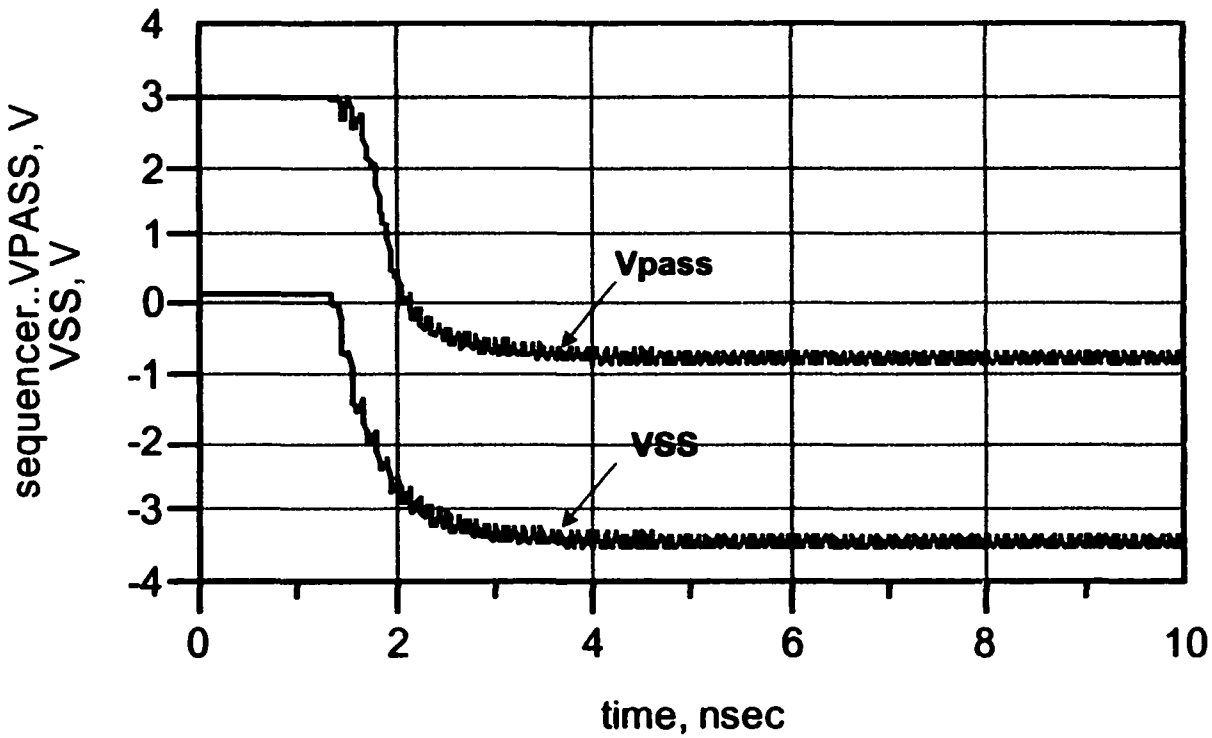

Fig. 5.3 Simulated Vpass of the sequencing circuit. VSS is shown for reference.

5.2.2 CDMA Module

This section introduces a product, where both the DC/DC converter and the sequencing circuit are used along with a GaAs PA. CDMA stands for Code Division Multiple Access, and it is the name for one of the wireless standards.

Fig. 5.4 shows a block diagram for that application, a three stage power amplifier is used to amplify a signal that conforms to the CDMA standard. A PASS transistor is used to shut off the PA. A sequencing circuit, along with a microwave DC/DC converter are used. V+ is a regulated supply voltage, while Vbatt is not regulated. Vref adjusts the gain of the amplifier, RFin/Vg1 is the input RF port and is the gate voltage of the first stage. Vg2 and Vg3 are the gate voltages of the second and the third stage. Rfout is the output port, and Vpa is the drain voltage of the PASS transistor.

IPM stands for Intelligent Power Management, which is a patented circuit that adjusts the bias of the three stages as a function of Vref.

Fig. 5.5 shows the layout or floor plan of the module. The module is square and is 7mm on the side. Fig. 5.6, is a microphotograph showing the actual components used to populate the board. The GaAs die is in the middle, while the PASS transistor die is in the top left corner. Other components include surface mount resistors, capacitors and an inductor.

Fig. 5.7 shows the layout of the GaAs die, both of the microwave DC/DC converter and the sequencing circuit are used.

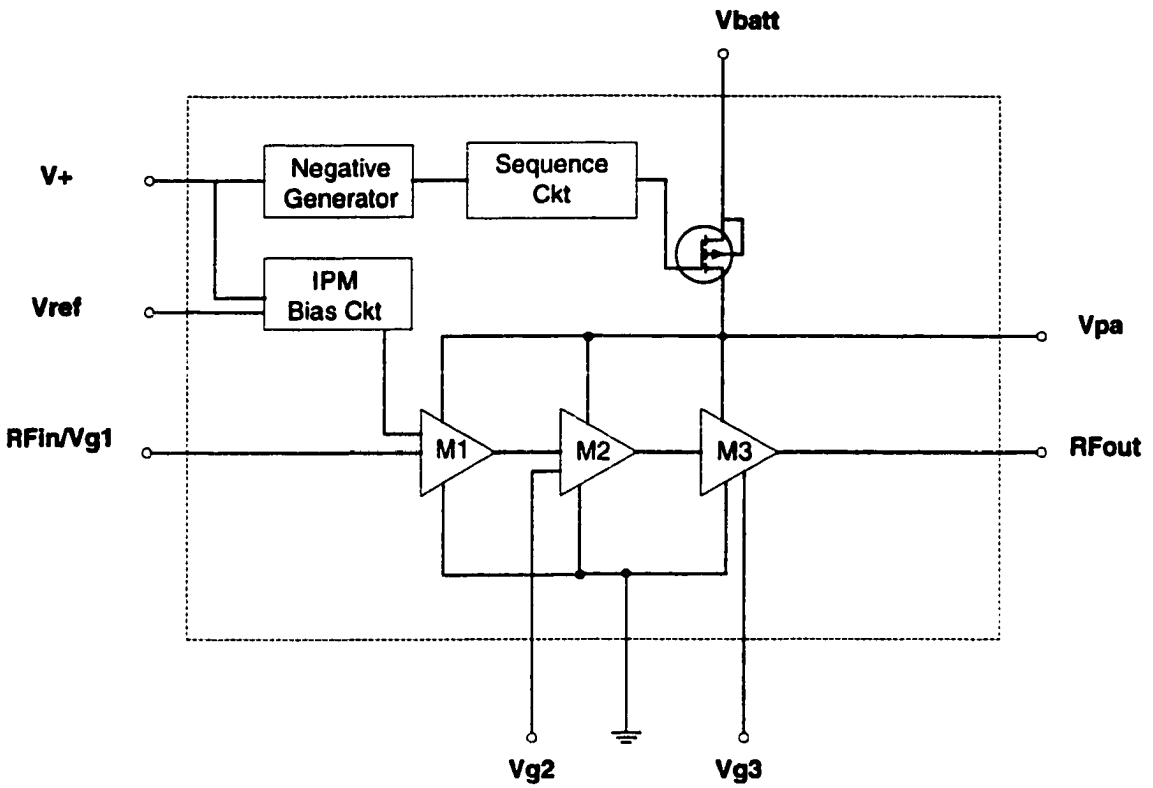

Fig. 5.4 Block diagram of the functional blocks of the CDMA PA module.

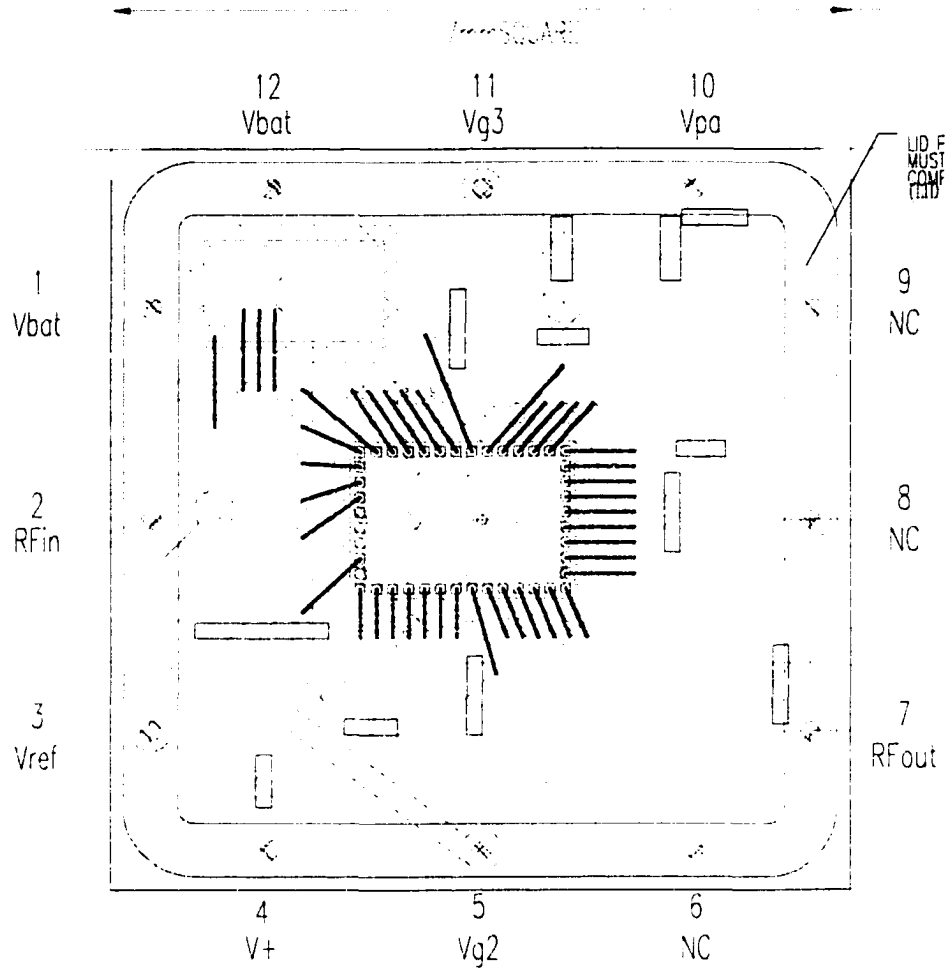

Fig. 5.5 CDMA module layout.

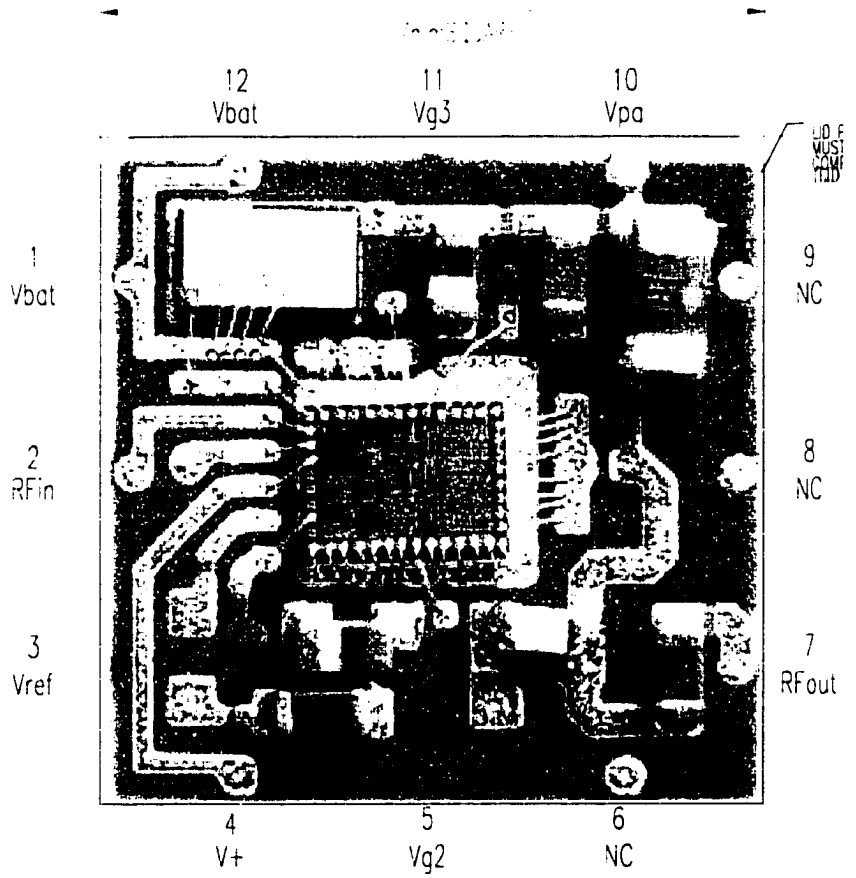

Fig. 5.6 Microphotograph showing actual components.

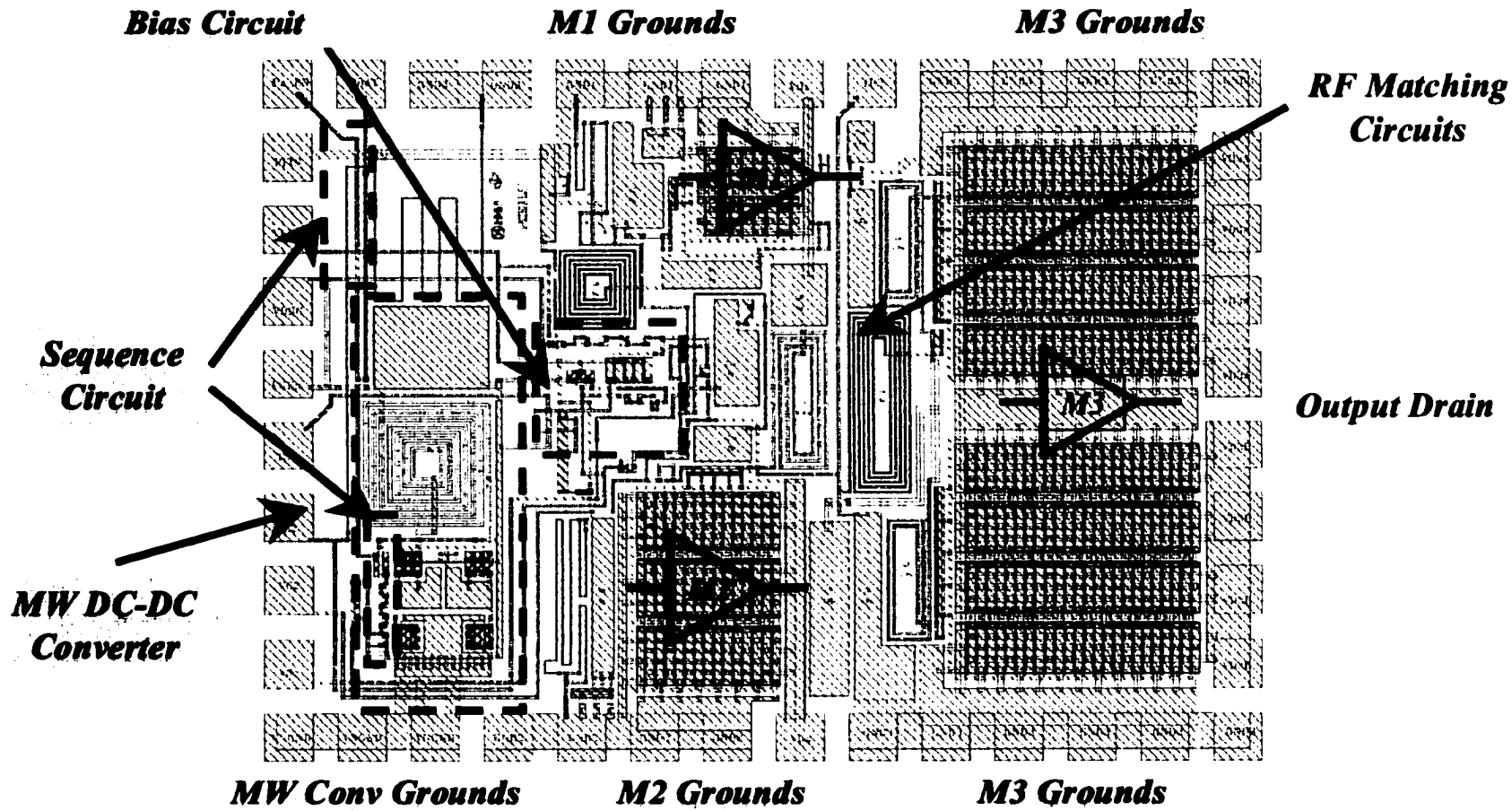

Fig. 5.7 Die layout of the GaAs circuit in the CDMA module.

5.3 Transimpedance Amplifier (TIA)

5.3.1 Introduction

Modern telecommunications networks transmit and receive data on fiber optic links. Semiconductor lasers are modulated with the data that is to be transmitted and the output light from these lasers are coupled to optical fibers for short or long distance transmission. At the receive end, a photodetector (PD) is used to convert the light pulses that emanate from the fiber into small electrical currents. An electronic device known as a Transimpedance Amplifier (TIA) converts this small current pulses into voltage pulses that is further amplified and utilized by the other components in the receive chain.

An example of this optical data transmission system is the Gigabit Ethernet optical transceiver system diagram shown in Fig. 5.8. It is comprised of optical devices, and both analog and digital ICs. The transmitter front end requires laser or LED and driver circuitry, while the receiver consists of a photo-detector, a low noise Transimpedance Amplifier (TIA) and a high gain post-amplifier. The back end is comprised of digital ICs that handle the data using Serializer/Deserializer chipsets, which feed into higher layer functions. This fiber optic transceiver is used in local area network interface cards (NIC), switches, routers and hubs.

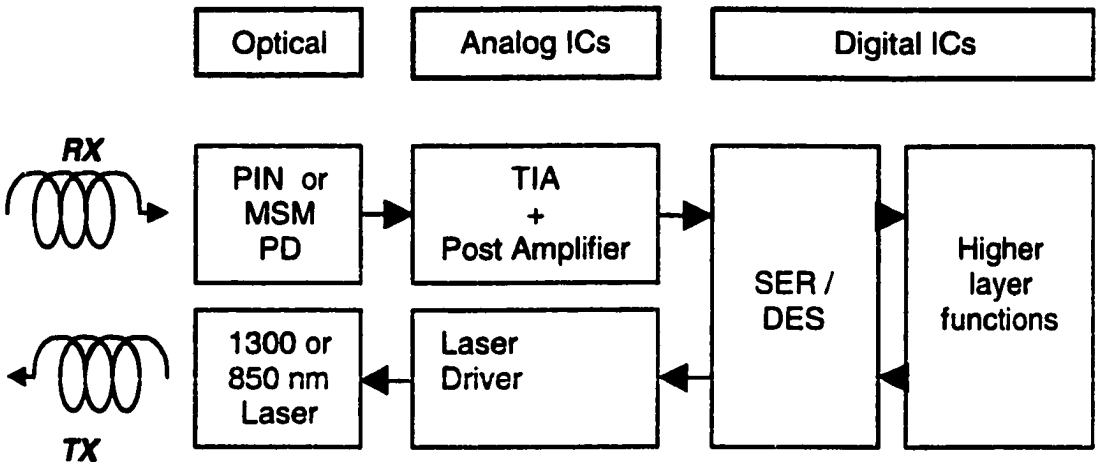

Fig. 5.8 Data communication transceiver system.

5.3.2 Photodetector

An optical photo-detector converts optical power in a specified band of wavelengths into an electrical current. The typical method of photo-detection is to illuminate a semiconductor material with the optical power, which results in the generation of electron-hole pairs by the absorbed photons in the material. These electron-hole pairs can be swept away by an electric field to generate current pulses.

The performance of the photodetector is measured by the efficiency with which it converts optical power to electrical light and by its speed. The conversion efficiency called Responsivity (R) is the ratio of the electrical current produced by the detector to the incident optical power. The responsivity is measured in Amperes/Watt. The speed of the photo-detector is measured by its Bandwidth (f_{3db}). The bandwidth can be determined by measuring the rise (T_{rise}) and fall (T_{fall}) times of the electrical current produced by a very fast optical pulse and by using the following formula:

$$f_{3db} = \frac{0.35}{T_{rise}} Hz \qquad (5.1)$$

The typical performance of a Metal-Semiconductor-Metal (MSM) photodiode yields a DC responsivity of 0.40 A/W and a bandwidth of 2400 MHz at a bias voltage of 4.5 V for a (100 x 100 $\mu m^{2)}$ geometry. The performance over reverse bias voltage is shown in Fig. 5.9. The plot shows that a photodiode bias voltage >3 V is necessary to maintain the required performance for 1.25 Gb/s and 2.5 Gb/s operation with high responsivity and sensitivity.

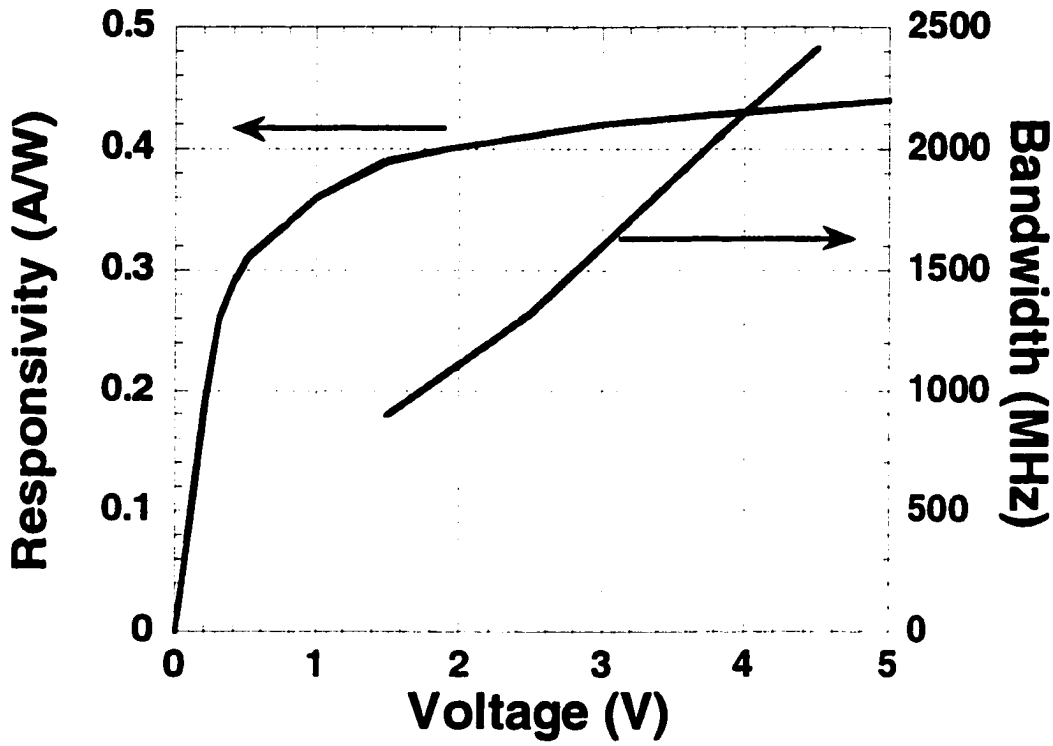

Fig. 5.9 MSM PD performance with revere bias.

5.3.3 Photodetector biasing at low power supply voltages

To reduce power consumption and manufacturing costs, and increase efficiency, communication systems are increasingly designed to operate at 3V. This reduction in power supply voltage is needed with higher performance operation. With the operating supply voltage at 3 V, it becomes very difficult to ensure adequate reverse bias on the photodetector and at the same time bias the amplifier properly for high performance operation. As shown in Fig. 5.9, the photodetector requires approximately 2.5 V reverse

bias for good responsivity and high bandwidth. If the detector is connected to the positive power supply, then only about 0.5 V is available to bias the gate and source of the input FET. This severely constrains the dynamic range of the amplifier output stages and also severely restricting the circuit topologies that could be used to improve the performance at the input stage. This constraint is more apparent in circuit topologies that use FET based technologies such as MESFET or Pseudomorphic-High-Electron-Mobility-Transistor(pHEMT) devices. Since these technologies offer superior sensitivity than other technologies, it becomes extremely difficult to design high performance receiver front ends (photodetector and transimpedance amplifiers) with power supply voltage at 3 V.

To relieve this constraint, a separate negative voltage can be used to reverse bias the photo-detector enabling a much higher degree of freedom in optimizing the first stage of the transimpedance amplifier. This negative voltage can also be used to power up some non-critical stages in the amplifier enhancing the performance.

The microwave DC/DC converter is used to provide this negative voltage. The converter is integrated on chip along with the MSM-TIA.

Connecting the photo-detector as shown in Fig. 5.10, ensures a reverse bias of about 3.5 V across the photodetector This also enables the transimpedance amplifier to be separately optimized irrespective of the reverse bias applied to the photodetector.

The on-chip negative voltage generator is composed of a 6.5 GHz microwave DC/DC (MWDCDC) converter. The oscillator frequency is chosen such that any fundamental and higher harmonics are out of band of the data rate bandwidth. By careful layout, the

fundamental feed-through of the oscillator that appears at the output is minimized. There is about -35 dBm of fundamental frequency appearing at the output, but this leakage is effectively filtered by the post-amplifier and other bandwidth limiting components in the receive chain. This leakage component cannot be considered as wide-band noise and hence no sensitivity penalty is paid.

Fig. 5.11 shows a the die layout of the TIA with the integrated microwave DC/DC converter, Vn is the negative output voltage pad. For space savings, and better balance, one center tapped inductor is used to replace the two separate inductors.

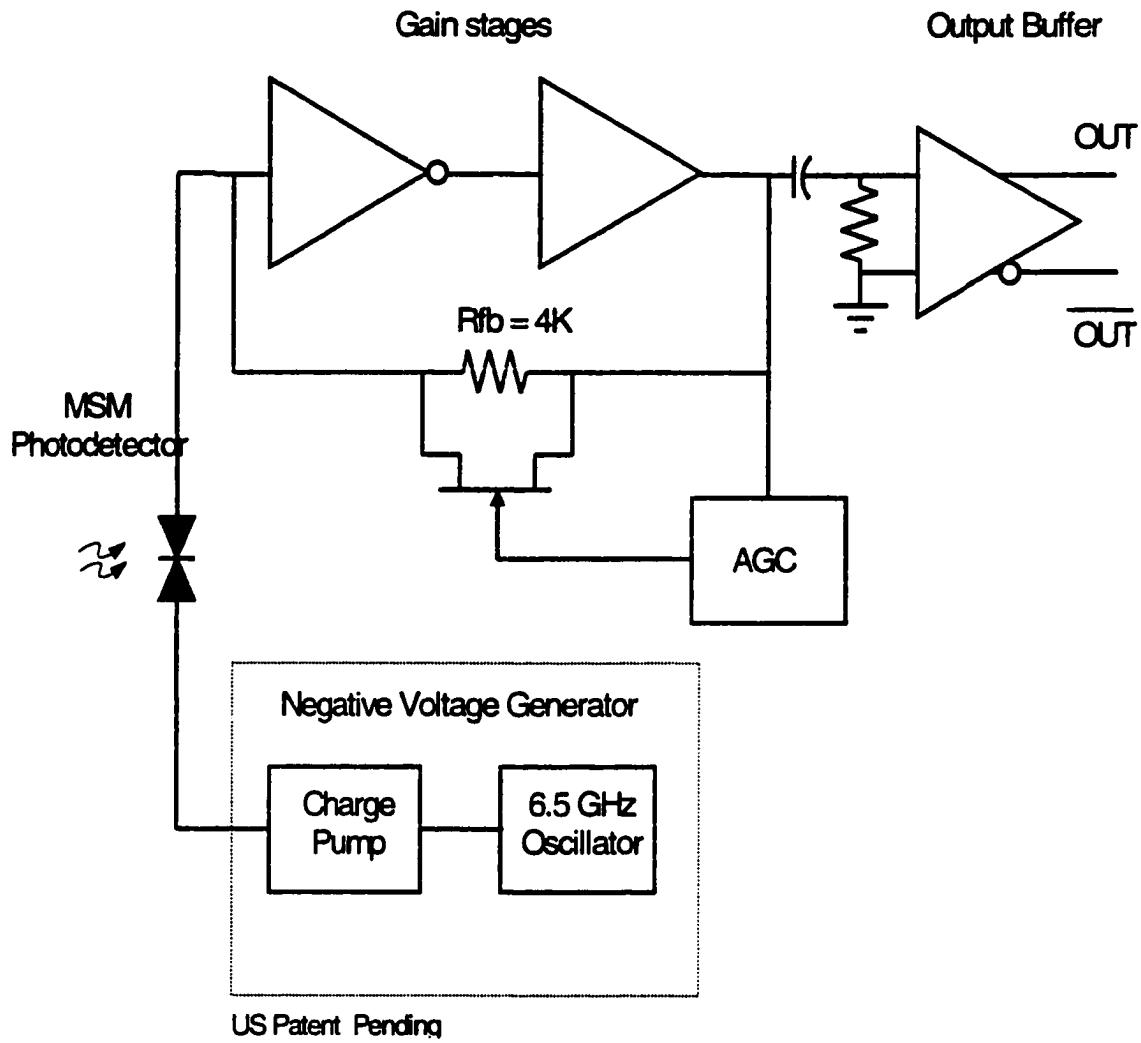

Fig. 5.10 Block diagram of MSM-TIA with on-chip MWDCDC converter for high performance photodetector biasing.

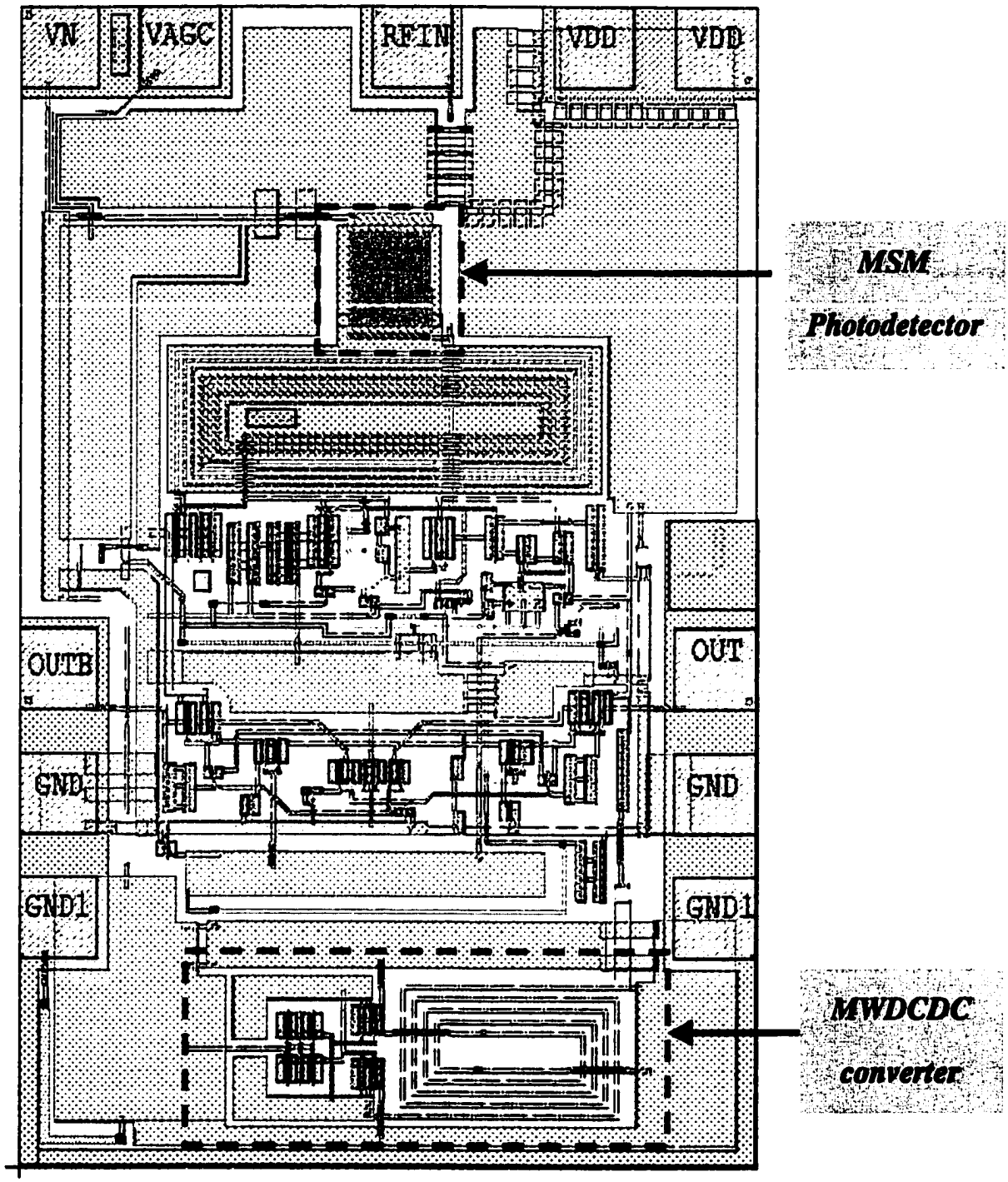

Fig. 5.11 Die layout of the MSM-TIA with the integrated MWDCDC converter.

6 CHAPTER VI

Conclusions

6.1 Summary

This thesis addresses the need of GaAs circuits for negative voltage. First, a brief comparison between GaAs and Si was presented. Then it was shown why depletion-mode GaAs MESFET circuits need negative voltage. In order to come up with negative DC/DC converter designs, the most common switch-mode DC/DC converter were presented in detail. After that, the first GaAs converter design was presented; the switched capacitor design. Analytical as well as experimental results were presented.

After discussing the advantages and disadvantages of the switched capacitor design, the microwave DC/DC converter is introduced. After introducing the design approach, experimental results were presented.

Applications of both converters are presented in chapter V, the first is a GaAs wireless PA, and the second is a transimpedance amplifier. Both used the GaAs DC/DC converters presented in this thesis. A sequencing circuit was also introduced in PA architecture. Block diagrams as well as die layouts are discussed.

6.2 Future Work

The designs presented were fabricated in a depletion-mode MESFET technology, and were used in practical applications. Millions of these converters were built for commercial products and have provided technological advantages to these applications.

The switched capacitor design is mainly used in wireless hand-held devices, while the microwave DC/DC converter is widely used in broadband transimpedance amplifiers.

Future work can be focused on improving the efficiency of the microwave DC/DC converter. Recent work [12], presents a microwave DC/DC converter that reaches a maximum power conversion efficiency of 49%, but it is built out of discretes and is built on a board that is 14-cm long, and 7-cm wide. It does deliver higher output power though.

Electromagnetic (EM) simulators can be used to optimize the passive components in the microwave converter, these components include interconnects and the spiral inductors. Spiral inductors tend to radiate energy at high frequencies. The use of an electromagnetic simulator that accounts of radiation is a good tool for optimizing such structures. In the market, there are several commercial products that use the Method of Moments for solving for the electromagnetic fields in a given geometry.

Impedance matching [12] can be experimented with to improve the efficiency.

Reducing the parasitics should lead to higher efficiency. This can be achieved via optimizing the layout or by using different active devices. MESFET's connected as diodes can be used in place of N- diodes to reduce parasitic capacitance.

For applications that require an even higher oscillator frequency, bond wires can be used in place of the spirals to realize a low inductance, high-Q inductors.

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