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A

**Shadow Mask Selective Area Molecular Beam Epitaxy  
for Applications in Device Processing and Integration**

by

**Yuanyuan Luo**

**A dissertation submitted to the Graduate Faculty in Chemistry in partial  
fulfillment of the requirements for the degree of Doctor of Philosophy,  
The City University of New York**

**2000**

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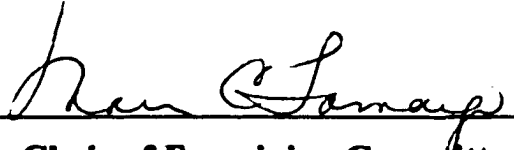
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# ABSTRACT

## **Shadow Mask Selective Area Molecular Beam Epitaxy for Applications in Device Processing and Integration**

by

Yuanyuan Luo

Advisor: Prof. Maria C. Tamargo

This thesis describes the development of a shadow mask selective area molecular beam epitaxy (MBE) technique and its applications in device structure processing and integration.

Two kinds of mask fixtures were designed and fabricated to perform shadow mask selective area epitaxy (SAE) during molecular beam epitaxial growth. The *ex situ* mask fixture requires the mask to be placed and removed outside the growth environment during the mounting and removing of the substrate. The *in situ* mask fixture allows the mask to be placed and removed inside the vacuum chamber. Therefore patterned layer growth can be performed within the structure wherever desired and multiple step SAE can

be performed for complex device structures. The growth behaviors of the shadow mask SAE employing these fixtures were investigated and presented.

The implementations of the shadow mask SAE technique on device structure processing and integration were demonstrated by the in situ processing of Au/CdTe detector-array-like structures for application in HgCdTe detector array fabrication, and by the integration of different ZnCdSe quantum wells on a single GaAs or InP substrate for application in integration of red-green-blue (Zn,Cd,Mg)Se based light emitting diodes on single InP substrate. The in situ mask fixture was used in these applications.

The influence of the shadow mask SAE on material quality was studied by investigating the defect density of the patterned CdTe and ZnSe layers grown with the shadow mask. Similar defect density was observed from these patterned epilayers as from the flat epilayers, indicating that no deleterious effect on the material quality was caused by the use of shadow mask. However, we were unable to identify if there is any defect reduction effect by the use of shadow mask SAE as there is with the patterned-substrate SAE due to the limited growth area.

A wide range of characterization techniques such as Photoluminescence (PL), micro-PL, X-Ray Diffraction (XRD), Secondary Ion Mass Spectroscopy (SIMS), Scanning Electron Microscopy (SEM) and

**Atomic Force Microscopy (AFM) were used in this research work to characterize the materials and device structures fabricated.**

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# CHAPTER 1

## INTRODUCTION

Molecular beam epitaxy (MBE) is a versatile crystal growth technique involving the interaction of atomic or molecular thermal beams with a single crystalline surface under ultrahigh vacuum. Its implementation and use involve a wide range of research in the fields of physics, chemistry, electrical engineering, and material science. With the ability to control the growth with atomic layer accuracy, it has proven strength in fabricating electronic and optoelectronic devices.<sup>[1]</sup>

Mercury Cadmium Telluride (HgCdTe) is an important material for infrared (IR) detection. It is appropriate for detecting IR radiation with very wide wavelength range by varying the Hg composition.<sup>[2]</sup> HgCdTe detector arrays with ~20-50 $\mu$ m pitch sizes are being developed for various military, commercial and astronomy applications.<sup>[3]</sup> MBE is a useful technique for the growth of HgCdTe.<sup>[4,5]</sup> Once the multi-layered structure is grown, the detector arrays are processed using photolithography and etching methods. The subsequent metal contact fabrication involves defining the metal contact area using photolithography, surface cleaning using chemical etching and plasma asher, and final metal layer deposition. These complex post growth

reticulation and metallization processes limit the yield of HgCdTe detector arrays.<sup>[6]</sup>

Semiconductor lasers and light emitting diodes (LEDs) emitting in the visible spectrum have potential applications in full color displays, high speed laser printing and high density digital recording.<sup>[7]</sup> Wide bandgap  $\text{Zn}_x\text{Cd}_y\text{Mg}_{(1-x-y)}\text{Se}$  lattice matched to InP is a new quaternary material system that can be used in the design and fabrication of red-green-blue (R-G-B) lasers and LEDs. By using different composition  $\text{Zn}_x\text{Cd}_y\text{Mg}_{(1-x-y)}\text{Se}$  layers as cladding, waveguiding and active layers, we can design totally lattice matched or pseudomorphic laser and LED structures with emission throughout the entire visible spectrum, from blue to red.<sup>[8,9]</sup> These properties make it possible to consider integrating full color display devices on a single InP substrate.

Selective area epitaxy (SAE) is a non-planar growth technique that is attractive for device applications, including HgCdTe detector arrays and integrated full color display devices. It enhances the capability of crystal growth techniques by locally defining areas where the desired structures can be grown using dielectric masks, patterned substrates or mechanical shadow masks.<sup>[10]</sup> It also has potential in achieving monolithic integration of optoelectronic components.<sup>[11-13]</sup> Furthermore, the reduction of the substrate

area through selective area growth can improve the quality of the lattice mismatched epilayers by reducing misfit dislocation densities.<sup>[14,15,16]</sup> The use of a mechanical shadow mask to block selectively the arrival of the molecular beams onto the substrate is a simple one. Since the mask can be easily removed from the surface *in situ*, it is also suitable for multiple step SAE needed for the fabrication of complex device structures.

In this thesis, I will present the development of a mechanical shadow mask selective area molecular beam epitaxy technique. Its applications in device structure fabrication, specifically in the *in situ* fabrication of HgCdTe detector arrays and integration of R-G-B full color displays based on (Zn,Cd,Mg)Se material system, will also be covered. Two mask fixtures were designed and fabricated for this study. The shadow mask SAE growth of patterned CdTe and *in situ* fabrication of Au/CdTe detector-array-like structure were performed as a demonstration of this technique for *in situ* device structure processing. The integration of different ZnCdSe quantum wells on a single GaAs or InP substrate was also performed to demonstrate the application of shadow mask SAE in device integration.

Chapter 2 introduces the basics of molecular beam epitaxy. The growths of CdTe on CdTe and CdZnTe substrates, ZnSe on GaAs substrate, ZnCdMgSe on InP substrate are described in detail in this chapter.

Chapter 3 introduces the concept of selective area epitaxy and the various ways to implement it. The mechanical shadow mask SAE is explained in detail since this is the technique used in this research. The influence of SAE on material defect density and the design and fabrication of the shadow masks used in this research are also presented.

Chapter 4 describes the material characterization techniques used in this research. They include Nomarski optical microscopy, scanning electron microscopy, atomic force microscopy, surface profilometry, thickness measurement, photoluminescence, x-ray diffraction, etch pit density measurement, secondary ion mass spectroscopy and adhesion test.

The development of the mechanical shadow mask SAE technique is described in detail in chapter 5. This was first performed by using an *ex situ* mask fixture that requires the mask to be attached to the substrate outside the MBE growth chamber during the mounting of the substrate. The gradual improvement of the mesa pattern definition along with the improvement of the mask fixture design and incident flux beam geometry are described in sequence. The shadow mask SAE growth habits developed based on these growth experiences are summarized. The growths of square array patterned CdTe structures using the optimized *ex situ* mask fixture and a mask design consisting of different size square window arrays that is more applicable for

HgCdTe detector array fabrication are also presented. Based on the growth experience with the *ex situ* mask fixture, an *in situ* mask fixture that allows the mask to be placed and removed within the MBE system was designed and fabricated. It enhances the capability of the shadow mask SAE. By using the *in situ* mask fixture, substrate oxide desorption can be performed without the presence of the mask, patterned layers can be grown within the structure wherever desired and multiple step SAE can be performed for complex device structures. The shadow mask SAE growth results obtained with this *in situ* mask fixture and its growth behaviors are presented.

Chapter 6 introduces the *in situ* fabrication of Au/CdTe detector-array-like structure using the *in situ* mask fixture as a demonstration of the shadow mask SAE technique for *in situ* device structure processing, especially for the HgCdTe detector array fabrication. The advantages of *in situ* metallization were also investigated and discussed.

Chapter 7 describes the growth and characterization of patterned ZnCdSe quantum wells and their integration on a single GaAs and InP substrate as a demonstration of the shadow mask SAE technique for device integration, especially in the integration of R-G-B full color display elements based on the (Zn,Cd,Mg)Se material system developed in our research group.

The influences of the shadow mask SAE on material defect density were investigated and they are presented in chapter 8. The CdTe/GaAs and ZnSe/GaAs material systems were studied.

Chapter 9 introduces the further enhancements of the *in situ* mask fixture design in an attempt to improve the performance of the *in situ* mask fixture and reduce the registration problem related with multiple step SAE.

The research in this thesis is summarized in chapter 10 and the directions for the future work are also pointed out in this chapter.

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# **CHAPTER 2**

## **Molecular Beam Epitaxy (MBE)**

### **2-1. Introduction**

Molecular beam epitaxy (MBE) is a versatile technique for epitaxial growth of semiconductor, metal and insulator thin films. It distinguishes itself from other vacuum evaporation techniques with its significantly more precise control of the beam fluxes and the deposition conditions.<sup>[1]</sup>

In this chapter, I will first introduce the principles of MBE and its in situ monitoring and analysis. The MBE system used in this research will be described and the MBE growth of CdTe, ZnSe and ZnCdMgSe will also be presented.

### **2-2. MBE principles**

MBE is an epitaxial growth process involving the reaction of one or more thermal beams of atoms or molecules with a crystalline surface under ultrahigh vacuum (UHV) conditions. The knowledge of surface physics and the observation of surface structure variations (by using reflection high energy electron diffraction which is abbreviated as RHEED) resulting from the relations between the atom arrival rate (beam flux) and the substrate temperature (which determines the mobility of the atoms on the surface)

allows considerable understandings of how to prepare high quality crystalline thin films with the compilation of atomic layer upon atomic layer.<sup>[2,3]</sup>

A conceptual schematic of the MBE growth is shown in Fig. 2-1. An MBE system consists of a substrate heated resistively to an appropriate temperature in an UHV environment. The substrate faces the fluxes of atomic or molecular beams that emanate from crucibles containing the source materials heated to appropriate temperatures to produce the desired flux. The growth process can be monitored by RHEED which consists of a high energy electron gun and a fluorescent screen for the observation of the diffracted electron beam pattern.

The atomic/molecular beams are usually generated thermally in knudsen-type effusion cells where quasi-equilibrium is maintained. Each cell contains a crucible that in turn contains one of the constituent chemical elements or compounds of the desired epilayer. The temperature of each cell is chosen so that the vapor pressure of the material is sufficiently high for generation of thermal energy atomic/molecular beam by free evaporation. After expanding in the vacuum space, the materials condense and order on the substrate surface under kinetically controlled conditions. Each cell is equipped with an individual shutter between the cell and the substrate. Operation of these shutters permits abrupt cessation or initiation of any given

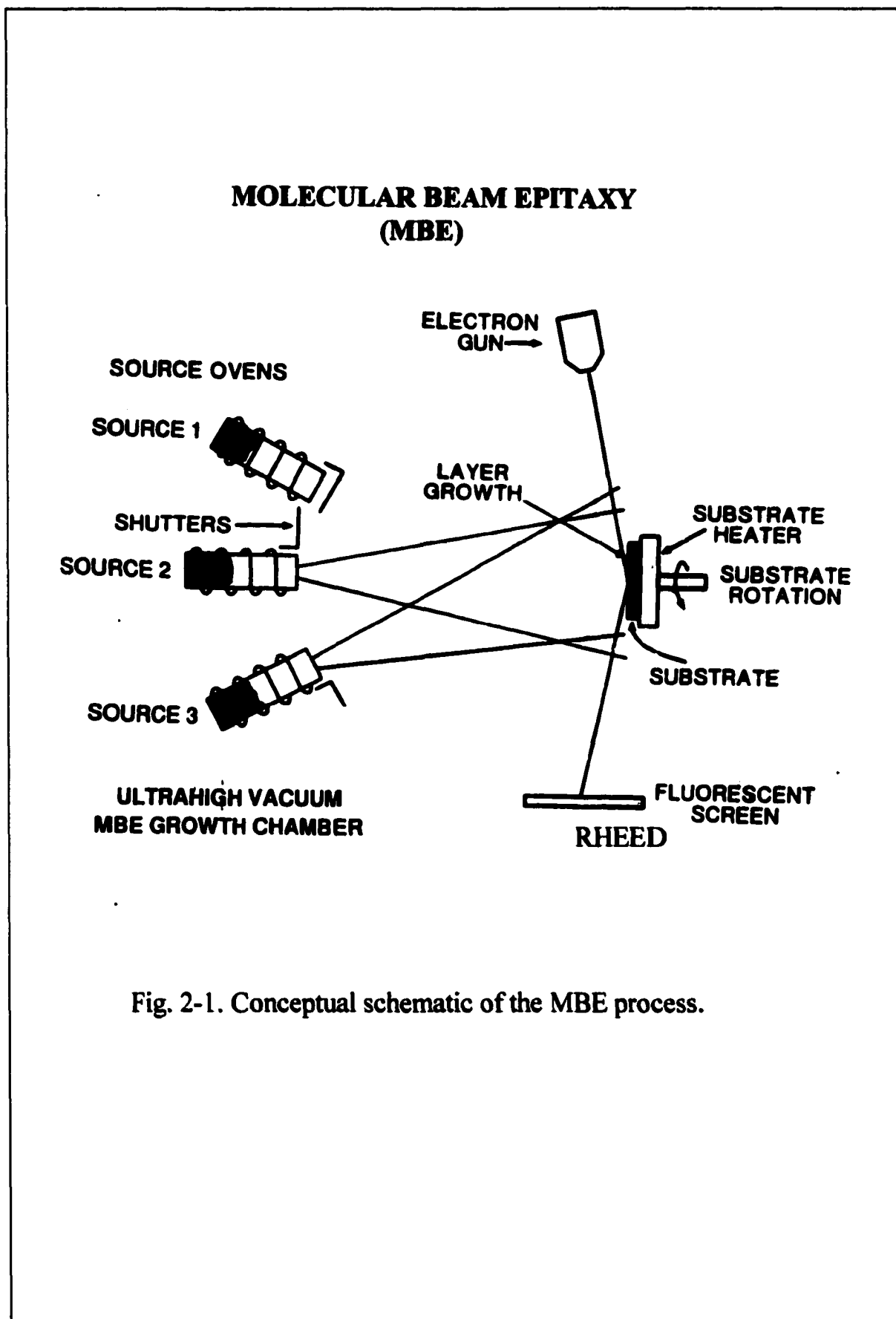


Fig. 2-1. Conceptual schematic of the MBE process.

beam flux to the substrate. The substrate assembly consists of a holder for mounting the substrate and a heater capable of raising uniformly the substrate to elevated temperatures. The substrate can be rotated during growth by using a rotation motor to improve the uniformity of the epitaxial layers. By choosing the appropriate cell through the opening of its shutter and the appropriate substrate temperature, epitaxial films of the desired chemical components can be obtained. The extremely high precision in beam flux control allows the growth of very thin layers, even monolayers. This distinguishing characteristic has enabled MBE to become one of the leading growth technologies for heterostructures including quantum wells and superlattices.

Additional accessory equipment inside an MBE chamber include a mass spectrometer for detecting leaks in the vacuum system or to measure the residual gases in the chamber, and a pyrometer to measure substrate temperature, etc.

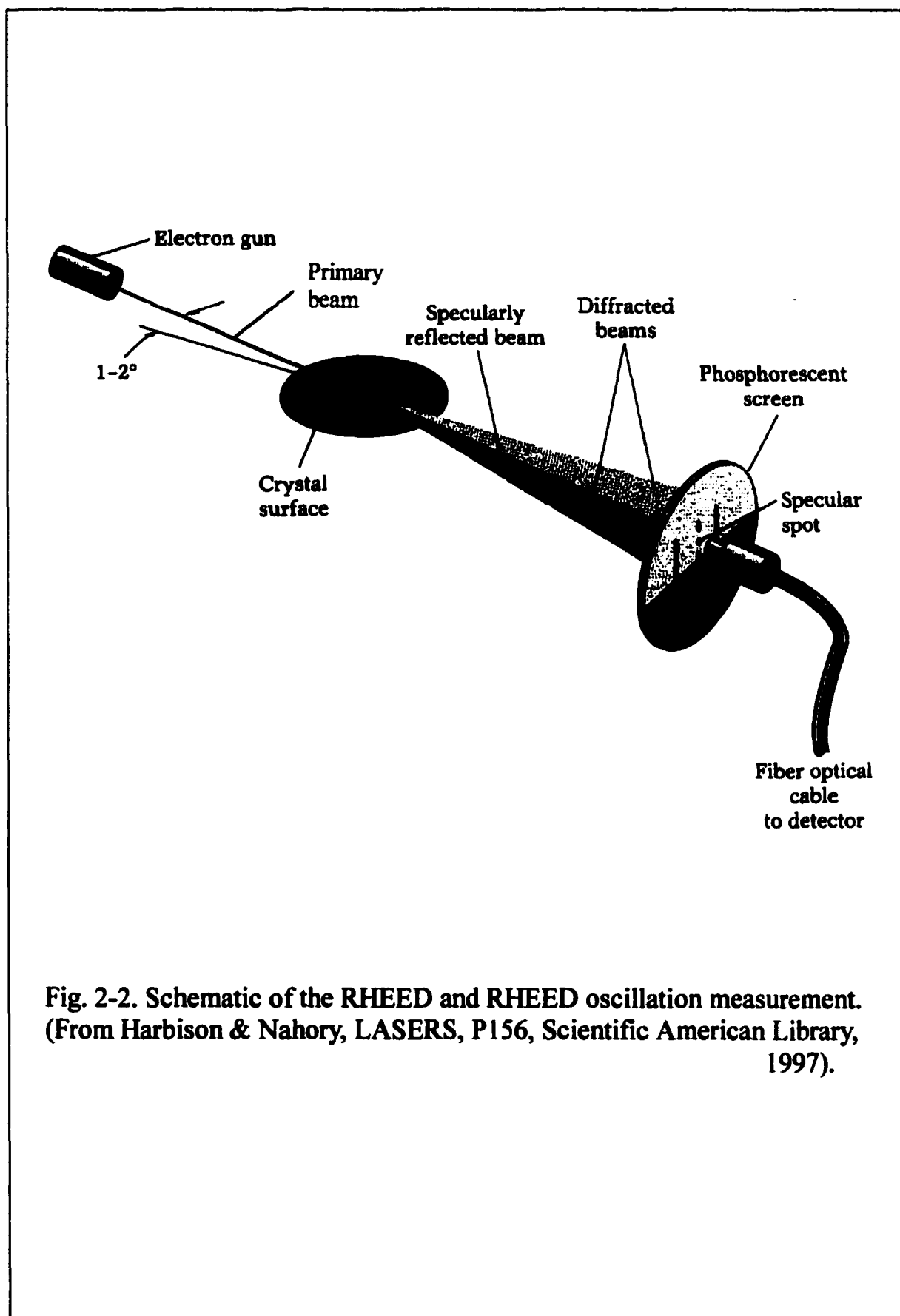
### **2-3. In situ monitoring and analysis in MBE**

While the UHV environment of the MBE system allows the growth of very pure materials, it is also ideal for *in situ* analytical instrumentation. It allows the placement of analytical instruments such as reflection high energy electron diffraction (RHEED) apparatus,<sup>[4]</sup> Auger electron spectrometers

(AES) and scanning reflection electron microscopes etc. inside an MBE chamber so that *in situ* monitoring and analysis can be performed.

It is desirable to have a RHEED apparatus in the MBE growth chamber because it gives information about substrate cleanliness and proper growth conditions. Fig. 2-2 shows the schematic of the RHEED. A monoenergetic electron beam (with high energy usually between a few keV to 50 keV) is incident on the substrate surface at glancing angle (a few degrees or less). This is called the primary beam. Because of the small component of the momentum normal to the substrate surface (which is only  $\sim 150\text{eV}$  even for the electrons having an energy of  $\sim 10\text{keV}$ ), beam penetration is limited to a few monolayers and the technique is therefore truly surface sensitive. The beam is diffracted by the surface and the near surface region, and the diffracted beam pattern can be observed on a phosphor screen. This geometry also allows the diffraction pattern to be observed while the growth is going on as the atomic/molecular beams are directed normal to the surface (see Fig. 2-1). Thus RHEED is an ideal method to monitor the substrate surface *in situ*.

The RHEED pattern depends on the atomic arrangement, flatness of the surface and the direction of the growth surface. A typical RHEED pattern for a disordered surface (for example the surface of the substrate before deoxidization) is a diffuse pattern or ring due to the thin amorphous oxide



**Fig. 2-2. Schematic of the RHEED and RHEED oscillation measurement.**  
(From Harbison & Nahory, *LASERS*, P156, Scientific American Library, 1997).

layer on the surface depending on the surface roughness;<sup>[5]</sup> for a clean substrate surface after deoxidization it is streaky lines or ordered spots.<sup>[5]</sup> For three dimensional growth it is ordered spots such as a bulk crystal pattern; for two dimensional growth it is streaky lines with surface reconstructions. The typical surface reconstructions for an As-rich (001) GaAs surface are  $(2 \times 4)$ ,  $c(4 \times 4)$  or  $c(2 \times 8)$  depending on how much excess As is on the surface; for a Ga-rich (001) GaAs surface they are  $(4 \times 2)$  or  $c(8 \times 2)$ ;<sup>[6]</sup> for a Se-rich (001) ZnSe the typical RHEED pattern is  $(2 \times 1)$  and for Zn-rich (001) ZnSe the pattern is  $c(2 \times 2)$ .<sup>[7]</sup> Therefore, from the RHEED pattern we can conclude whether the deoxidization is finished, whether the growth is two dimensional or which element terminates the surface.

Intensity oscillations of the RHEED pattern may be monitored as a function of the growth time to determine the material growth rate. Fig. 2-3 shows the plot of this intensity oscillations vs. time. Typically, the specular spot that is created only by electrons that are directly or specularly reflected off the surface without being diffracted by the underlying crystal structure is monitored since it is the brightest feature in the pattern and therefore intensity changes are more easily detectable. The intensity change can be monitored by an optical fiber connected to the photomultiplier tube (PMT) detector. The RHEED intensity measurement is also illustrated in Fig. 2-2.

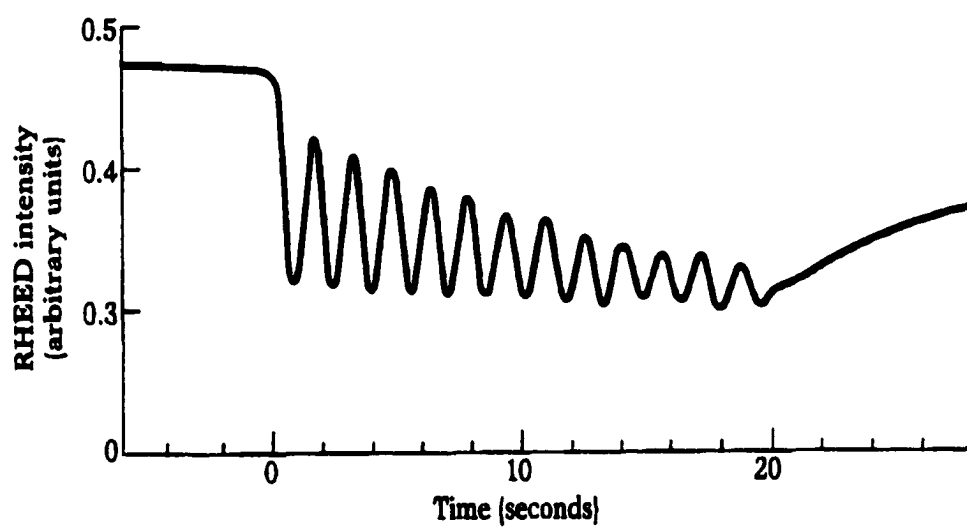
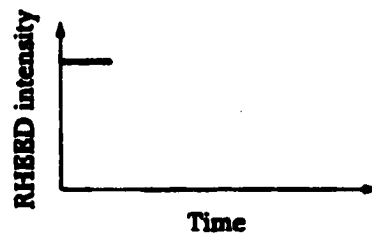
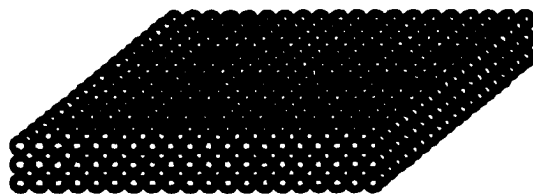


Fig. 2-3. Diagram of RHEED intensity oscillations vs. time.

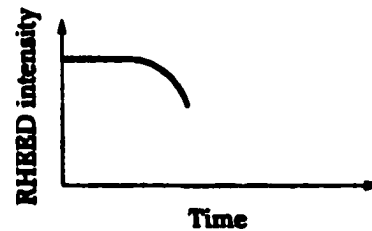
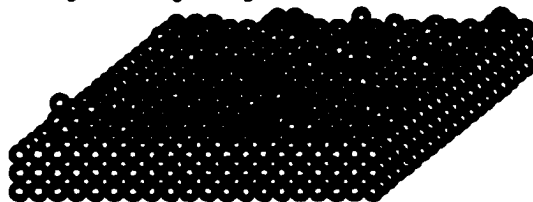
The oscillation effects in thin film growth can be explained in terms of layer by layer growth model.<sup>[8]</sup> The intensity of the specular spot in the RHEED pattern oscillates with changes in surface roughness. Fig. 2-4 illustrates this effect. Initially the surface is smooth and the specular electron reflection is at its maximum intensity (2-4-1). Then, as we begin to add atoms to the layer, it becomes increasingly rough and RHEED intensity begins to drop (2-4-2). This roughness reaches a maximum at about half a layer of coverage and the intensity drops to the lowest level (2-4-3). But thereafter the surface becomes smoother and smoother as the surface is almost filled with atoms and the RHEED intensity rises (2-4-4). Finally, the surface returns to its original smooth state once the layer is completed and the RHEED intensity goes to the highest level (2-4-5). Since nucleation is not restricted to a single layer but can reoccur before the preceding layer is complete, the subsequent roughening as the next layer develops will cause the oscillation in reflectivity gradually to be damped as the surface becomes statistically distributed over several incomplete atomic layers. By monitoring the intensity oscillation of the RHEED pattern, we can establish that the period of the oscillation corresponds to the growth of a monolayer and therefore determine the growth rate.

#### **2-4. MBE system used in this research**

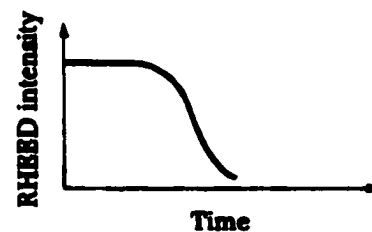
## 1. New Layer



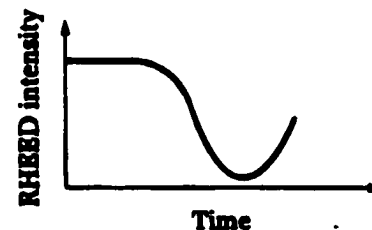
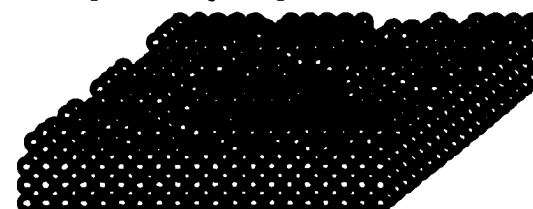
## 2. One-quarter layer deposited



## 3. One-half layer deposited



## 4. Three-quarters layer deposited



## 5. Full layer deposited

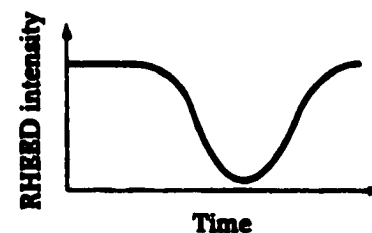
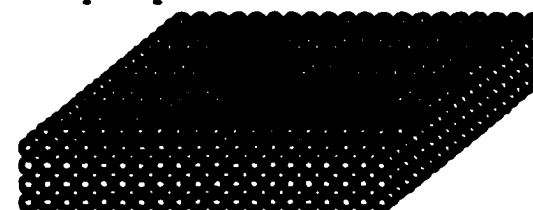


Fig. 2-4. Illustration of the RHEED oscillation process.  
 (From Harbison & Nahory, LASERS, P158, Scientific  
 American Library, 1997)

The MBE system used in this research is a Riber 2300P multi-chamber MBE system. Fig. 2-5 shows the schematic of the top view of the system. The system consists of two growth chambers UHV inter-linked via a system of transfer channel. One growth chamber is dedicated to the growth of III-V materials (III-V chamber) and the other one is dedicated to the growth of II-VI materials (II-VI chamber). There are also a loading chamber, a substrate treatment chamber, and an electron beam metallization chamber. The chambers are isolated by manually operated gate valves to insure that unintentional cross contamination between them does not occur. Each chamber is pumped by an ion pump and a titanium sublimation pump except the loading chamber which is pumped by a turbo molecular pump with a mechanical pump as the first stage and the substrate treatment chamber which is pumped by a cryopump. Besides the ion pump, the II-VI chamber and the metallization chamber are each pumped by an additional cryopump.

The loading chamber is used for loading substrates. There is a gate valve between the loading chamber and the other chambers. It allows us to vent the loading chamber by ultra pure nitrogen gas to load the substrates without affecting the vacuum in other chambers (which remain in the range of  $10^{-10}$  Torr). The substrates or samples can be transferred within the system through the transfer channel by an elaborate system of rails on which a cart

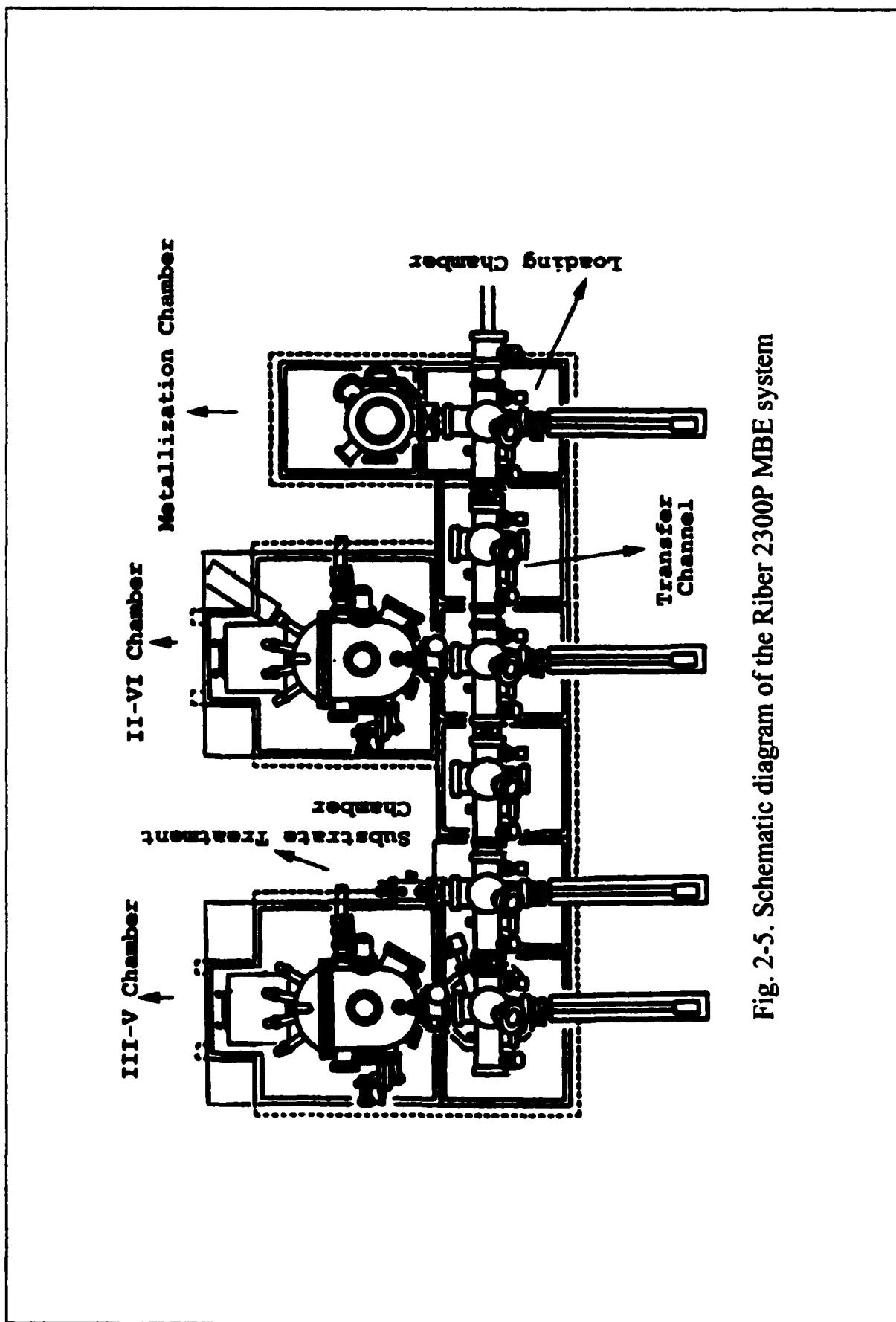


Fig. 2-5. Schematic diagram of the Riber 2300P MBE system

containing the substrate holders can move. The movement of the cart is controlled from the outside by vacuum feedthrough rotary movement knobs. The substrates may be removed or inserted into the cart and individual chambers by UHV compatible magnetically coupled transfer rods. In this way one achieves complete flexibility of sample transfer between any of the chambers in the system. The substrate treatment chamber is used to outgas the substrates before transferring them into the growth chamber. The metallization chamber is equipped with an electron beam evaporator with four pockets. Layer thickness during deposition is monitored and controlled by a quartz crystal thickness monitor.

The chambers for the growth of III-V and II-VI semiconductor materials are similar. Each is equipped with a substrate manipulator (holder, rotator, heater and temperature sensor of the substrate), RHEED, quadrupole mass spectrometer, and cryo-shrouds around the manipulator and the cells. These cryo-shrouds will have a flow of liquid nitrogen ( $\text{LN}_2$ ) through them during growth to prevent thermal interference between the source materials and to trap the residual molecules inside the chamber to maintain an UHV environment. There are 8 cells in the III-V chamber equipped for Ga, In, Al, Mn, As, InP (for P flux), Si (for n-type doping) and Be (for p-type doping), and 8 cells in the II-VI chamber for Zn, Cd, Mg, Se, Te, CdTe,  $\text{ZnCl}_2$  (for Cl

flux used for n-type doping) and a radio-frequency (RF) nitrogen cell for p-type doping. Very high purity materials from 6N to 8N are used as the source materials to ensure high purity film growth. Each time when new sources are charged, the temperatures of all the source cells are elevated to at least 100°C (except Se and ZnCl<sub>2</sub>, whose temperatures are 80°C and 60°C respectively) without introducing LN<sub>2</sub> in the cryo-shrouds for ~ 6 hours to roughly outgas the source materials. Then the cells are elevated to a temperature ~ 20°C higher than the temperature required during growth, with the LN<sub>2</sub> cooling of the chamber, for ~6 hours to insure the source materials are thoroughly outgassed before the actual growth takes place. All the pyrolytic boron nitride (PBN) crucibles used in the growth chambers are outgassed in the transfer channel or substrate treatment chamber by heating to ~ 1200°C for ~ 24 hours before being used.

The substrates are loaded through the loading chamber. After opening, the loading chamber is first pumped by an oil-free mechanical pump, then pumped by two sorption pumps to ~ 10<sup>-3</sup> Torr. After that, the turbo molecular pump system is opened and the loading chamber can be pumped down to 10<sup>-8</sup> Torr. The substrates are then transferred to the substrate treatment chamber for outgassing at 150°C for 20 min. before they are transferred to either the III-V or the II-VI chamber for epilayer growth.

## 2-5. MBE growth procedures

The MBE growth starts with a single crystalline substrate that acts as a support and a template. It needs to be *ex situ* and *in situ* cleaned before being exposed to the atomic/molecular beams. Different cleaning procedures are used for different substrates and the growth conditions for different materials also vary. In the following paragraphs, the MBE growth of CdTe, ZnSe and ZnCdMgSe will be introduced. Other specific growth details will be covered in the individual chapters.

### 2-5-1. Growth of CdTe on CdTe(211)B and CdZnTe (211)B substrates

The CdTe(211)B and Cd<sub>0.96</sub>Zn<sub>0.04</sub>Te (211)B substrates were used for the growth of CdTe. The substrates were *ex situ* cleaned by etching in 1% Br<sub>2</sub>/Methanol solution for 1 minute and then rinsed in methanol.<sup>[9]</sup> They were finally blown dried with filtered air or N<sub>2</sub> gas and mounted on a preheated moly block with indium solder. The substrates were loaded into the MBE system immediately after the *ex situ* cleaning.

The *in situ* oxide desorption of the CdTe or Cd<sub>0.96</sub>Zn<sub>0.04</sub>Te substrates was performed in the II-VI chamber by heating the substrates to ~340°C. We could see a clear “ladder” shape pattern at [0 $\bar{1}1$ ] and [ $\bar{1}11$ ] azimuth. After oxide desorption, the substrate temperature was lowered to 285°C and the CdTe growth was performed at this temperature.<sup>[9]</sup> The CdTe source beam

equivalent pressure (BEP) was around  $1.1 \times 10^{-6}$  Torr resulting in the growth rate of about  $1 \mu\text{m/hr}$ . The RHEED lines became longer and streakier after the growth was initiated and they remained streaky throughout the growth process.

### *2-5-2. Growth of ZnSe on GaAs (100) substrate*

The GaAs (100) substrates were *ex situ* cleaned by degreasing in trichloroethylene (TCE), acetone and methanol and etching in  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (4:1:1) etchant for 1 minute to remove the residual polishing damage. After being flushed with de-ionized water, an oxide layer was formed on the substrate surface to protect the fresh GaAs surface from contamination. The substrates were then In-bonded onto the moly blocks and loaded into the loading chamber in the MBE system.

The oxide desorption of the GaAs (100) substrates was performed in the III-V chamber with an As flux impinging on the surface. Prior to heating, a half-concentric circular RHEED pattern appeared indicating the presence of an amorphous oxide layer. As the temperature rose, a diffraction pattern of spots was seen. The spotty RHEED pattern became elongated into lines with the further increase of the temperature indicating a smoothing of the surface. At temperature near  $580^\circ\text{C}$ , bright RHEED patterns were seen with 2-fold reconstruction lines in the [011] azimuth and 4-fold reconstruction line

or triangular shapes in the  $[01\bar{1}]$  azimuth, indicating the end of the oxide desorption.

The growth of ZnSe on GaAs substrate usually incorporates a GaAs buffer layer to improve the GaAs surface morphology and intentionally control the surface stoichiometry to improve the initial ZnSe nucleation.<sup>[10]</sup> The GaAs buffer layer (~200nm) was grown at 580°C in the III-V chamber. Streaky (2x4) RHEED reconstruction was observed during growth. The As shutter was closed at ~500°C after growth and a final (2x4) RHEED pattern was seen indicating an As-terminated surface. The starting As-terminated GaAs surface results in less stacking fault in the subsequent ZnSe layer due to the suppression of the formation of Ga<sub>2</sub>Se<sub>3</sub> clusters in the ZnSe-GaAs interface.<sup>[11,12]</sup>

The GaAs substrates with the GaAs buffer layers were transferred quickly into the II-VI chamber for the growth of ZnSe epilayers. The contamination or damage during transfer is expected not to be severe.<sup>[13]</sup> The growth of ZnSe was performed at 250-270°C using Se/Zn BEP ratio of ~2-4. The growth rate is ~1 μm/hr.

### *2-5-3. Growth of ZnCdMgSe on InP substrate*

The InP substrates were *ex situ* cleaned in the same way as with the GaAs substrates. *In situ* oxide desorption of the InP substrates was also

performed in the III-V chamber by heating the substrates with an As flux impingement. Clear 4-fold RHEED reconstruction was seen at  $\sim 480^\circ\text{C}$ , indicating the end of the oxide desorption. InGaAs buffer layers ( $\sim 60\text{nm}$ ) lattice matched to InP were grown at  $480^\circ\text{C}$  to improve the substrate surface morphology. After that, the InP substrate together with the InGaAs buffer layers were transferred to the II-VI chamber for the growth of ZnCdMgSe alloys.<sup>[14]</sup>

The ZnCdMgSe layer was grown under Se rich conditions with a BEP ratio of the group VI to group II fluxes of  $\sim 4$ . It was initiated with a growth of a thin ZnCdSe ( $\sim 10\text{nm}$ ) buffer layer at  $170^\circ\text{C}$ . After that, the substrate temperature was raised to the optimum growth temperature of  $250\text{-}270^\circ\text{C}$ . The growth of ZnCdMgSe was performed with various Cd/Zn flux ratios and Mg cell temperatures. Different ZnCdMgSe epilayers with bandgaps ranging from  $2.18\text{eV}$  to  $\sim 3.5\text{eV}$  while still being lattice matched to the InP substrate were obtained.<sup>[14,15]</sup>

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## **CHAPTER 3**

### **Selective Area Epitaxy (SAE)**

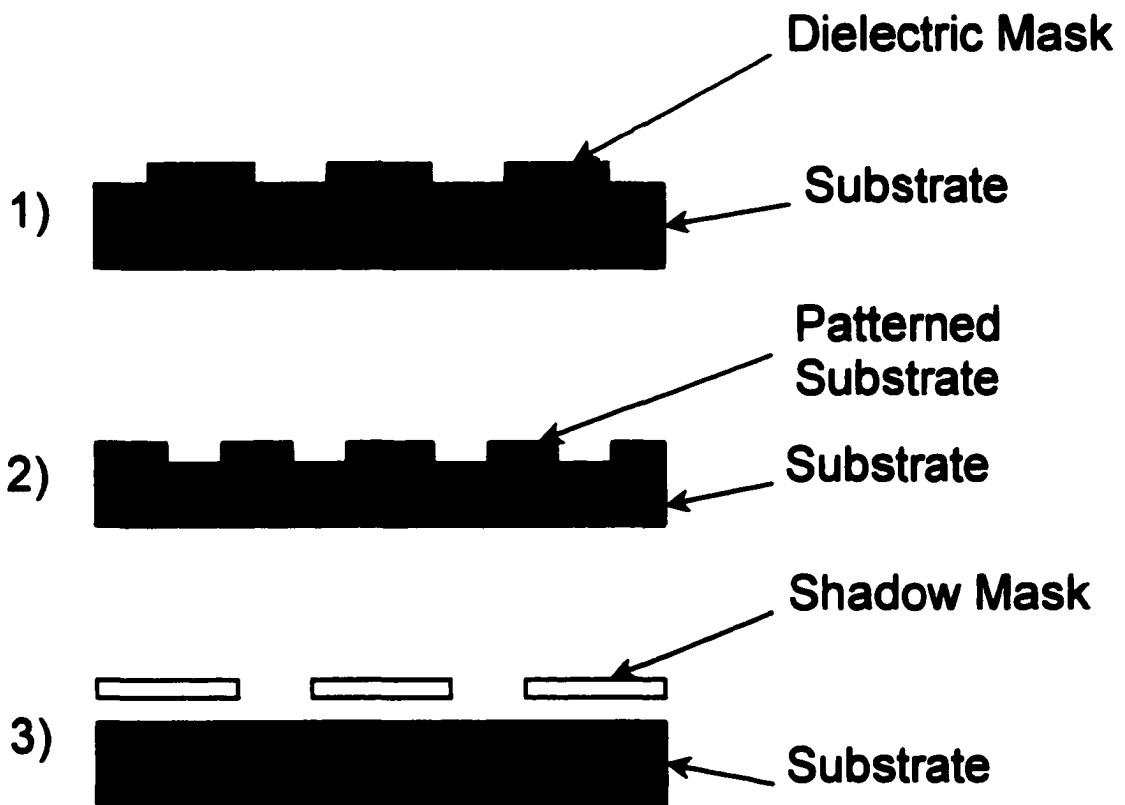
#### **3-1. Introduction**

Selective area epitaxy (SAE) is a technique of laterally defining the substrate surface and growing layers and structures over the selected substrate area. Lateral definition of the epilayer thus can be accomplished during the MBE growth process by using a variety of defining procedures.

In this chapter, I will introduce selective area epitaxy using various defining techniques. Shadow mask SAE will be introduced in detail since this is the technique used in this research. The relationship between SAE and material defect density will be briefly mentioned. The design and fabrication of the shadow masks used in this research will also be presented.

#### **3-2. Defining techniques used in the SAE**

The lateral definition of the substrate area used in the SAE can be generated in three ways: 1) by opening defined windows in a dielectric layer on the substrate photolithographically; 2) by using preferential etching of the substrate to produce self-aligned structures; and 3) by using a separate mechanical shadow mask.<sup>[1]</sup> These techniques are illustrated in Fig. 3-1.



**Fig. 3-1. Illustration of the three techniques used in the SAE.**

The dielectric mask used in the SAE growth may be a thin  $\text{SiO}_2$  film,  $\text{Si}_3\text{N}_4$  film, or a similar amorphous material that can withstand the growth temperature. The desired opening patterns are defined photolithographically. The appropriate structure is then grown over the whole substrate in the usual way. In the unmasked substrate areas (not covered by the dielectric layer) the material grows as a single crystal, but over the dielectric layer the deposit is polycrystalline. The unmasked substrate areas define the locations of the desired material. Fine pattern definition and device performance with this masking technique have been demonstrated in both III-V<sup>[2,3,4,5]</sup> and II-VI materials.<sup>[6]</sup>

Because of the collimated nature of the incident beams, MBE lends itself to the use of patterned substrates where preferentially etched mesas and troughs are formed on the substrate and mechanical shadow masking by the interposition of a mechanical shadow mask over the substrate surface that can effectively block the arrival of the molecular beams on the substrate surface.

Using selective etching and photolithographic masking, the substrate area can be laterally defined. It was found that the thickness of the epitaxial layers grown on the patterned substrates depends on the orientation of the surface on which these layers grow.<sup>[7]</sup> This lateral thickness variation results from the variation in the flux of the source beams across surfaces with

different orientations and different effective sticking coefficients associated with different crystal planes.<sup>[8,9]</sup> This feature can be utilized to achieve controllable patterning of semiconductor heterostructures<sup>[10]</sup> and has proven useful in fabricating optoelectronic devices.<sup>[9,11]</sup> It is also being increasingly used in producing quantum wire and dot structures.<sup>[12-14]</sup>

Since the use of a mechanical shadow mask is the technique adopted in this research, it is covered separately in the next section .

### **3-3. Shadow mask selective area epitaxy**

Shadow masking was originally used in the metal layer deposition to make contacts on the devices. It was first used with MBE in 1972 to grow three-dimensional dielectric waveguides for integrated optics.<sup>[23]</sup> It was performed by using a masking wire in front of the substrate surface which resulted in the blocking of the incident flux. The growth of taper-coupled  $\text{Al}_y\text{Ga}_{1-y}\text{As}$  -  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  laser structures was reported later by using a movable tantalum mask.<sup>[24]</sup> Multiple step SAE using shadow mask has been demonstrated by the growth of single crystal aluminum Schottky-barrier diodes on a GaAs substrate<sup>[25]</sup> and the fabrication of two-dimensional optical waveguides having a tapered coupler at the end.<sup>[26]</sup>

Shadow mask SAE has advantages over the other two SAE techniques. Some of them are: the simplicity of fabrication, the ease of the complete

removal of the mask and the polycrystalline deposit that grows over the mask, and the flexibility for sequential SAE growth required in more complex device structures.

Shadow masking has also been used in chemical beam epitaxy (CBE)<sup>[27]</sup>, metal-organic vapor phase epitaxy (MOVPE)<sup>[28]</sup>. A silicon shadow mask has been used by various groups<sup>[29,30]</sup>. It is more pure, rigid, and reusable than the metal mask. Different mask mounting techniques were also reported, either by modifying the manipulator design or using mechanical methods to attach the mask on the substrate.<sup>[24,29,31]</sup>

### **3-4. SAE and material defect density**

SAE using patterned substrates and oxide masking have been reported to have a defect reduction effect due to the limited growth area. It has previously been shown that lattice mismatched systems such as InGaAs/GaAs<sup>[15,16]</sup> and GaAs/Si<sup>[17,18]</sup> can be grown on patterned substrates or through post growth patterning to produce materials with lower defect densities than when the growth is performed over a large, “infinite” area. A similar effect has also been observed in the SiGe/Si system using an oxide mask.<sup>[19]</sup> The mechanism of this defect reduction effect is not well understood. It is most probably attributed to a reduced density of the sources for defects on the finite areas<sup>[15,20,21]</sup> and to the strain relaxation phenomena

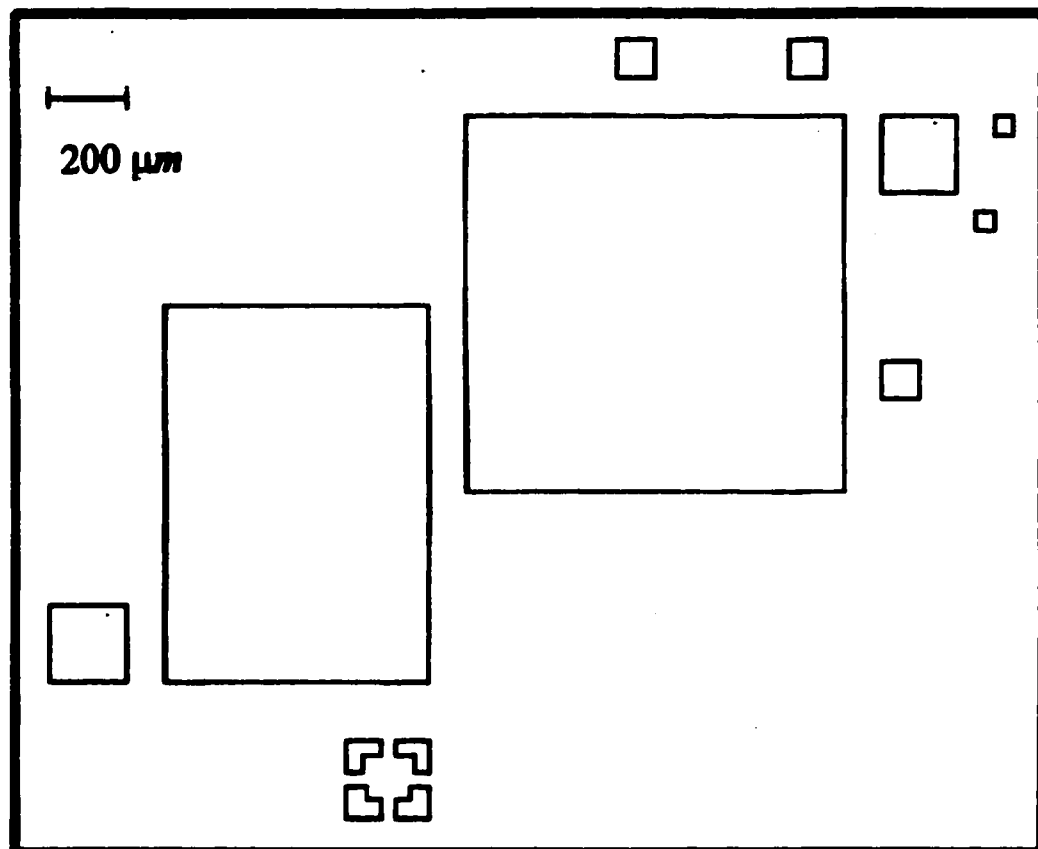
near edges when the finite substrate size is comparable to the migration length of the species on the surface.<sup>[16,22]</sup> The defect reduction effect has not been previously investigated for SAE using shadow mask.

### **3-5. Shadow masks design and fabrication**

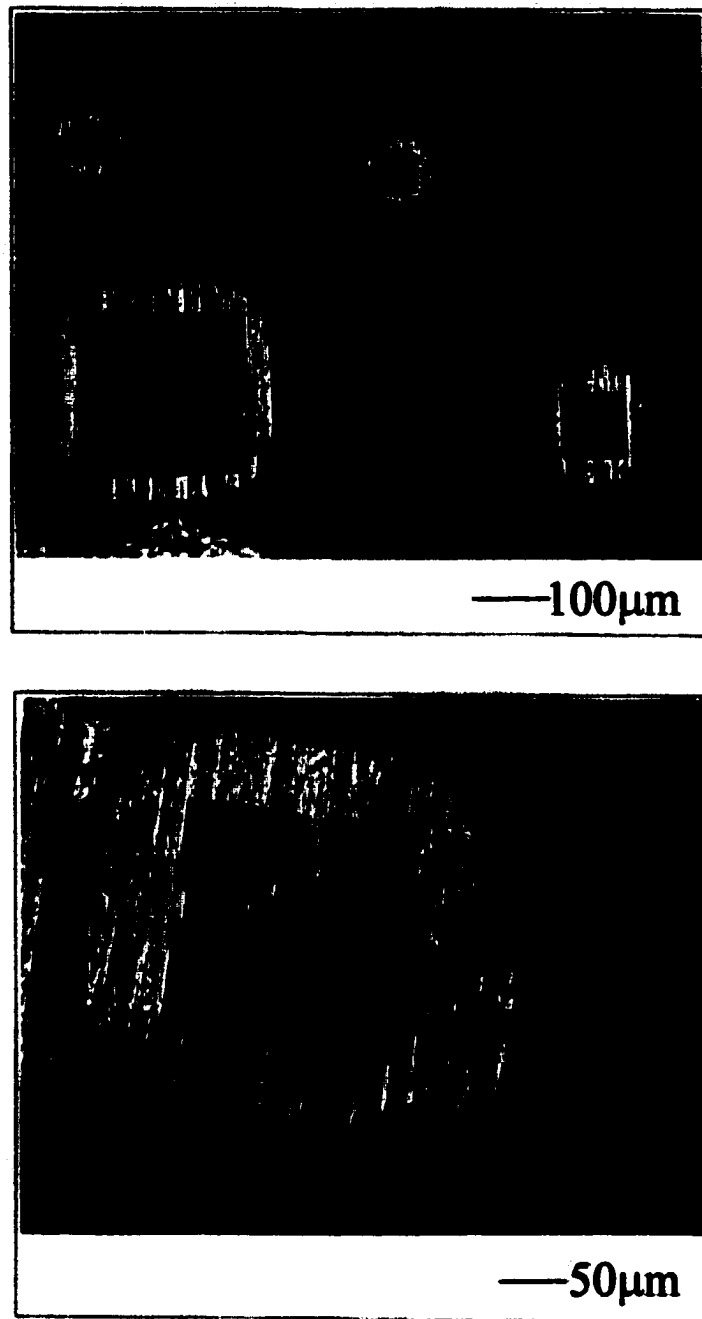
There are two kinds of mechanical shadow masks used in this research. One is made out of refractory metals: Ni, Cu and Be. The metal masks were fabricated by a company called Photo Sciences Inc. in Torrance, California. The other one is made out of the (100) silicon wafer. The silicon masks were fabricated by us in the National Nanofabrication Facility at the Penn State University using conventional photolithography and wet chemical etching.

#### ***3-5-1. Metal shadow mask***

The schematic of the mask patterns we used in the initial metal mask is shown in Fig. 3-2. It has squares, rectangles and other shapes with sizes and separations down to 50 $\mu\text{m}$  and 20 $\mu\text{m}$  respectively. The mask is 2 inches in diameter and 150 $\mu\text{m}$  thick. It is machined to have 45° tapered side walls in the window openings to reduce the mask shadowing effect that will be discussed later. Fig. 3-3 shows the optical micrographs of some typical window openings in this metal mask. The bright region surrounding the openings corresponds to the tapered side wall of the window openings.



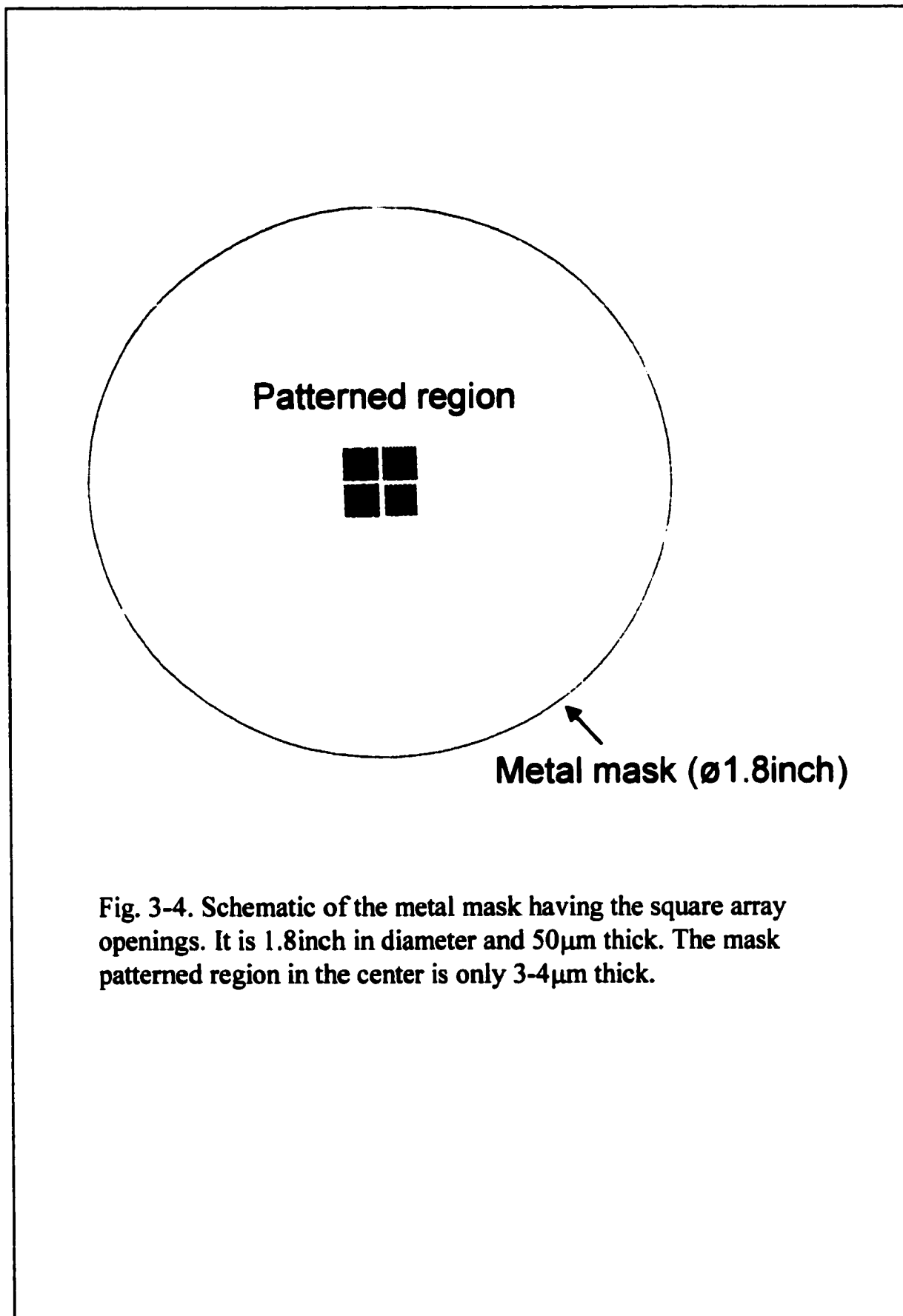
**Fig. 3-2. Schematic of the mask patterns in the initial metal mask.**



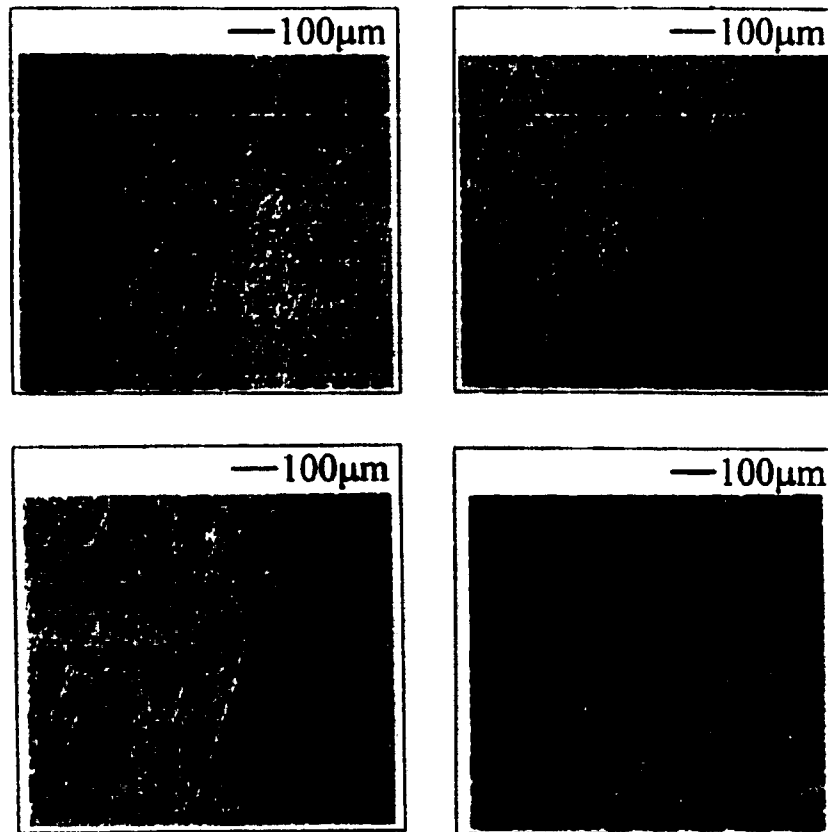
**Fig. 3-3. Nomarski micrograph of the typical window openings in the initial metal mask. The bright region corresponds to the tapered side wall.**

We also have some metal masks fabricated to have various square window arrays with sizes and separations ranging from 20, 30, 40 to 50 $\mu\text{m}$ . These feature sizes are comparable to those used in the photodetector arrays. Fig. 3-4 shows a schematic of this mask design and Fig. 3-5 is the optical micrographs of the square window arrays in the mask patterned region. This metal mask was designed to be only 50 $\mu\text{m}$  thick and the thickness in the mask patterned region was reduced to only a few microns. This was necessary because, for a 50 $\mu\text{m}$  thick mask, if we want to have 45° tapered side walls of the window openings, the separation between these openings will be at least 100 $\mu\text{m}$ . This geometric limit is schematically shown in Fig. 3-6a. Smaller separations can be achieved by using a thinner mask as shown in Fig. 3-6b. In the real mask fabrication, vertical side wall openings were made instead of tapered openings to facilitate the mask machining technique in thin (3-4 $\mu\text{m}$ ) metal plate. The vertical side wall is tolerable for a thin mask as the use of the thin mask can reduce the mask shadowing effect significantly (see chapter 5). It also allows us to achieve even smaller separations between the window openings. Fig. 3-6c illustrates the actual metal mask design using vertical openings in the thin mask patterned region.

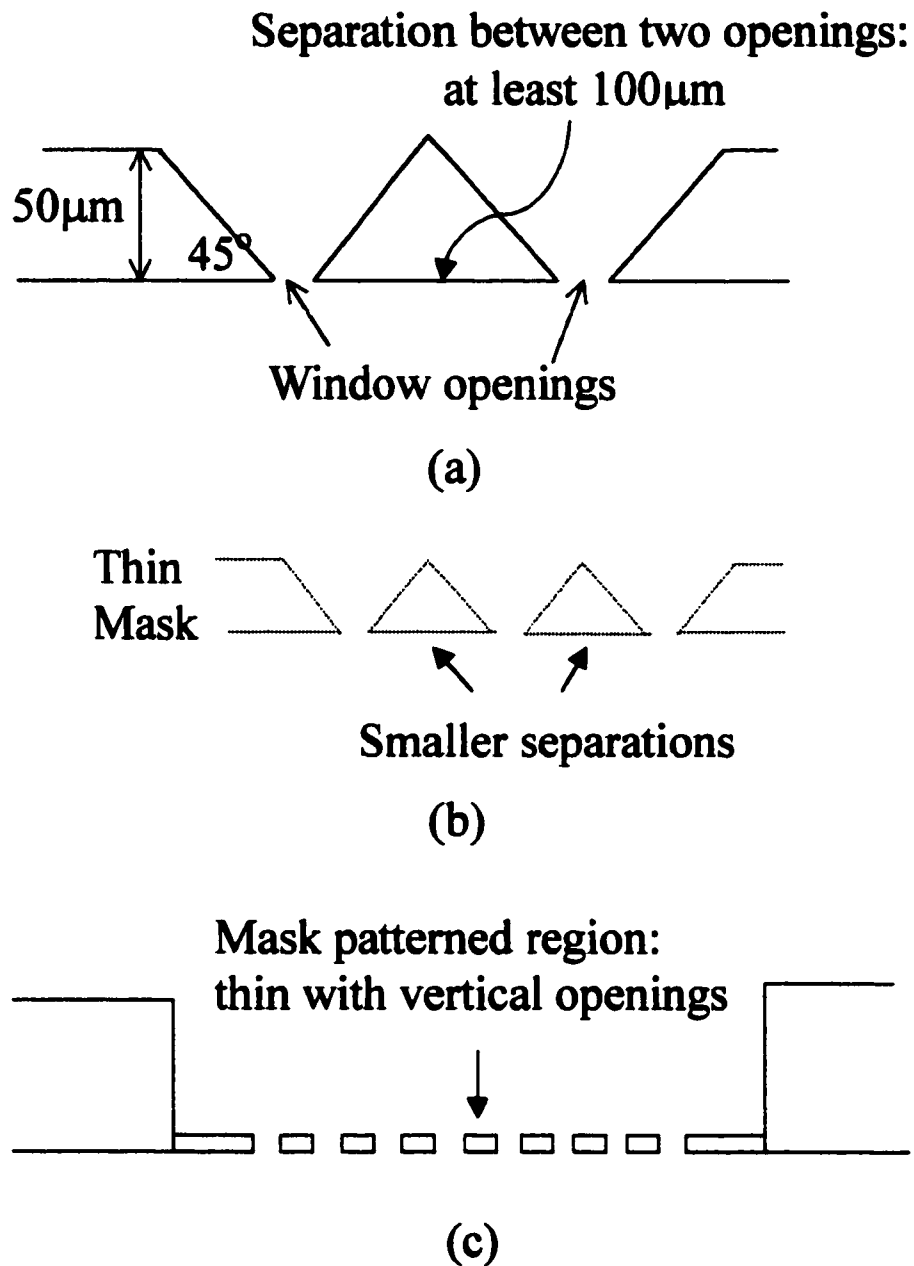
### *3-5-2. Silicon shadow mask*



**Fig. 3-4. Schematic of the metal mask having the square array openings. It is 1.8inch in diameter and 50 $\mu$ m thick. The mask patterned region in the center is only 3-4 $\mu$ m thick.**



**Fig. 3-5. Nomarski micrographs of the square window arrays in the mask patterned region with sizes and separations ranging from 20, 30, 40 to 50 $\mu$ m.**



**Fig. 3-6. a) Illustration of the large separations between the window openings required for thick mask; b) small separations achievable with thin mask; and c) the actual mask design using vertical openings in the thin mask patterned region.**

The silicon mask was fabricated from a 250 $\mu\text{m}$  thick silicon (100) wafer using conventional photolithography and wet chemical etching. The silicon wafer was first double-side coated with SiN<sub>x</sub> by Liquid Phase Chemical Vapor Deposition (LPCVD). About 5000 $\text{\AA}$  thick nitride layers were deposited during 2.5 hours at 780 $^{\circ}\text{C}$ . One side of the wafer was then spin coated with photoresist (PR1813). The mask pattern was defined by a Karl Suss MA6 mask aligner. The exposed photoresist was removed by Developer 312. Reactive ion etching (RIE) was used to etch away the nitride layer at the areas that were no longer covered by photoresist so that regions of bare silicon were exposed. Before using KOH chemical etching, the remaining photoresist was removed by acetone. The wet etching of the silicon not covered by the nitride layer by KOH was done at  $\sim 80^{\circ}\text{C}$  and it took about 8 hours to etch through holes in the 250 $\mu\text{m}$  thick silicon wafer. The remaining SiN<sub>x</sub> was etched away by HF before use. Fig. 3-7 lists the procedures for the fabrication of the silicon mask.

The silicon shadow mask consists of stripe and square openings with sizes ranging from 15 to 60  $\mu\text{m}$  at the narrow opening side placed toward the substrate. Fig. 3-8a shows the SEM micrograph of several stripe and square openings viewed from the back narrow opening side. Fig. 3-8b is the

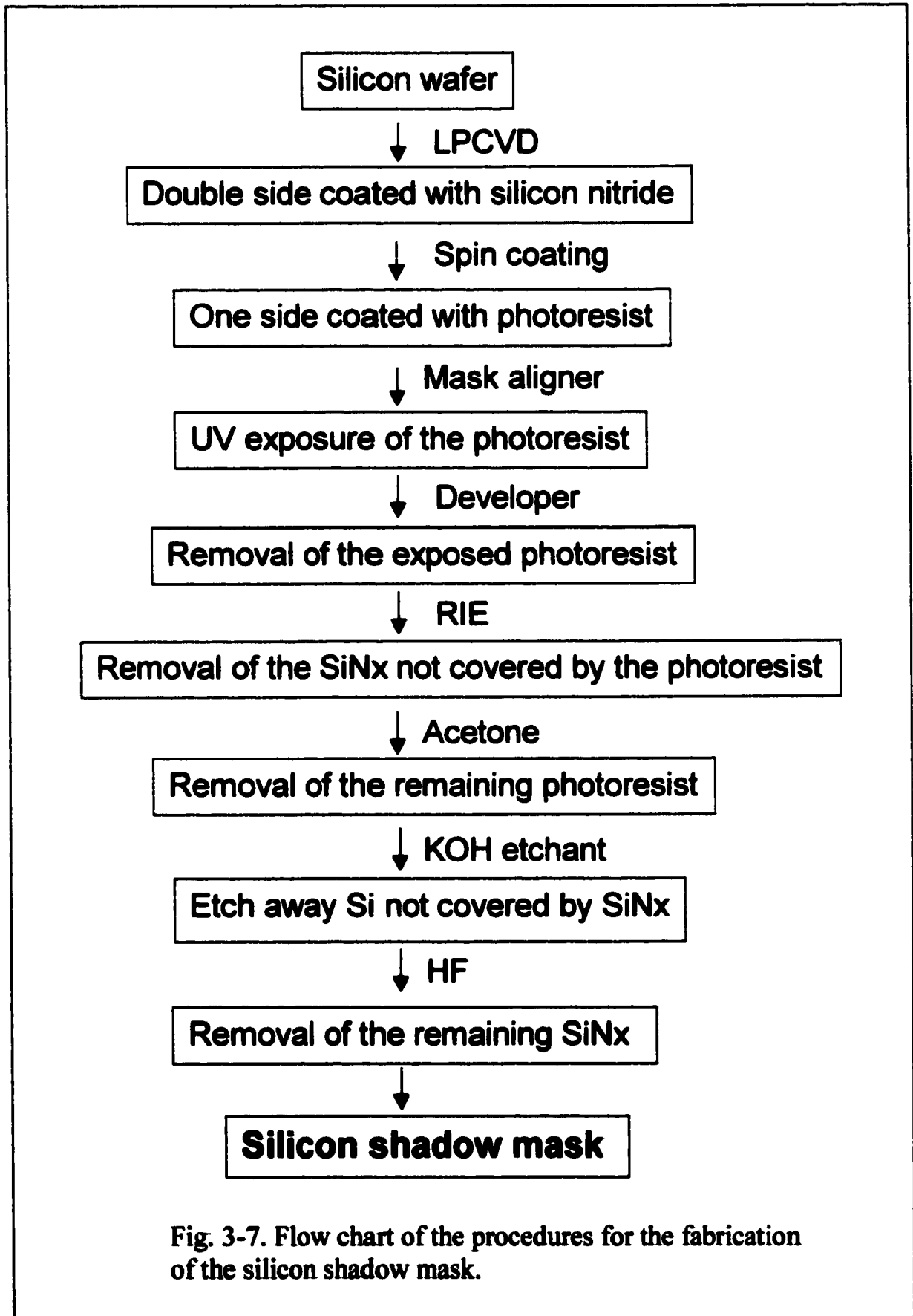
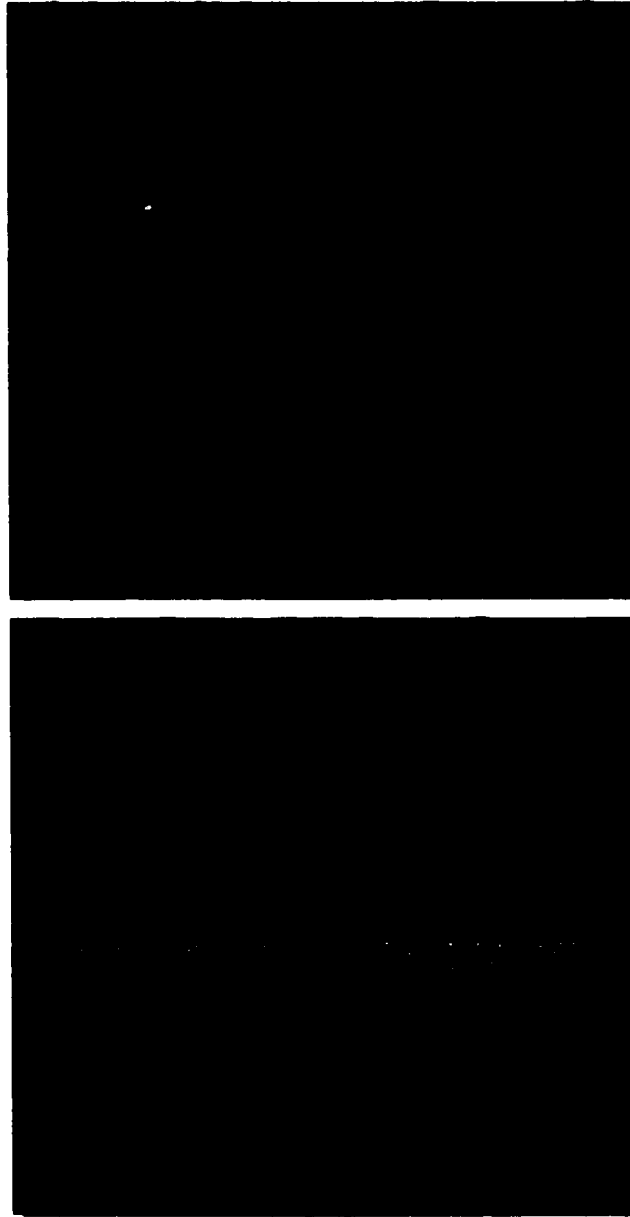


Fig. 3-7. Flow chart of the procedures for the fabrication of the silicon shadow mask.



**Fig. 3-8. SEM micrographs of the patterns in the silicon shadow mask:**  
a) Viewed from the back narrowing opening side;  
b) Viewed from the front wide opening side.

corresponding SEM micrograph viewed from the top wide opening side revealing the well defined tapered side wall (Si (111) plane) which can reduce the mask shadowing effect. The silicon mask was used in the growth of ZnSe based materials and excellent results were obtained.

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# **CHAPTER 4**

## **Material Characterization Techniques**

### **4-1. Introduction**

After the MBE growth, the samples were taken out of the growth chambers and removed from the moly blocks. The sample surface and pattern definition were evaluated by Nomarski optical microscopy, scanning electron microscopy (SEM) and atomic force microscopy (AFM). The thickness of the flat epilayers was measured by Philtec's radial sectioning instrument. The thickness of the patterned epilayers was assessed using surface profilometry. The optical properties of the samples, from which we can usually obtain their bandgap and material quality, were measured by photoluminescence (PL). The samples' crystalline quality and their lattice mismatch to the substrate were assessed using single and double crystal x-ray diffraction. Etch pit density (EPD) measurements were performed to characterize the epilayer defect density. Secondary ion mass spectroscopy (SIMS) and adhesion test were performed to measure the interface contamination and metal adhesion properties on the semiconductors.

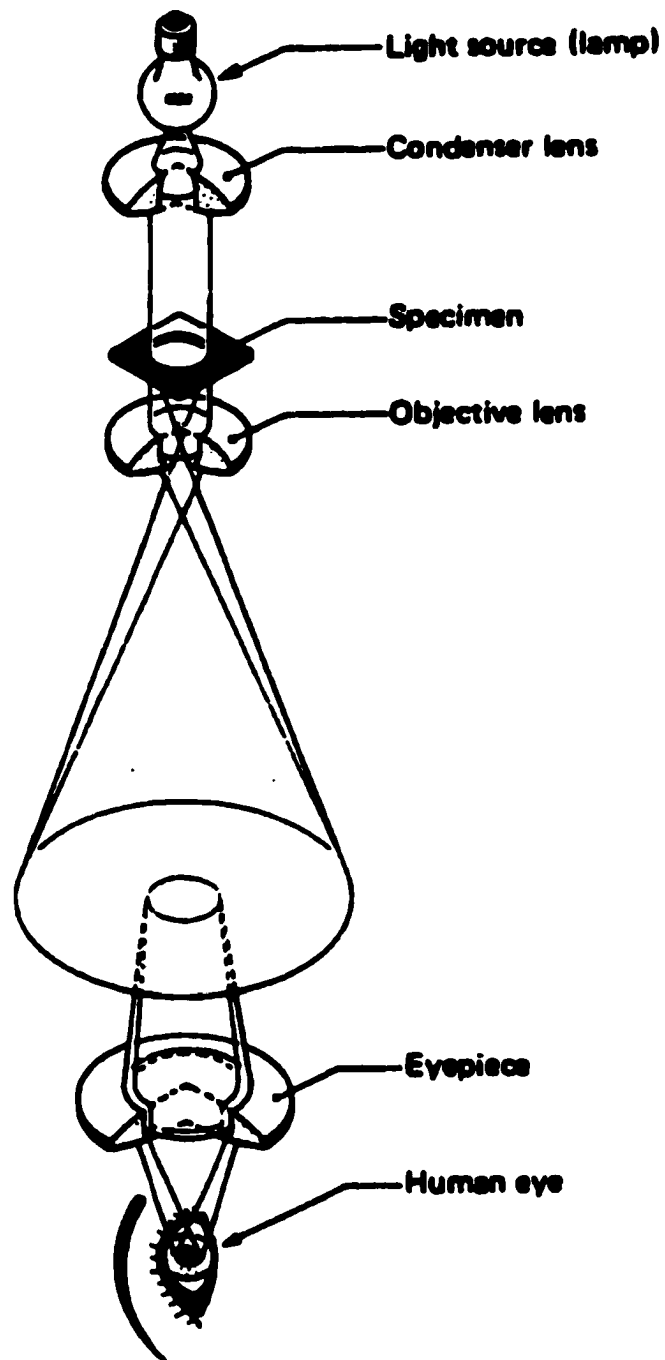
### **4-2. Nomarski optical microscopy**

A Leitz LABORLUX S optical microscope was used in this research. As with basic optical microscopes, it consists of a halogen lamp as the light source, a condenser lens to focus the light, a specimen stage, an objective lens system (four interchangeable lenses with magnifications of 10x, 20x, 50x, and 100x), a projective lens (eyepiece lens, 10x), and a dual knob for coarse and fine focusing of the microscope images. The microscope also has a photographic camera system attached to take pictures of the images. Fig. 4-1 shows the schematic of the optical microscope.

The microscope can be operated in three contrast modes: bright field, dark field and Nomarski differential interference contrast (DIC). The Nomarski DIC mode is the one we usually employ and that is why we call it Nomarski optical microscopy. An interference contrast polarizer is used in this case. It can form high-contrast images of thin specimens due to the rate change of the optical path across the object in the direction of shear.<sup>[1,2]</sup>

### **4-3. Scanning electron microscopy (SEM)**

In a scanning electron microscope, a short wavelength electron beam is used as the illumination source. The secondary reflected electrons from the individual specimen positions can be collected through rapid scanning, forming an image on the screen. The scanning electron microscope also consists of a condenser lens and a objective lens, as with the optical



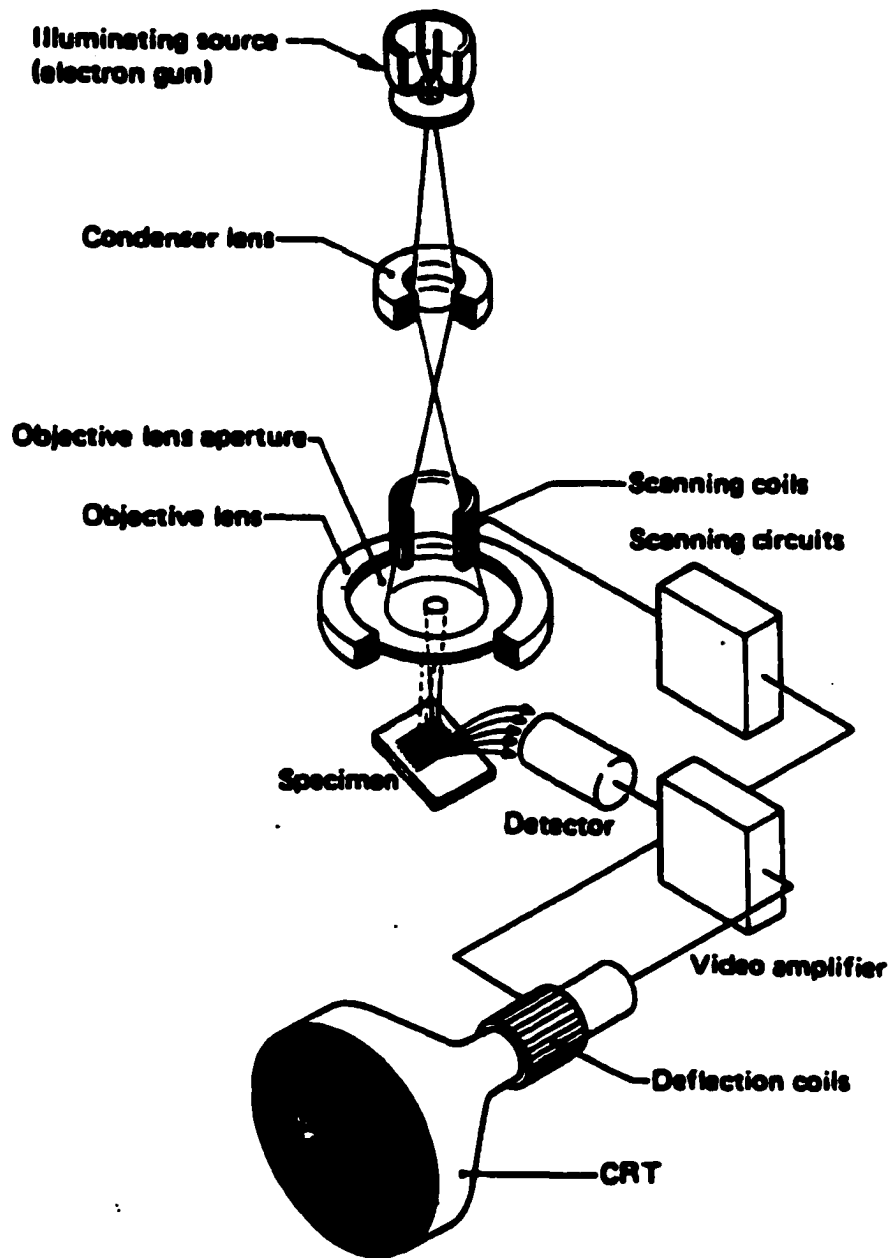
**Fig. 4-1. Schematic of the optical microscope.**  
(From *Light and Electron Microscopy*, Slayter and Slayter, Cambridge University Press, 1992)

microscope. But instead of being constructed from a material medium, the lenses are electromagnetic fields able to interact with the electron beams and produce a magnified view of the specimen. Fig. 4-2 shows the schematic of the SEM.

A JEOL JSM-6301F scanning microscope was used in this research. It employs a cold-cathode field emission electron gun with acceleration voltage from 0.5 to 30 KV as source and a scintillator as detector. The base pressure in the electron gun chamber is in the  $10^{-7}$  Pa range and the specimen chamber is in the  $10^{-4}$  Pa range. The specimen exchange uses a loadlock to maintain good vacuum in the specimen chamber.

#### **4-4. Atomic force microscopy (AFM)**

Atomic force microscopy is a powerful tool for the determination of the structural properties of material surfaces down to the atomic level. Unlike scanning tunneling microscopy, it is capable of topographically imaging both insulating and conducting layers. The AFM records interatomic forces between the apex of a tip and the atoms in a sample as the tip is scanned over the surface of the sample. In contact mode, the tip actually touches the sample so that the tip can trace over the individual atoms. The AFM tip should be sharp and the tracking force should be weak so that the tip will not damage the surface of the sample. The AFM can also be operated in a tapping mode.



**Fig. 4-2. Schematic of the scanning electron microscope.**  
 (From *Light and Electron Microscopy*, Slayter and Slayter, Cambridge University Press, 1992)

The force between the sample and the tip placed in proximity to the surface of the sample is measured. A feedback system then prevents the tip from touching (and damaging) the sample by keeping this force at a constant level. When the tip is moved sideways it will follow the surface contours.<sup>[3]</sup>

A Digital Instrument MultiMode scanning probe microscope (SPM) system was used in this research. Fig. 4-3 shows the principle operation of the AFM. The AFM system is comprised of two main components: 1) the scanner; 2) the AFM detection system. The scanner houses the piezoelectric transducer. The piezo element physically moves the sample in the X, Y and Z directions. The tip is attached to a cantilevered spring. The position of the tip or the small tacking force between the tip and the sample are recorded by measuring the deflections of the spring through measuring the deflection of a laser beam from a mirror mounted on the spring. The laser beam is finally reflected into a photodetector and an electrical signal which varies rapidly with the laser deflection is generated from the difference between the photodiode segment. A feedback circuit controls the voltage applied to the z piezoelectric element so that the electrical signal is maintained constant as the tip is scanned across the sample surface with the x and y piezos in the case of the tapping mode.

#### **4-5. Surface profilometry**

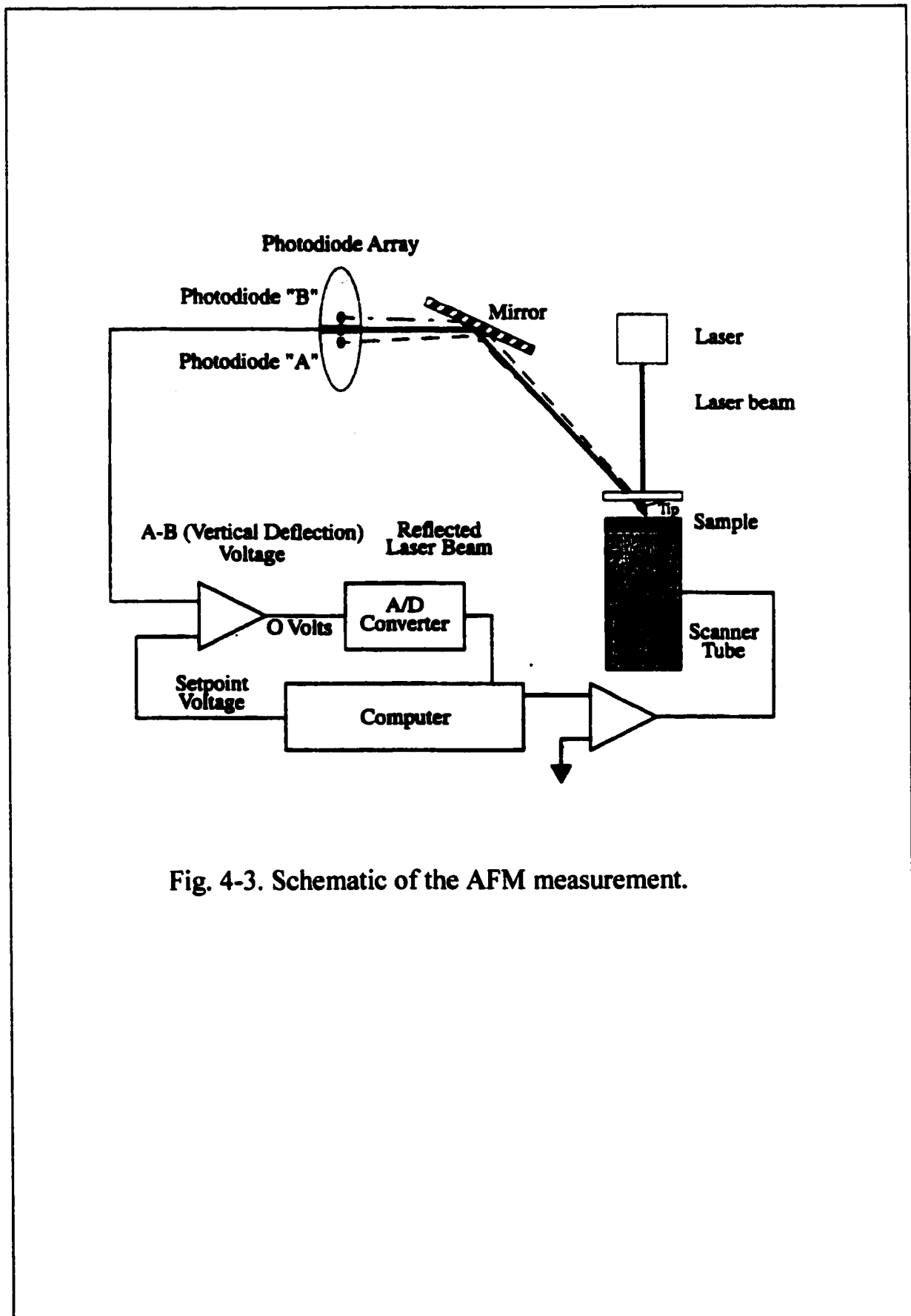
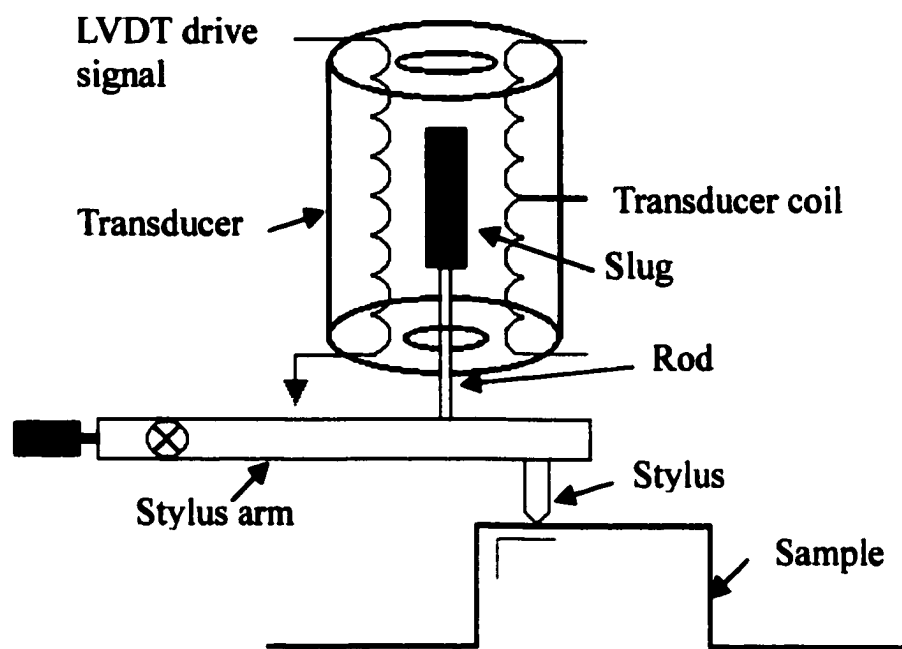


Fig. 4-3. Schematic of the AFM measurement.

An alpha-step 200 surface profilometer was used in this research for tracing the surface profiles of the patterned epilayers grown by shadow mask SAE. It operates by moving a stylus arm assembly from the center position to either the left or the right to measure the sample surface. The stylus arm assembly uses a three-position pivot to allow friction free vertical motion as it moves across the sample being measured. The arm is glued to the center pivot, and the two outside sections are glued to a bracket surrounding the stylus arm. The bracket is connected to a bolt that is then used to align the arm and set the stylus force. The stylus motion is measured by means of a transducer. Fig. 4-4 illustrates the surface profiler measurement and measurement transducer. Either a clear quartz rod or a black graphite rod is attached to the stylus arm. This rod isolates the slug of the transducer so that even the slightest vertical motion of the stylus arm can be detected by the transducer. When the slug is in the exact center of the transducer (null position), the needle in the measurement display should also be in the center. The measured linear voltage differential drive (LVDT) signal goes to the computer control unit for display, calibration and leveling.

#### **4-6. Philtec sectioning thickness measurement**

The basic idea of using Philtec's radial sectioning machine to make thickness measurement is to use a spindle with known radius to make a



**Fig. 4-4. Schematic of the surface profile measurement And measurement transducer.**

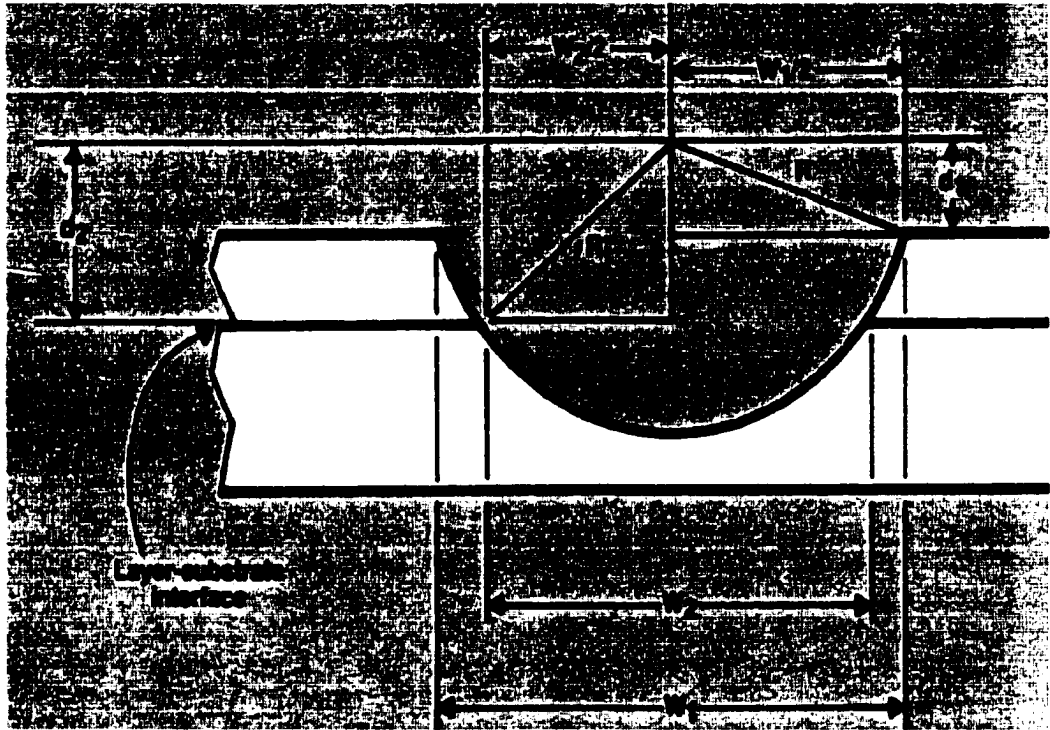
groove on the surface in order to amplify the thickness of the epilayer. Fig. 4-5 shows the cross section of the groove, where  $R$  is the radius of the spindle,  $W_1$  is the width of the cylindrical section,  $W_2$  is the width of the section at the level of the layer interface and  $X_t$  is the thickness of the epilayer.  $W_1$  and  $W_2$  can be measured using microscopy. Mathematically, the layer thickness is the difference in the heights of two triangles having the groove radius ( $R$ ) as the common hypotenuse. So the epilayer thickness,  $X_t$ , is given by:

$$X_t = [R^2 - (W_2/2)^2]^{1/2} - [R^2 - (W_1/2)^2]^{1/2}$$

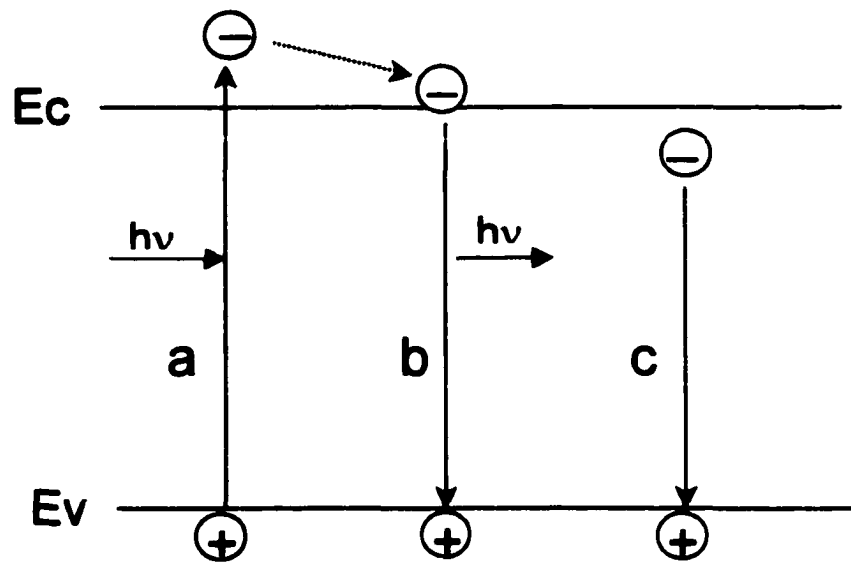
This thickness measurement method has relatively large error, in the range of 10%.

#### **4-7. Photoluminescence (PL)**

Photoluminescence is optical radiation resulting from excitation to a non-equilibrium state by absorption of photons. It can be used to identify bandgap, quality and band structure of the semiconductors.<sup>[4]</sup> Fig. 4-6 shows a simple schematic of the PL process. The electrons are promoted to the conduction band from the valence band by absorption of light which creates the electron-hole pairs. The electron-hole pairs may recombine radiatively by emitting light with energy equivalent to the bandgap energy between the conduction band and valence band. Impurities give rise to states within the bandgap which may bind electrons, holes or excitons by Coulombic



**Fig. 4-5. The principle of the thickness measurement using Philtec's radial sectioning machine.**



- a: photo-excitation**
- b: bandgap emission**
- c: impurity or defect emission**

**Fig. 4-6. Illustration of the PL process.**

interaction. The recombination involving such bound carriers results in impurity or defect related luminescence. In this way the material properties and quality can be assessed.

There are three PL systems used in this research. The conventional PL setup installed in our lab is illustrated in Fig. 4-7. The samples are mounted on the cold finger of a Janis cryogenic system. The system is pumped to  $\sim 10^{-5}$  Torr before being cooled down to 5.8 K using liquid helium or 78 K using liquid nitrogen. The temperature of the cold finger can be controlled between 5.8 K to 300 K by using a heater installed on the back of the cold finger. A He-Cd laser with the emission wavelength of 325 nm is used as the excitation source. The laser beam passes through a chopper and is focused to a small spot (tens of microns) by optical lenses before reaching the sample. The luminescence from the sample is collected by lenses and converted to a collimated beam. The collimated beam is focused to a spot on the first slit of the SPEX 1680-B spectrometer. The beams that pass through the spectrometer are detected by a photomultiplier tube (PMT) and are converted to electrical signals. The signals are then fed to a lock-in amplifier and finally sent to the computer to be collected and analyzed.

Micro-PL was also used to measure the photoluminescence from the finite-sized patterned epilayers grown by SAE. It was done using a triple-

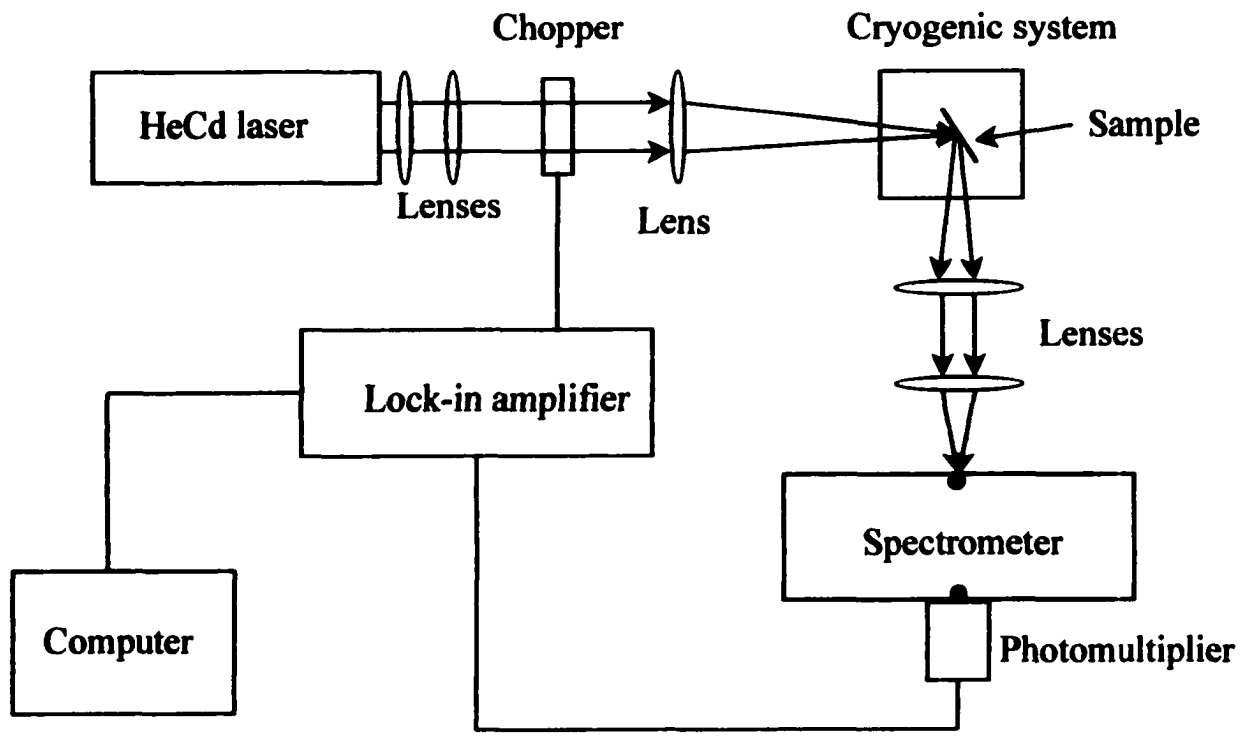


Fig. 4-7. Schematic of the conventional PL setup.

grating micro-Raman/PL spectrometer (JY-Model T64000, in Brooklyn College). Fig. 4-8 shows the schematic of the micro-PL. The Argon ion laser is focused into a small size of a few microns by optical lenses and then excites the sample placed under a microscope. The excitation position, spot size and sample surface morphology are monitored by a video camera monitor attached to the microscope. The signals are detected in a backscattering geometry by a PMT detector or charge coupled device (CCD) detector.

The third PL setup (in Hunter College) is able to obtain PL images with an optical multi-channel analyzer (OMA) which consists of a grating spectrograph equipped with a 256 x 1024 element CCD detector array. In this case a frequency-tripled Nd:YAG laser is used for excitation. The CCD detector array can capture the PL signal from individually sampled region simultaneously therefore spatially resolved PL can be obtained. The spatial resolution can be expanded by magnifying the region sampled by the CCD detector using the magnification lenses.

#### **4-8. X-ray diffraction**

X-ray diffraction is an important technique for characterizing semiconductor materials. It can reveal information such as lattice structure, lattice constant, layer quality and the embedded strain.

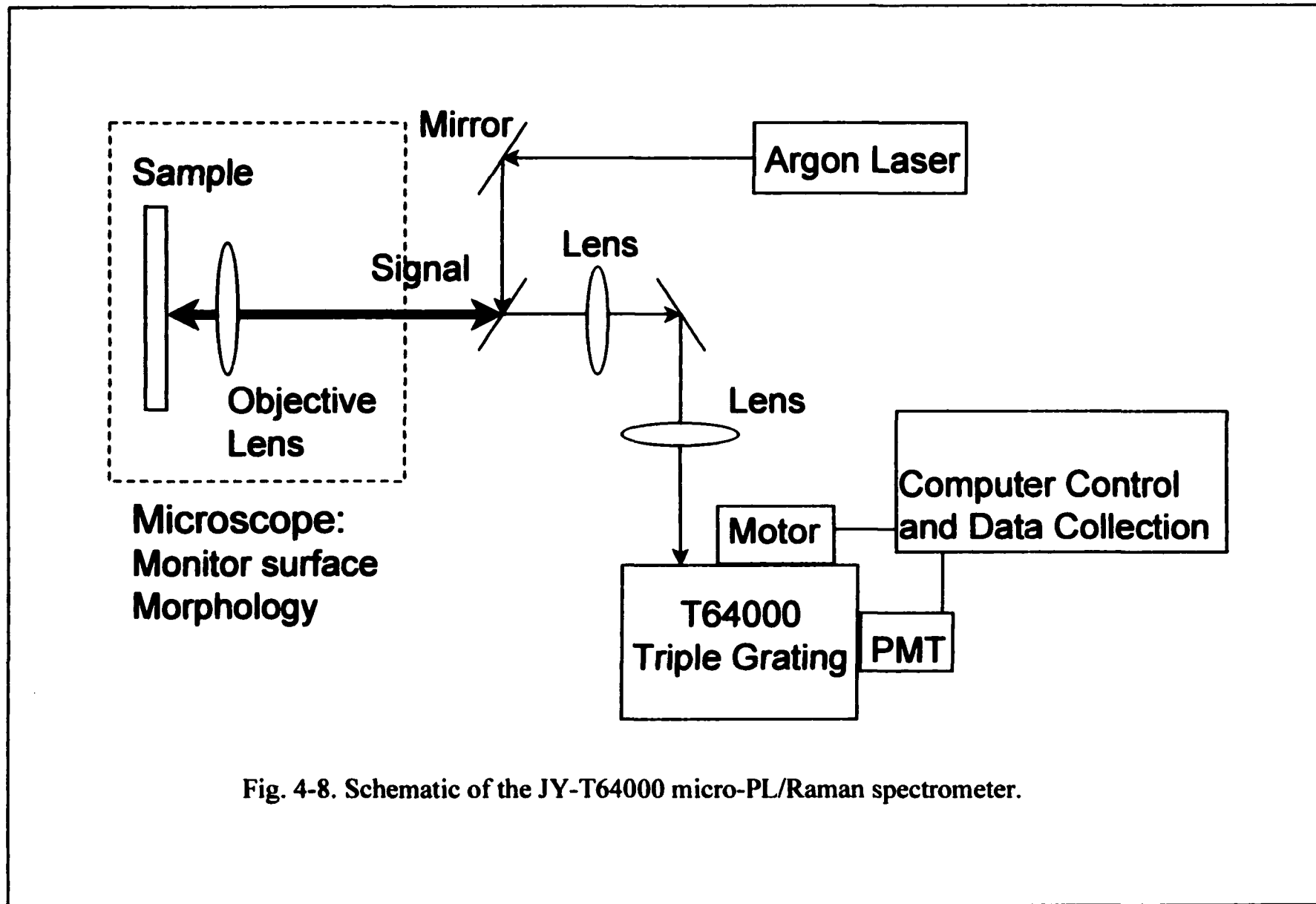


Fig. 4-8. Schematic of the JY-T64000 micro-PL/Raman spectrometer.

The schematic of the x-ray diffraction system used in this research is shown in Fig. 4-9. It consists of an x-ray source, a single crystal x-ray diffraction system shown on the right (SCXRD) manufactured by RIGAKU and a double crystal x-ray diffraction system shown on the left (DCXRD) manufactured by Blake Industries, Inc. In both cases, the rotation of the sample holder will change the incident angle  $\omega$  while rotation of the goniometer will change  $2\theta$ .

In SCXRD, only one crystal (the sample) is used. The incident x-ray beam contains both  $\text{Cu } K_{\alpha 1}$  and  $\text{Cu } K_{\alpha 2}$  lines. Therefore in the diffraction each layer has two peaks corresponding to  $\text{Cu } K_{\alpha 1}$  and  $\text{Cu } K_{\alpha 2}$ . Usually the intensity of the peak corresponding to  $\text{Cu } K_{\alpha 1}$  is twice that of the peak corresponding to  $\text{Cu } K_{\alpha 2}$ . Because the beam has a broad band of wavelengths, the diffraction peaks are usually broad. In single crystal x-ray measurements, we usually use  $\theta - 2\theta$  coupled mode, which means that the  $\omega$  and  $2\theta$  are moving simultaneously and  $\omega$  is always half of  $2\theta$ . In the practical measurement, the back of the sample has indium and it is very hard to mount the sample exactly parallel to the sample holder. To make sure the  $\omega$  and  $2\theta$  are coupled, we usually first fix the  $2\theta$  and rotate the  $\omega$  around  $\theta$  (referred to as rocking curve). The  $\omega$  value corresponding to the peak is then

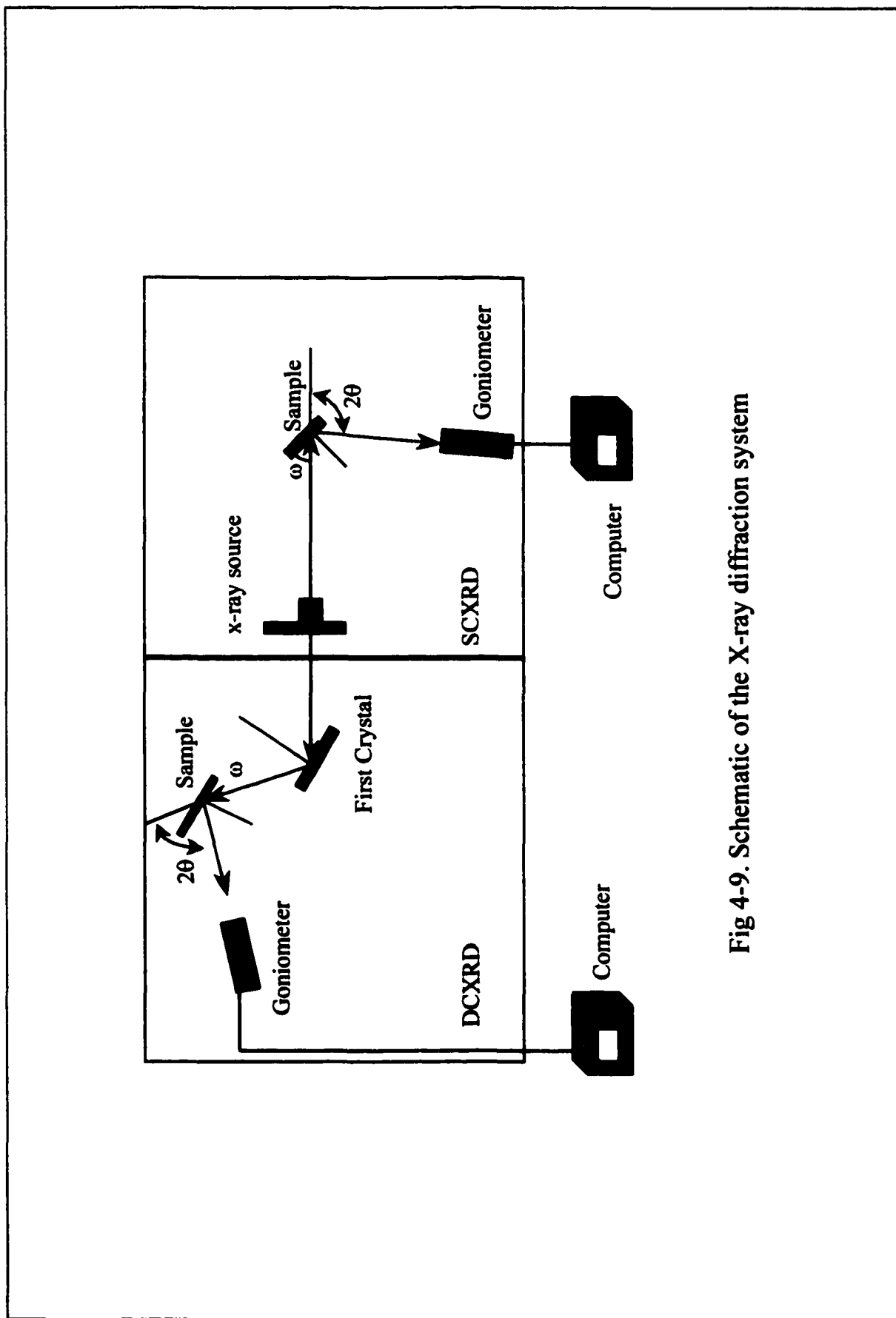


Fig 4-9. Schematic of the X-ray diffraction system

searched and adjusted to be  $\theta$ . We then set the scan mode as the  $\theta - 2\theta$  couple mode and measure the diffraction scan. The SCXRD is suitable for measuring epilayers having relatively large lattice-mismatch to the substrate. It is suitable for establishing the material crystalline structure as well.

In DCXRD, a first crystal [(100) Ge in our system] is used to separate the various wavelengths of the incident x-ray beam in order to narrow the x-ray band before the x-ray beam reaches the sample. The incident x-ray beam is therefore more monochromatic than SCXRD and has only the  $\text{Cu } K_{\alpha 1}$  line. The sample under measurement is the second crystal. The rocking curve is usually measured for the double crystal x-ray, that is, the  $2\theta$  is fixed and the  $\omega$  is varied around  $\theta$ . This method is good for measuring epilayers having small lattice-mismatch to the substrate and evaluating the layer quality based on the full width at half maximum (FWHM) of the diffraction peaks.

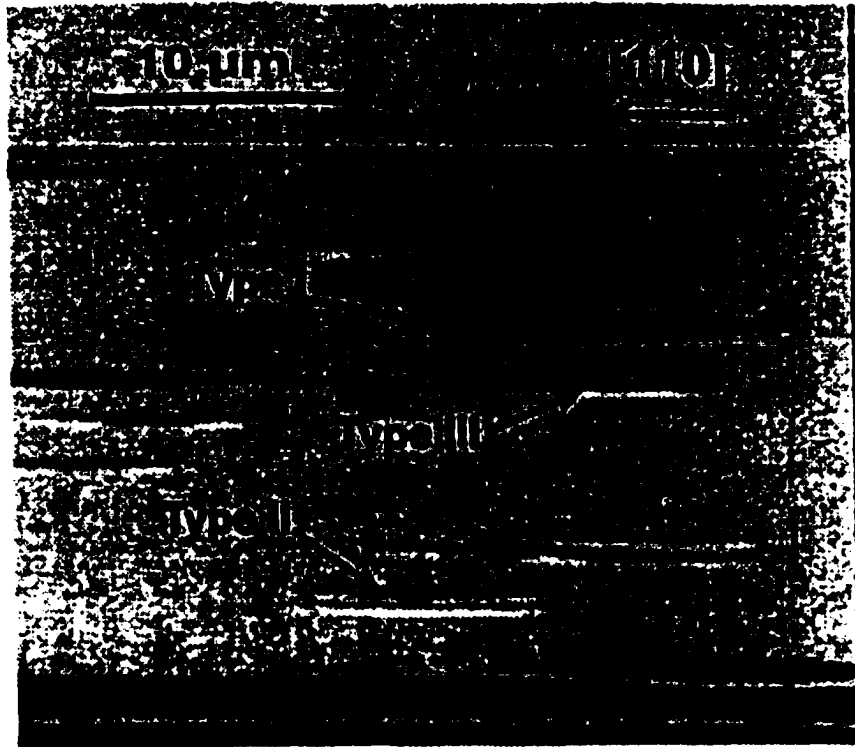
#### **4-9. Etch pit density measurement**

There are a number of methods for characterizing the defect density and defect distribution in a crystal. They include transmission electron microscopy (TEM), cathodoluminescence (CL), electron beam induced current imaging (EBIC), x-ray topography, etch pit density (EPD)

measurement, etc. Among these, the EPD measurement using chemical etching is a simple and convenient one. It is typically useful when relatively low defect density ( $<10^6 \text{ cm}^{-2}$ ) are expected. The chemical reaction velocity with some etchants around the defects can be faster than that of perfect crystal therefore etch pits are formed in the vicinity of defects. Various etchants have been developed to selectively etch defects in semiconductor materials.

In this research, dilute  $\text{Br}_2/\text{Methanol}$  solution ( $\sim 1\%$ ) was used to reveal defects in the ZnSe epilayers. There are three types of etch pits formed in the etched ZnSe epilayers corresponding to defects of different origins (Fig. 4-10).<sup>[8,9]</sup> Type I etch pits have an elongated shape and their origin can be the chemical reaction at a pair of narrowly separated Shockley partial dislocations. Type II etch pits show an internal structure of two parallel pits and they are ascribed to paired Frank type stacking faults. The third class of singular etch pits (type III) can be attributed to the presence of a single stacking fault or it can be interpreted as the etch pits on a perfect dislocation. The etching rate is  $\sim 20\text{nm}/\text{sec}$  at room temperature.

Everson etchant which consists of 48% HF,  $\text{HNO}_3$  and Lactic acid in a ratio of 1:4:25 is used to reveal the defects in the CdTe epilayers.<sup>[10]</sup> The etch



**Fig. 4-10. SEM micrograph of the three different types of etch pits formed on the ZnSe based layer.**

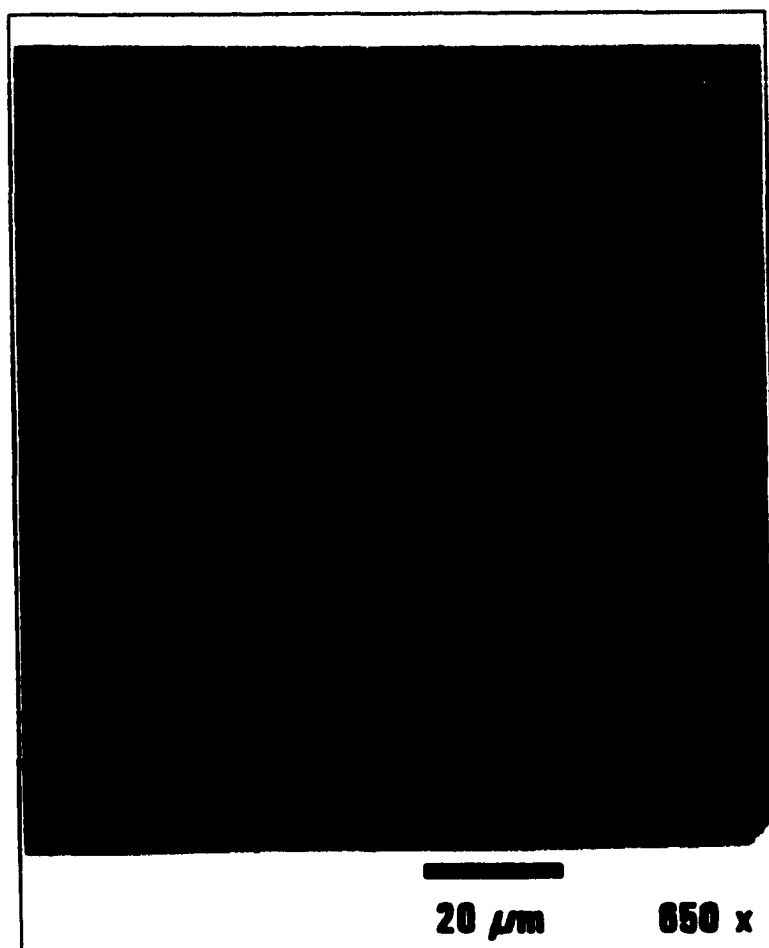
**(From F. Fischer, M. Keller, T. Gerhard, T. Behr, T. Litz, H.J. Lugauer, M. Keim, G. Reuscher, T. Baron, A. Waag and G. Landwehr, J. Appl. Phys. 84(3), 1650 (1998))**

produces elongated triangular pits in the (211)B face of CdTe as shown in Fig. 4-11. The etching rate is ~ 40nm/sec at room temperature.

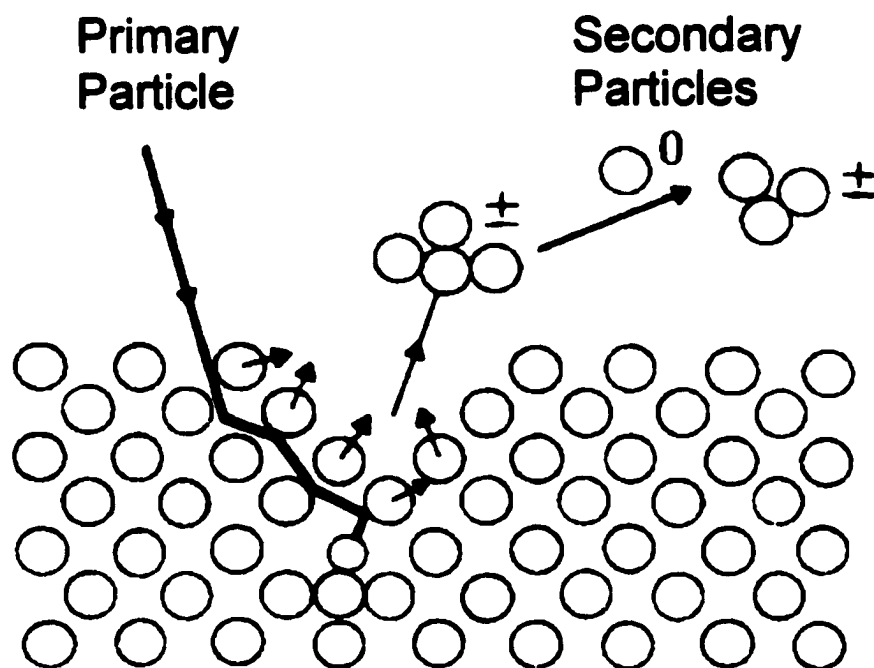
#### **4-10. Secondary ion mass spectroscopy (SIMS)**

Secondary ion mass spectroscopy is a mass spectroscopy of ionized particles that are emitted when a surface, usually a solid, is bombarded by energetic primary particles.<sup>[5]</sup> The primary particles may be electrons, ions, neutrals, or photons. The emitted (so-called “secondary”) particles will be electrons, neutral species, atoms and molecules etc. Fig. 4-12 shows a schematic diagram of the SIMS phenomenon indicating the collision of the primary particles with a solid surface and the emission of the secondary particles. It is the secondary ions that are detected and analyzed by a mass spectrometer. SIMS provides a mass spectrum of a surface and enables a detailed chemical analysis of the surface of a solid to be performed.

The SIMS measurements carried out in this research were performed using an Atomika 3000-30 quadrupole ion microprobe (Fig. 4-13). The primary  $\text{Ar}^+$  ion beam is created through electron bombardment. It is extracted and accelerated by electromagnetic lens. The ion beam can be focused and x-y deflected to meet the required positioning or raster scanning. A mass-energy filter is included to remove contaminant ions. The neutral particles are separated by deviating the ion beam by a few degrees. The ion



**Fig. 4-11. Optical micrograph of the etch pits formed on the (211)B CdTe using Everson etchant. (From W.J. Everson, C.K. Ard, J.L. Sepich, B.E. Dean, G.T. Neugebauer and H.F. Schaake, *J. Electron. Mater.* 24(5), 505 (1995))**



**Fig. 4-12. Schematic diagram of the SIMS phenomenon. The sample surface is bombarded by the primary particles and the secondary particles emit.**  
(From *Secondary Ion Mass Spectroscopy, P2*, Vickerman, Brown and Reed, Oxford Science Publications, 1989)

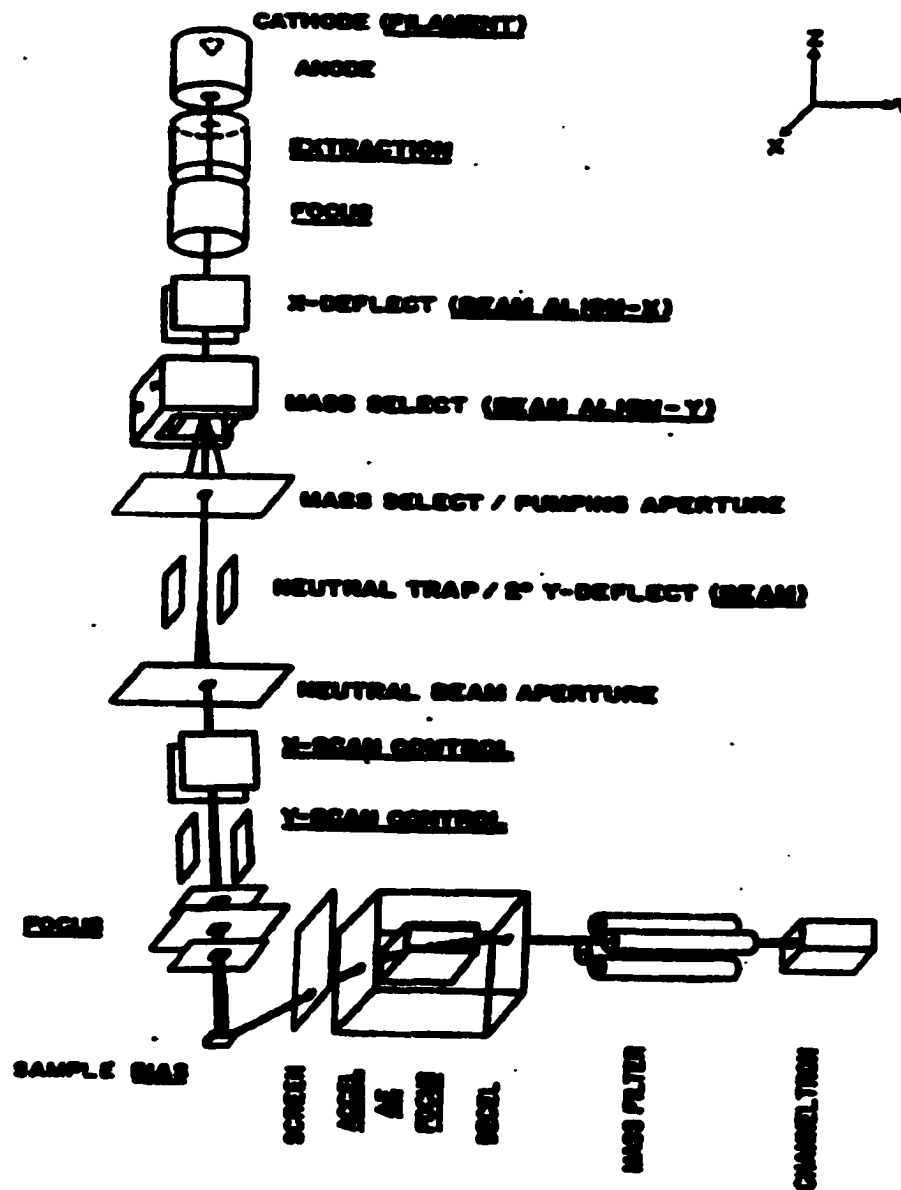


Fig. 4-13. Schematic of the Atomika 3000-30 SIMS system.

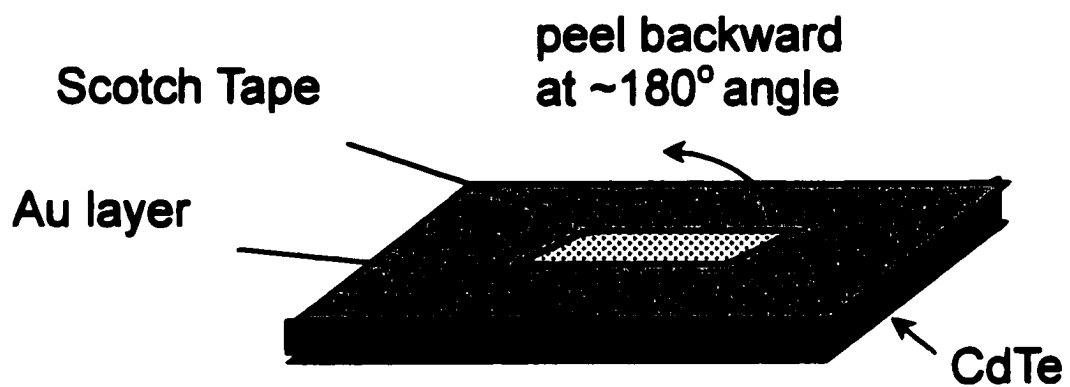
beam is finally focused on to the sample and the diffracted secondary ions are detected by a quadrupole mass spectrometer.

#### **4-11. Adhesion measurement – Tape method**

Adhesion is a fundamental parameter in surface chemistry and physics because it depends directly on interatomic and intermolecular forces. There are various ways to measure the adhesion between two similar or dissimilar materials, both qualitatively and quantitatively.<sup>[6]</sup>

The tape method is a mechanical, destructive technique to measure the adhesion of thin film on the substrate. It was first used by Strong to determine the adhesion of evaporated aluminum films on glass.<sup>[7]</sup> A pressure sensitive tape is pressed onto the film and then rapidly stripped. Three possibilities arise: a) the film is completely removed; b) the film is not at all removed; and c) the film is partly removed or removed in patches. Therefore this technique is highly qualitative. However, it has advantages of being inexpensive and quick. It can be utilized for screening cases of very poor adhesion from the ones showing appreciable adhesion.

The tape method was employed in this research to measure the adhesion of the gold films on the CdTe epilayers. It was performed following the procedure prescribed by the American Society for Testing and Materials (ASTM-B571). Fig. 4-14 illustrates the way to perform the test. Commercial



**Fig. 4-14. Illustration of the scotch tape measurement.**

**scotch tape was used instead of pressure sensitive tape (Permacel 99). It was placed over the gold surface and pressed lightly to ensure flat and even contact. The tape was then rapidly peeled backward at an approximately 180° angle, indicating a purely shear force being applied at the Au-CdTe interface.**

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1. **Light and Electron Microscopy, Slayter and Slayter, Cambridge University Press, 1992**
2. **Advanced Light Microscopy, Pluta, Elsevier, 1988**
3. **G. Binnig, C.F. Quate and Ch. Gerber, Phys. Rev. Lett. 56, 930 (1986)**
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9. **F. Fischer, M. Keller, T. Gerhard, T. Behr, T. Litz, H.J. Lugauer, M. Keim, G. Reuscher, T. Baron, A. Waag and G. Landwehr, J. Appl. Phys. 84(3), 1650 (1998)**
10. **W.J. Everson, C.K. Ard, J.L. Sepich, B.E. Dean, G.T. Neugebauer and H.F. Schaake, J. Electron. Mater. 24(5), 505 (1995)**

# CHAPTER 5

## Development of the Shadow Mask Selective Area

### Molecular Beam Epitaxy Technique

#### 5-1. Introduction

The shadow mask selective area molecular beam epitaxy was initially performed by placing the shadow mask on top of the substrate outside the MBE growth environment during the mounting of the substrate on the moly block. We call the mask fixture used to perform these growths *ex situ* mask fixture. The gradual improvement of the mesa pattern definition along with the improvement of the *ex situ* mask fixture design and the positioning of the incident flux beams enabled us to develop an understanding of the shadow mask SAE growth habits. Based on the shadow mask SAE growth experience obtained with the *ex situ* mask fixture, we designed and fabricated an *in situ* mask fixture that allows the mask to be placed and removed within the vacuum growth system.

In this chapter, I will first introduce the SAE growth of patterned CdTe epilayers using the *ex situ* mask fixture. The mesa pattern definition optimization along with the improvement of the mask mounting technique and the CdTe flux incidence will be described in sequence. The shadow mask

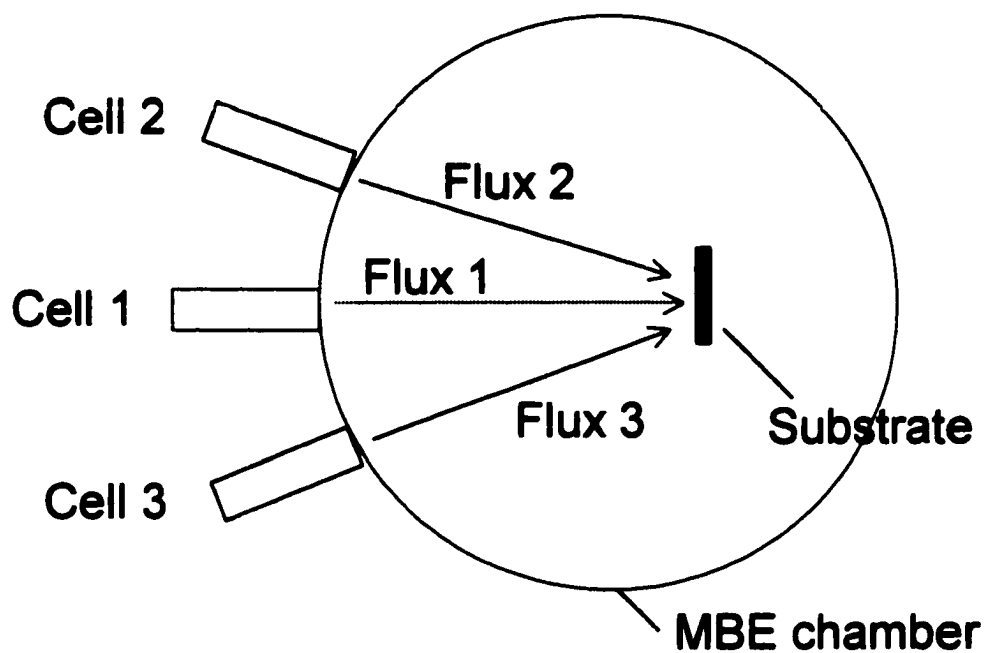
SAE growth habits related to the mask and flux geometry will be illustrated. The excellent pattern definition of CdTe square arrays obtained with near normal incidence flux and optimized mask and mask fixture design will be presented. Finally I will introduce the growth with the *in situ* mask fixture.

## **5-2. SAE growth using the *ex situ* mask fixture**

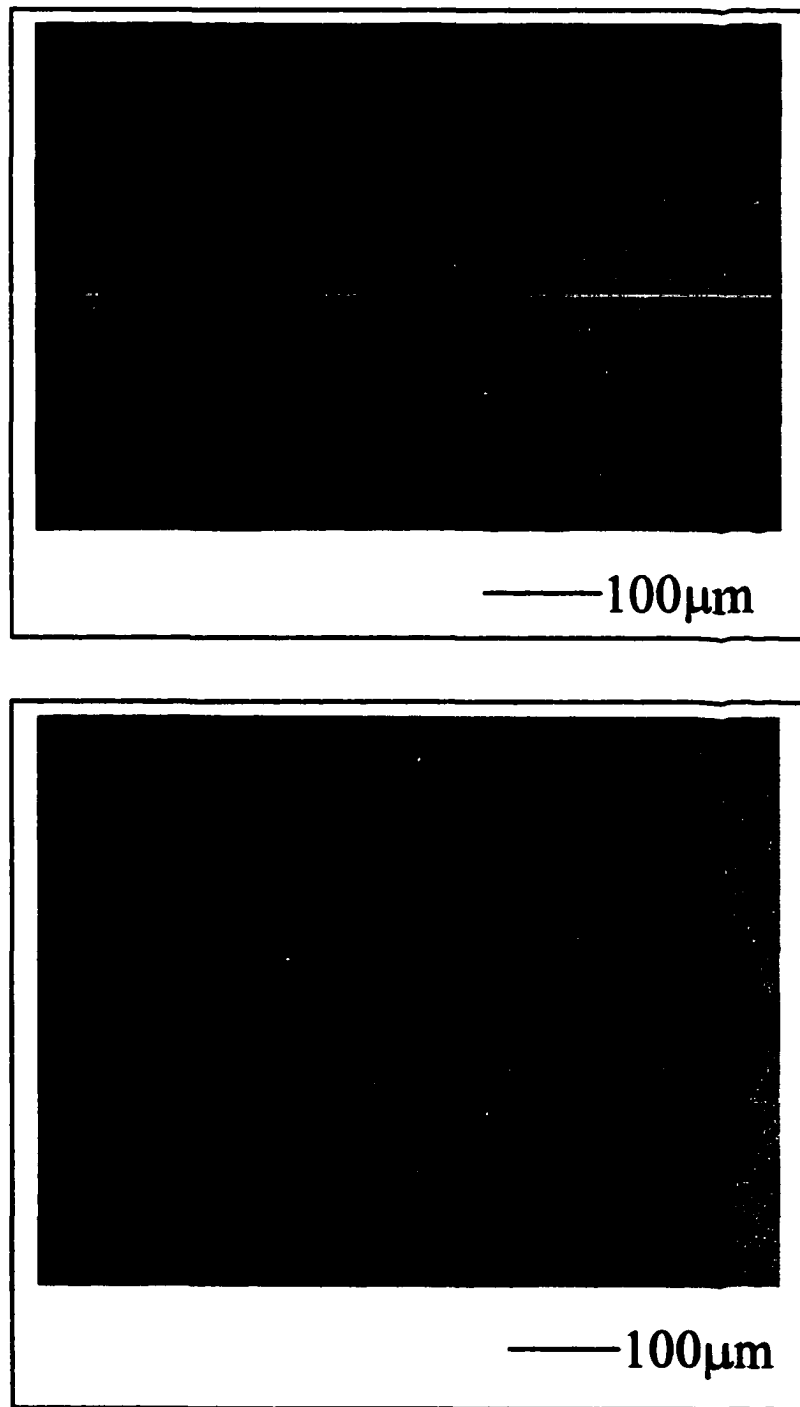
### **5-2-1. Optimization of the mesa pattern definition**

The initial CdTe shadow mask SAE growth was performed with the CdTe source cell placed in an outer port of the MBE source flange resulting in an oblique ( $\sim 10\text{-}15^\circ$ ) flux incidence (Fig. 5-1). Rotation of the sample during growth was also performed as with the flat layer growth. The shadow mask was attached to the substrates by clamps following the method described by Tsang et. al.<sup>[1]</sup> We experienced difficulties in placing the mask flat and intimate with the substrate surface. The pattern definition of the mesas obtained this way is very poor (Fig. 5-2).

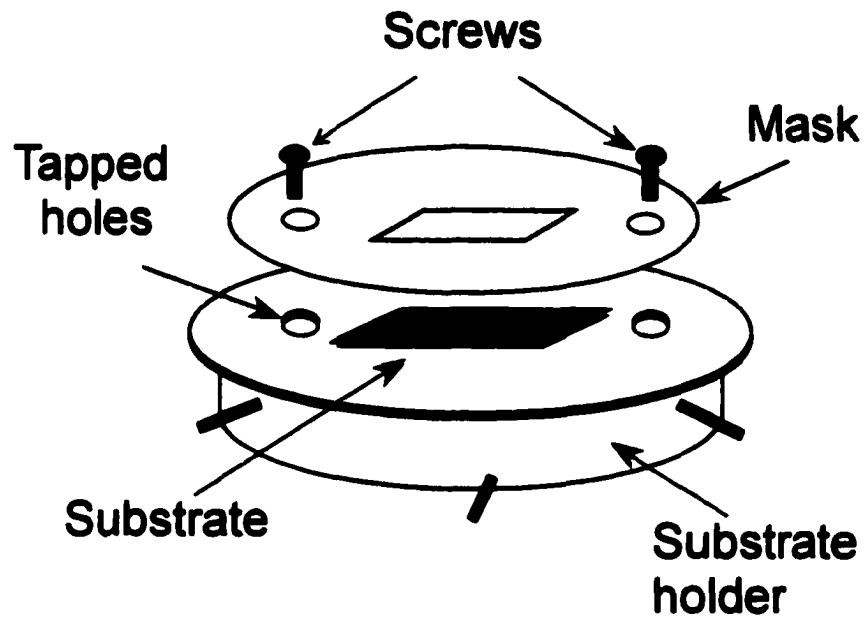
A modified mask mounting technique was employed to correct some of the problems. Two holes were drilled into both the mask and the substrate holder so that the mask could be secured onto the substrate by using screws (Fig. 5-3). With this modification we obtained samples on which there are regions with reasonably good pattern definition (Fig. 5-4a). However, there are regions with poor definition (Fig. 5-4b), which suggests that the mask was



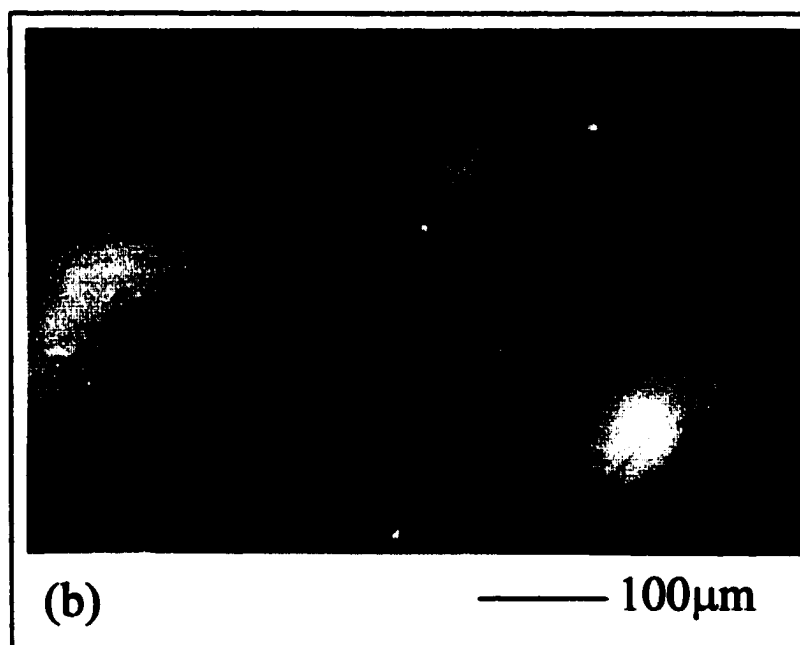
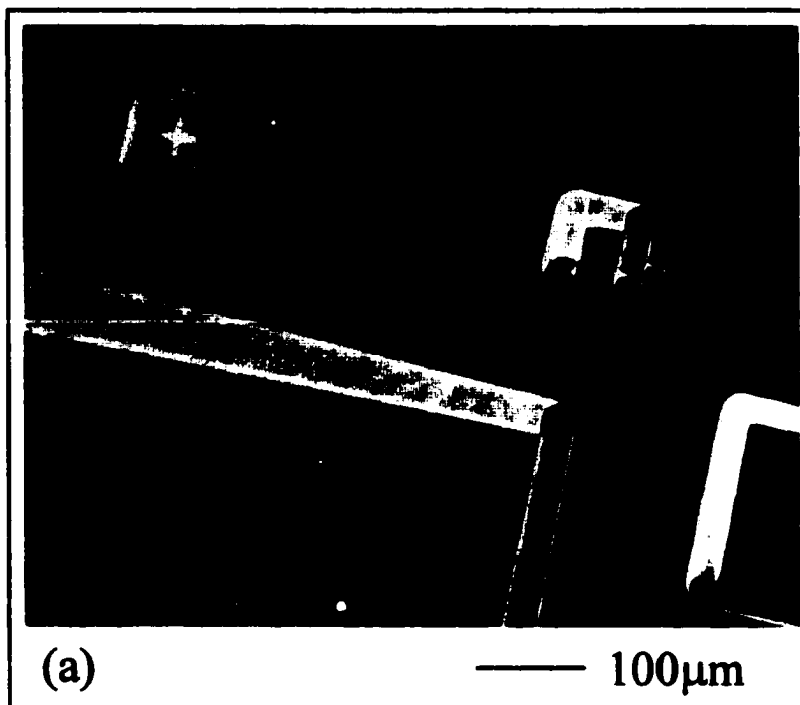
**Fig. 5-1. Schematic of the normal and oblique incident fluxes. Flux 1 emanate from cell 1 in the center port position of the MBE source flange is normal to the substrate while flux 2 and 3 from cell 2 and 3 in the off normal position in the MBE source flange are oblique fluxes.**



**Fig. 5-2. Poor pattern definition of the CdTe mesas obtained in the initial SAE growth using clamps to attach the mask to the substrate.**



**Fig. 5-3. Mask mounting using screws to attach the mask to the substrate.**

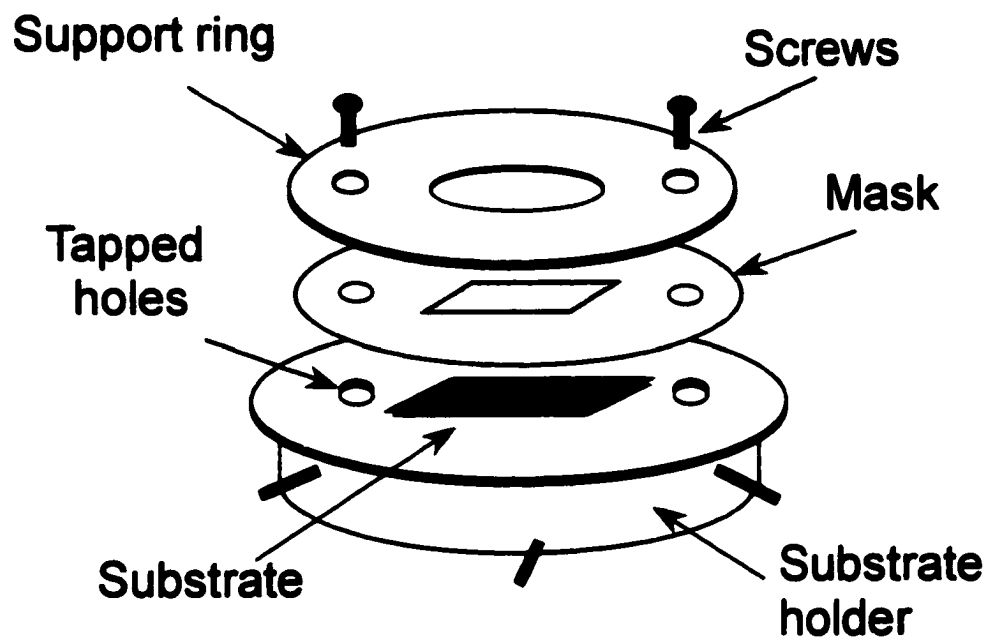


**Fig. 5-4. CdTe mesas obtained with the SAE growth using screws to attach the mask to the substrate: a) regions with reasonably good mesa pattern definition; and b) regions with poor pattern definition.**

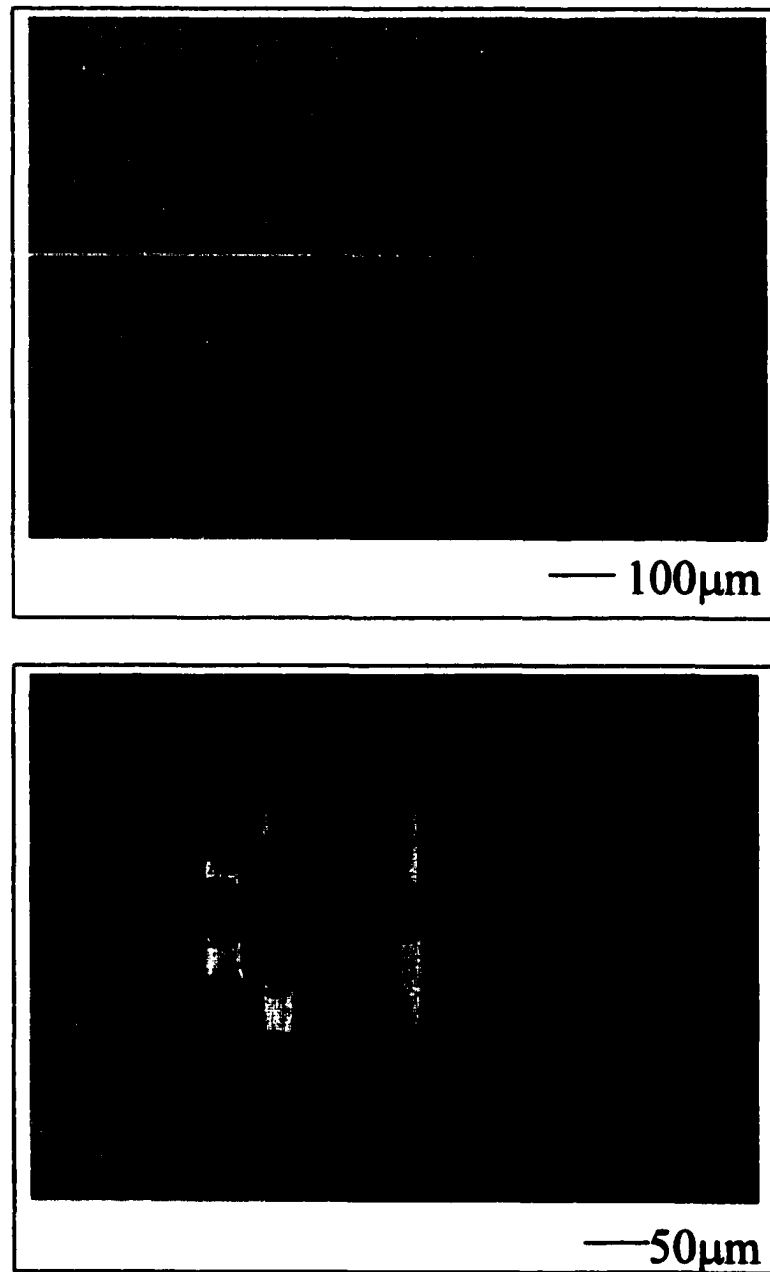
not in good contact with the substrate throughout the entire surface. In addition, we observed some permanent damage to the mask, such as bending and bowing, due to the nature of the metal mask.

Further improvement was made by using a stainless steel support ring on top of the mask to reduce the mask bending so that the mask can be in good contact with the substrate (Fig. 5-5). With this, we obtained better lateral definition and uniformity throughout the wafer (Fig. 5-6). However, the mesa edges are still somewhat broad and the surfaces of the mesas are not flat, especially for small structures ( $<100\mu\text{m}$ ). Fig. 5-7 shows a Nomarski micrograph and the corresponding profiler plot of one of the  $50\mu\text{m}$  square mesas grown this way. The dark region in the center of the mesa seen in the optical micrograph suggests that the mesa top is not flat. This is confirmed by the profiler plot, which also indicates that the average mesa height is only  $\sim 0.5\mu\text{m}$ , while  $\sim 1.0\mu\text{m}$  thickness is observed in the larger mesas.

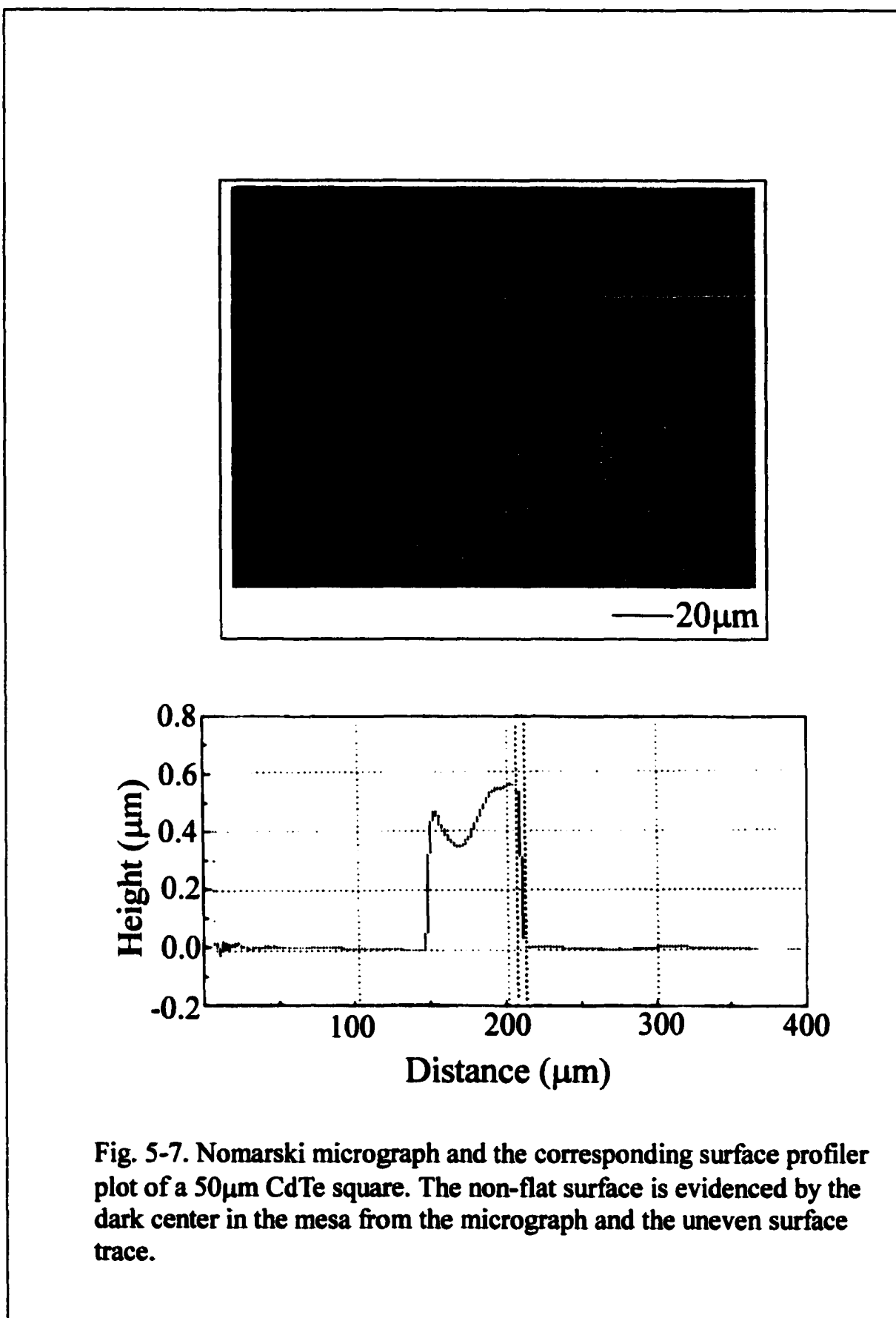
To investigate the reasons for this, a sample was grown without substrate rotation to compare the pattern definition. Very good results were obtained as shown in Fig. 5-8. The mesa surfaces are flat and the edges are sharp ( $\sim 6\text{-}8\mu\text{m}$ ). However, the small size structures are incomplete and the edges of some structures are missing. We concluded that this behavior was

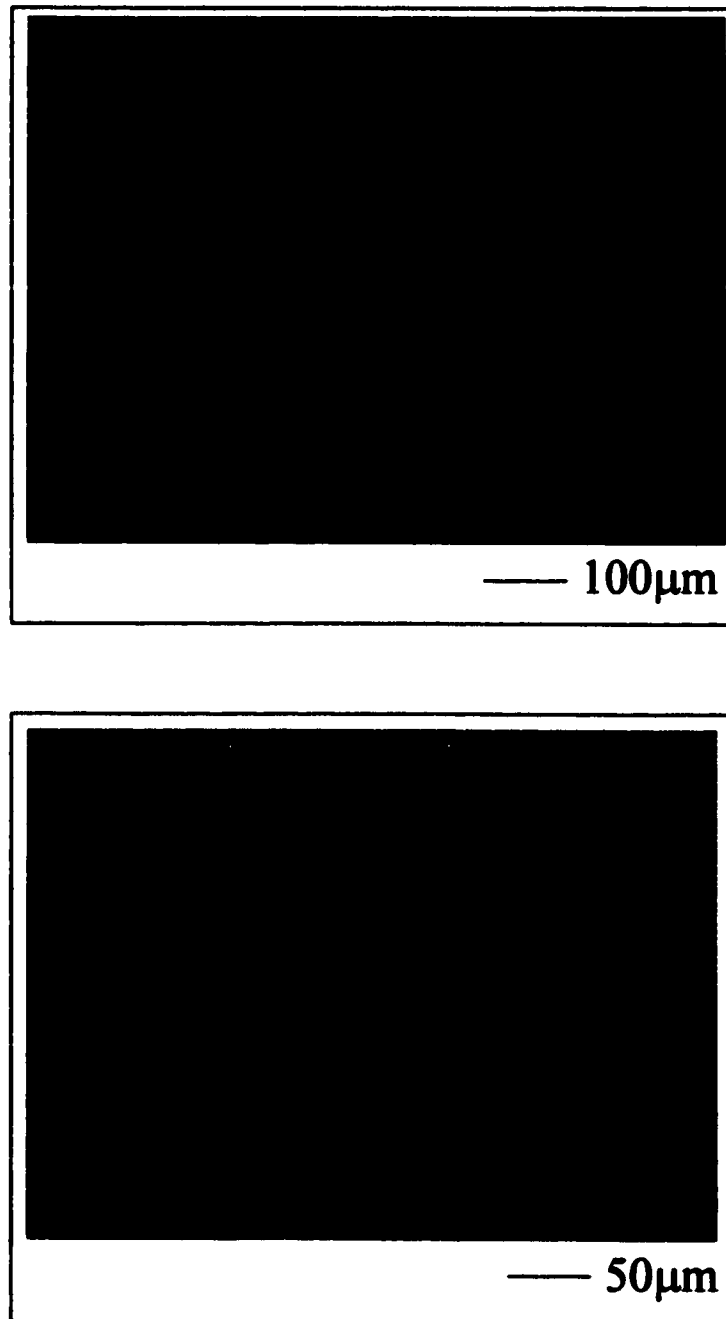


**Fig. 5-5. Improvement of the mask mounting using an additional support ring on top of the mask to ensure flat and intimate contact between the mask and the substrate.**



**Fig. 5-6. Nomarski micrographs of the CdTe mesas exhibiting good pattern definition and uniformity.**





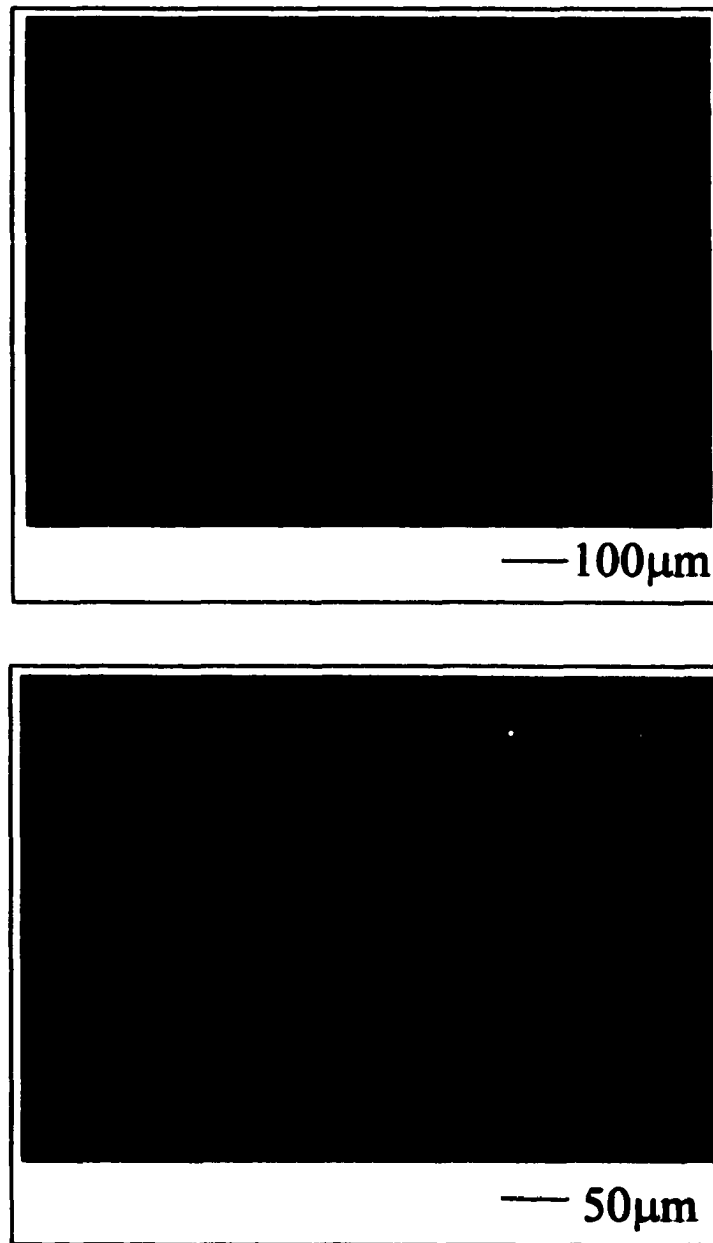
**Fig. 5-8. Nomarski micrographs of the CdTe mesas grown without substrate rotation. Some of the mesa shapes are incomplete.**

caused by the thickness of the mask ( $150\mu\text{m}$ ) which blocks the oblique CdTe incident flux.

When the CdTe cell was moved to a central position in the MBE source flange, ensuring a more normal incidence of the CdTe flux, greatly improved pattern definition was obtained. Fig. 5-9 shows the Nomarski micrographs in two areas of the wafer grown with this geometry without sample rotation and Fig. 5-10 shows the corresponding surface profiler plots. Very abrupt side walls of the mesas are evident both from the optical micrographs and from the surface profiles. The surfaces of the mesas are flat and the mesa height are  $\sim 1.2\mu\text{m}$ . Good uniformity across the wafer surface was obtained when the metal mask was placed flat relative to the substrate surface. The use of the sample rotation under similar growth conditions also results in good mesa pattern with slightly broader side walls. This suggests that some growth under the mask is occurring due to the presence of a finite separation between the substrate and the mask and to the slightly off-normal position of the CdTe source, even in the central cell port.

#### *5-2-2. Pattern definition vs. mask and flux geometry*

Table 5-1 summarizes the growth results obtained with the various growth conditions described in the previous paragraphs. As indicated, the



**Fig. 5-9. Nomarski micrographs of the CdTe mesas with excellent pattern definition.**

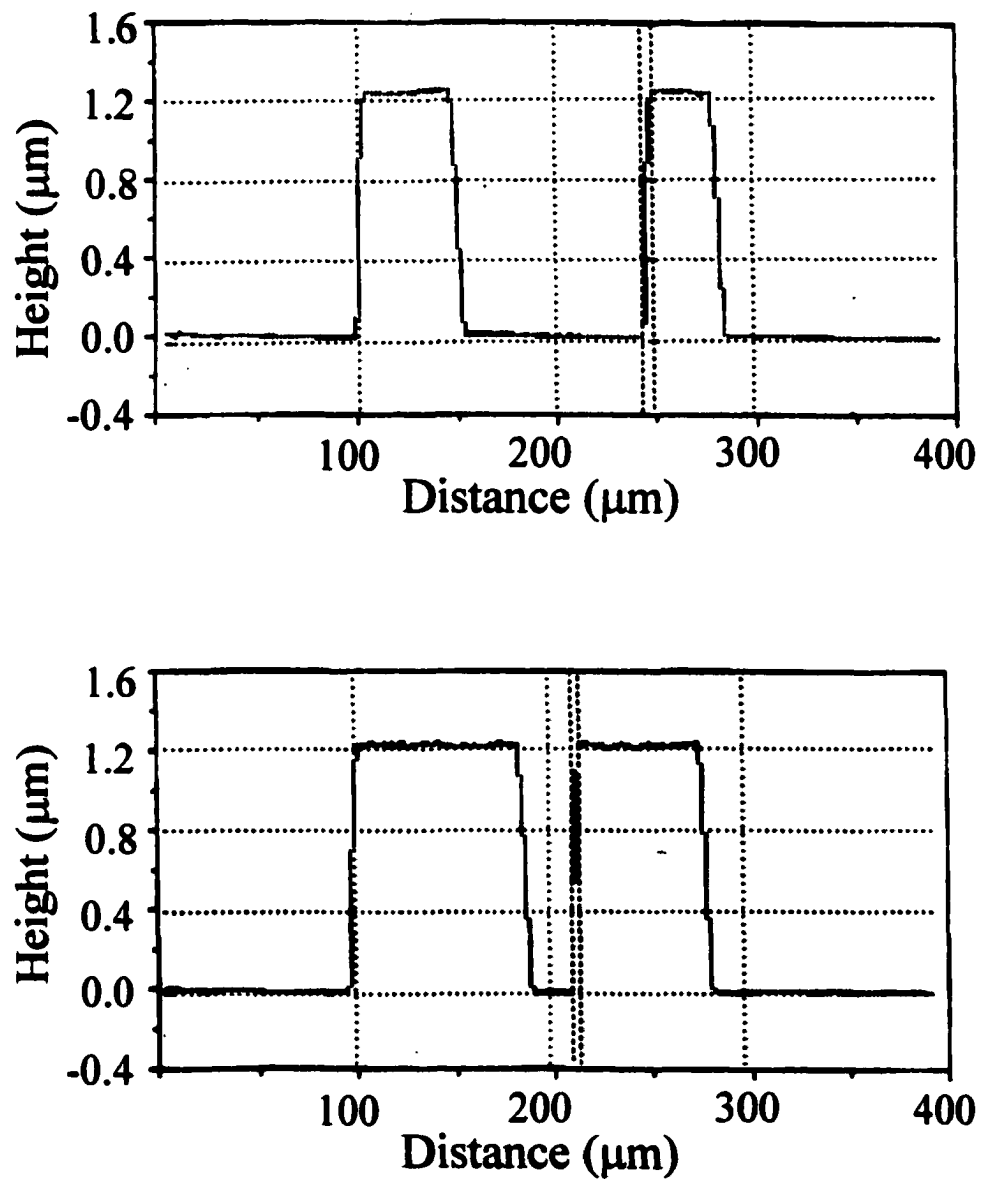


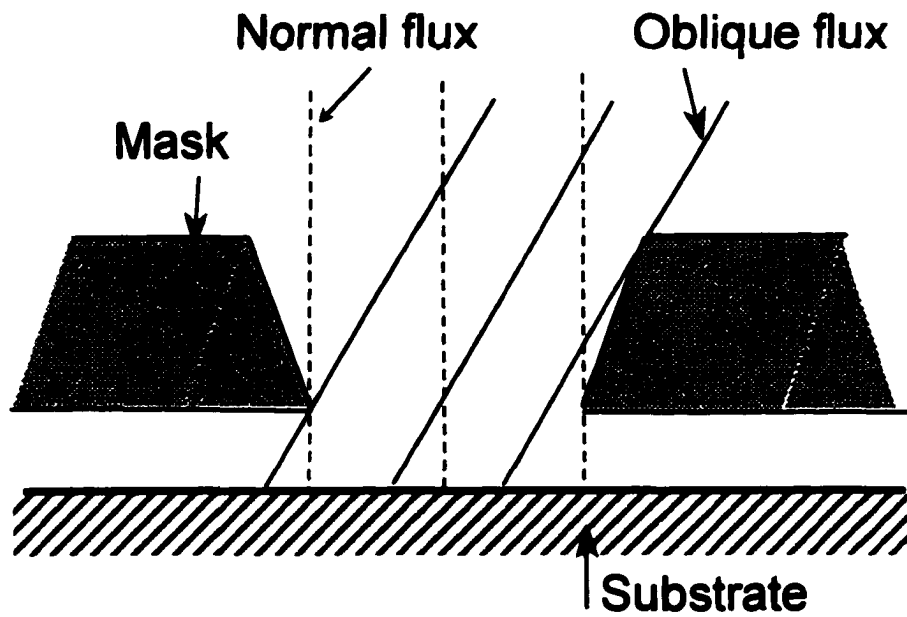
Fig. 5-10. Surface profiler plots of the CdTe mesas shown in Fig. 5-9.

<b>CdTe Cell position</b>	<b>Sample rotation</b>	<b>Fixture</b>	<b>Pattern definition</b>
Oblique	Yes	Clamps	Very poor
Oblique	Yes	Screws	Poor
Oblique	Yes	Screws + Support ring	Broad edge + non-flat surface
Oblique	No	Screws + Support ring	Incomplete feature
Near normal	No	Screws + Support ring	Excellent
Near normal	Yes	Screws + Support ring	Excellent (slightly broader edge)

**Table 5-1. Summary of the growth results obtained with the various growth conditions. The best results were obtained with normal incident flux and use of screws and support ring to attach the mask to the substrate.**

growths with near normal incident CdTe flux and *ex situ* mask fixture employing screws and support ring give the best results.

Based on the above growth results, we developed an understanding of the shadow mask SAE growth habits. When the CdTe source was in an outer port of the MBE source flange, severe mask shadowing effect resulted. Fig. 5-11 illustrates this mask shadowing effect. In spite of the tapered side wall of the window openings, the thickness of the mask produces significant shadowing when the incident flux is oblique. This limits the overall height and the shape of the small mesas. The shadowing effect was made very clear by the observation that the growth without rotation resulted in distorted mesa shapes. The effect of sample rotation during growth was to make the mesas more uniform, but the net mesa height was reduced and the mesa tops were not flat. There is also growth under the mask due to the separation between the mask and the substrate. It causes the broadening of the mesa edges. Ideally, a normal incidence flux is required to eliminate these effects as also illustrated in Fig. 5-11. This is evidenced by the fact that significant improvements in the mesa pattern definition were observed when the CdTe cell was moved to a more normal incident position. However, in practice, it is not possible that all the fluxes be normal incidence. The presence of a tilt of the incident flux will still cause certain broadening of the mesa edges with the



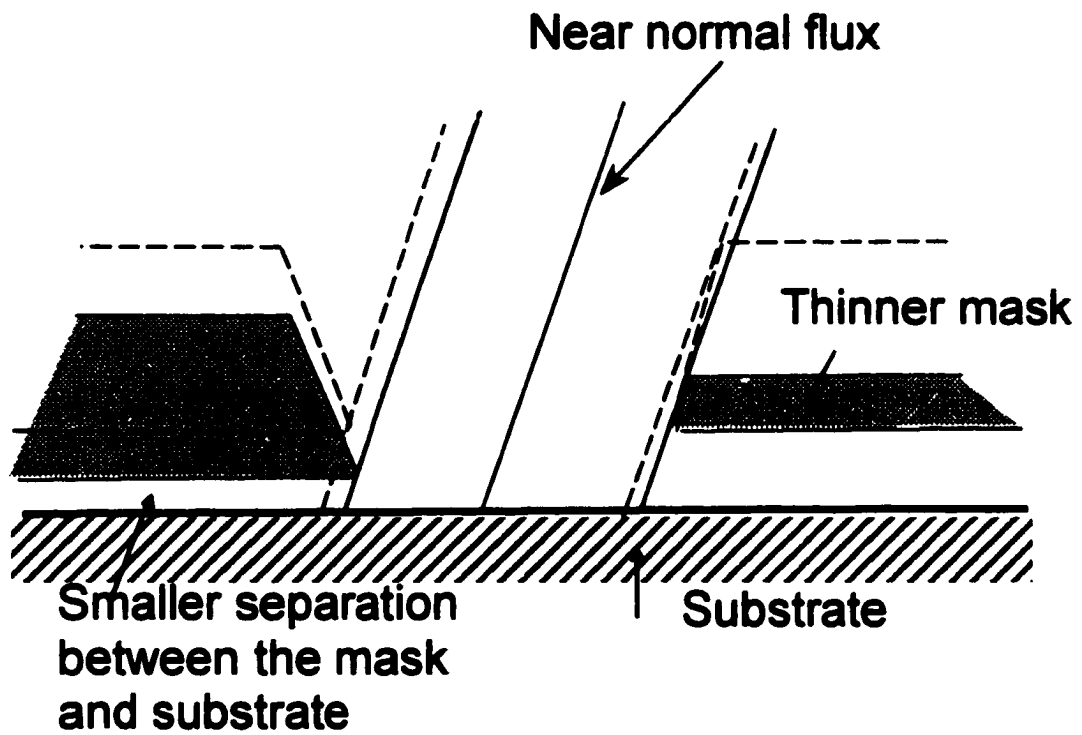
**Fig. 5-11. Illustration of the mask shadowing effect. The oblique incident flux can be blocked by the mask with finite thickness and growth under the mask occurs with the existence of the separation between the mask and substrate.**

separation between the mask and substrate, and the blocking of the incident flux still exist with the finite thickness of the mask. Therefore other ways to minimize these effects are needed. As Fig. 5-12 suggests, the use of a thinner mask will minimize the mask shadowing effect. Besides that, an intimate contact between the mask and the substrate will also compensate for the tilt of the beam flux and reduce the growth under the mask. Fig. 5-13 illustrates the optimum conditions for the shadow mask SAE growth in order to obtain excellent pattern definition.

It is worth mentioning that the tapering of the mesa edge might be beneficial in some device applications. For example, it can be used in taper coupled lasers and some light emitting devices.<sup>[2,3]</sup>

### *5-2-3. Growth with optimum mask and flux geometry*

We have so far optimized the shadow mask SAE growth by using near normal incident CdTe flux and using screws and a support ring to fix the mask on the substrate. To make the shadow mask SAE technique more applicable for detector array fabrication, a new mask consisting of square window arrays was designed and implemented in the growth. As described in chapter 3, the new mask is only 50 $\mu\text{m}$  thick. The thickness in the mask patterned region is much thinner, only 3-4 $\mu\text{m}$ . The use of a thin mask is expected to further reduce the mask shadowing effect.



**Fig. 5-12. Illustration of two ways to improve the mesa pattern definition with near normal incident flux: 1) use of thinner mask and 2) closer contact between the mask and substrate.**

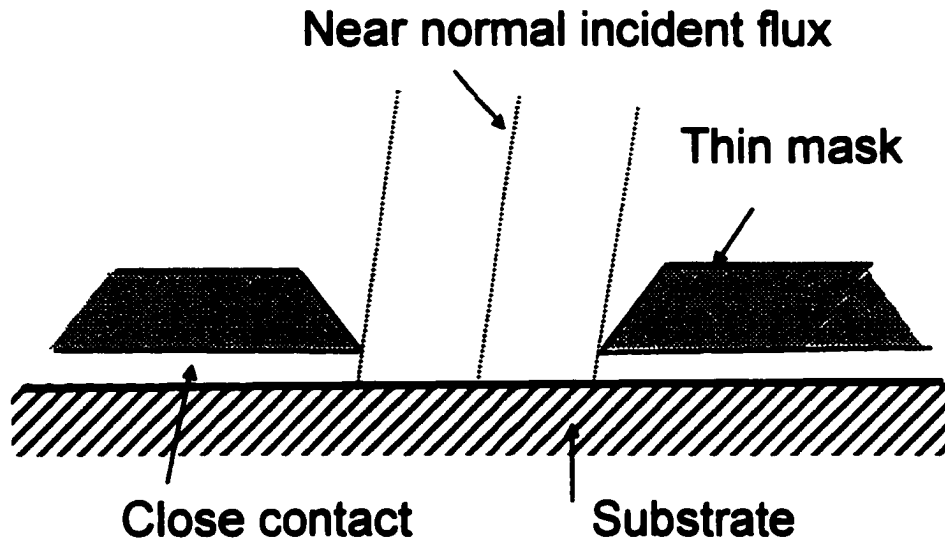


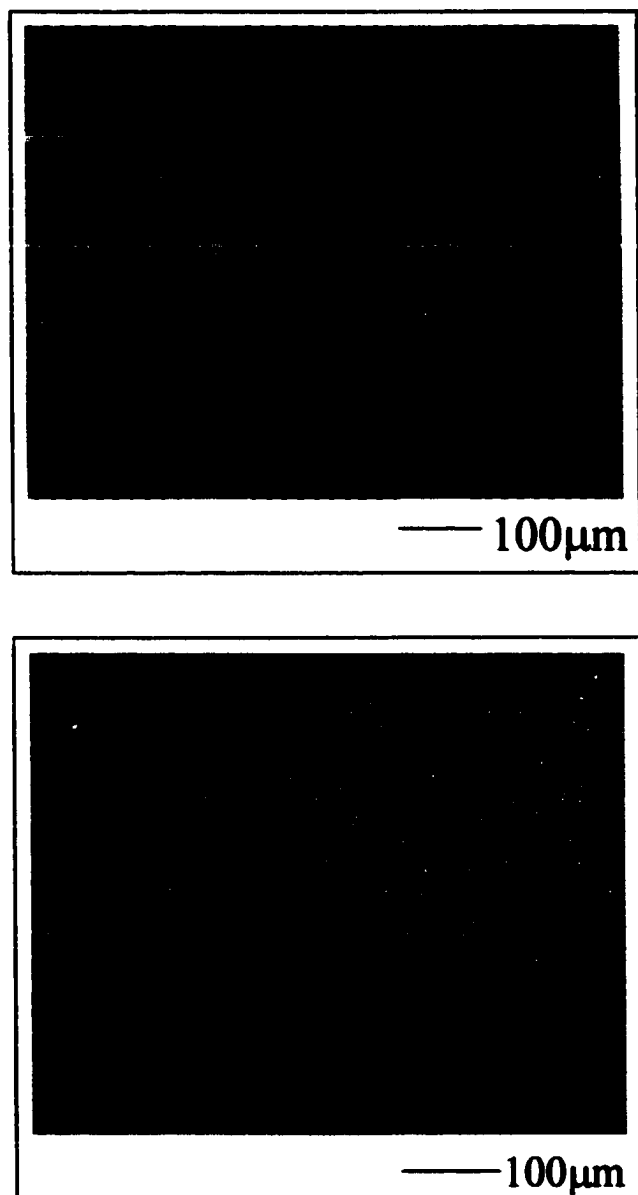
Fig. 5-13. Optimum conditions for shadow mask SAE growth:

- 1) use of near normal incident flux;
- 2) thin mask;
- 3) close contact between the mask and substrate.

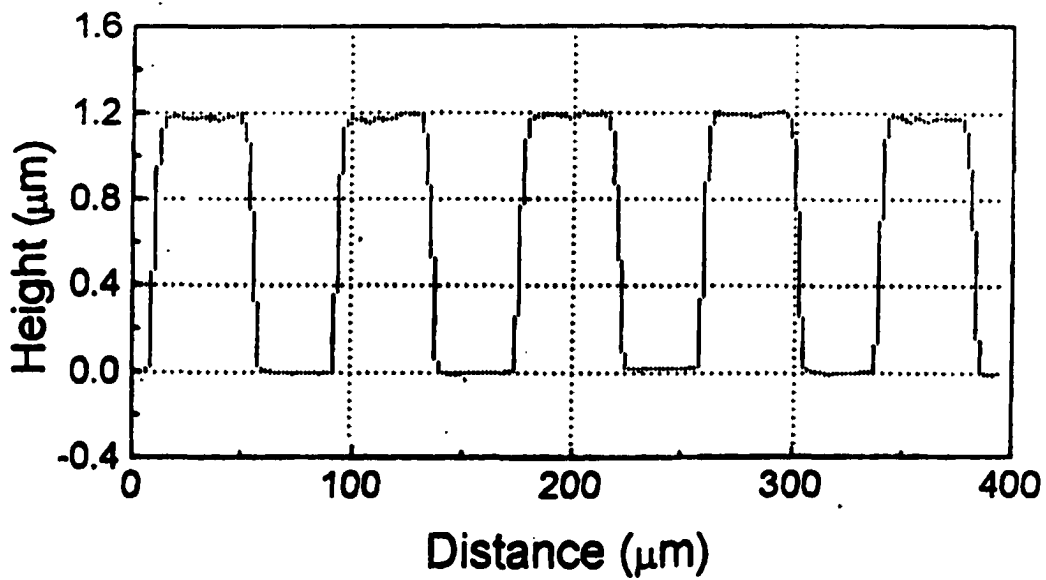
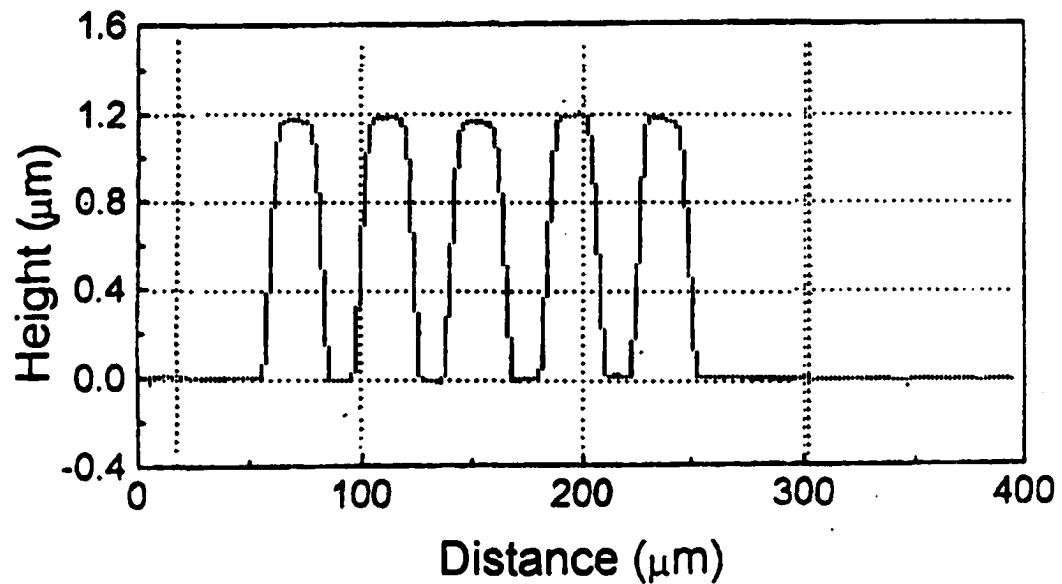
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We obtained excellent pattern definition of the CdTe square arrays grown with the new mask. The Nomarski micrographs and profiler plots of the representative CdTe square arrays are shown in Fig. 5-14 and Fig. 5-15. The mesas have abrupt side walls, flat and smooth surfaces, and well defined separations. No growth was observed between the CdTe mesas. This is so even for the smallest  $20\mu\text{m}$  squares with  $20\mu\text{m}$  separation. Fig. 5-16 shows a high magnification micrograph of the  $40\mu\text{m}$  square arrays and the corresponding surface profile in a more sensitive scale. The mesa edges taper over  $\sim 5\text{-}7\ \mu\text{m}$  when grown without sample rotation. The side walls of the CdTe mesas grown with sample rotation are somewhat broader than those grown without sample rotation. They taper over  $\sim 7\text{-}9\ \mu\text{m}$ . This is consistent with our earlier observations and it is due to the presence of a slight tilt of the CdTe incident flux and a finite separation between the mask and the substrate.

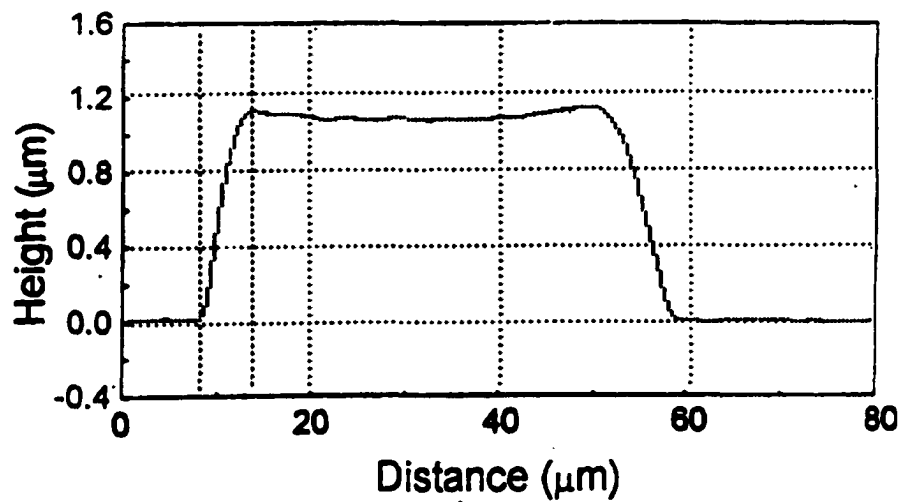
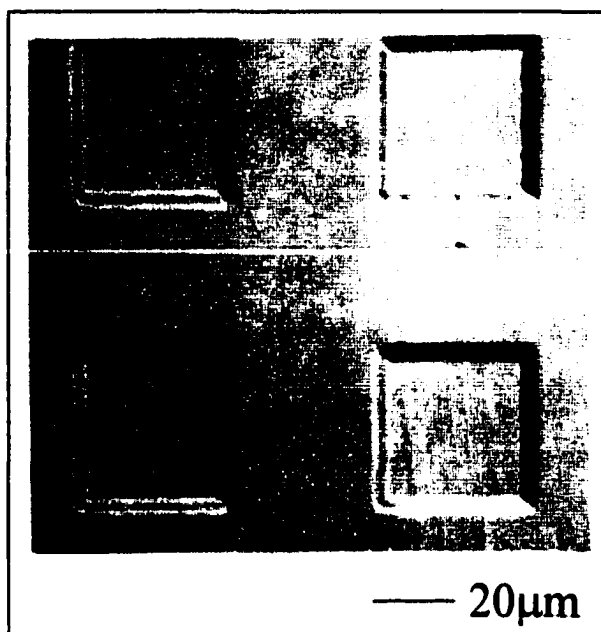
The shadow mask SAE growth of CdTe was also performed at  $190^\circ\text{C}$  which is the typical MBE growth temperature for HgCdTe. Similar excellent pattern definition was observed. Fig. 5-17 and 5-18 show their optical micrographs and corresponding surface profiles. Growth at lower temperature was expected to reduce the diffusion of the atoms under the mask and



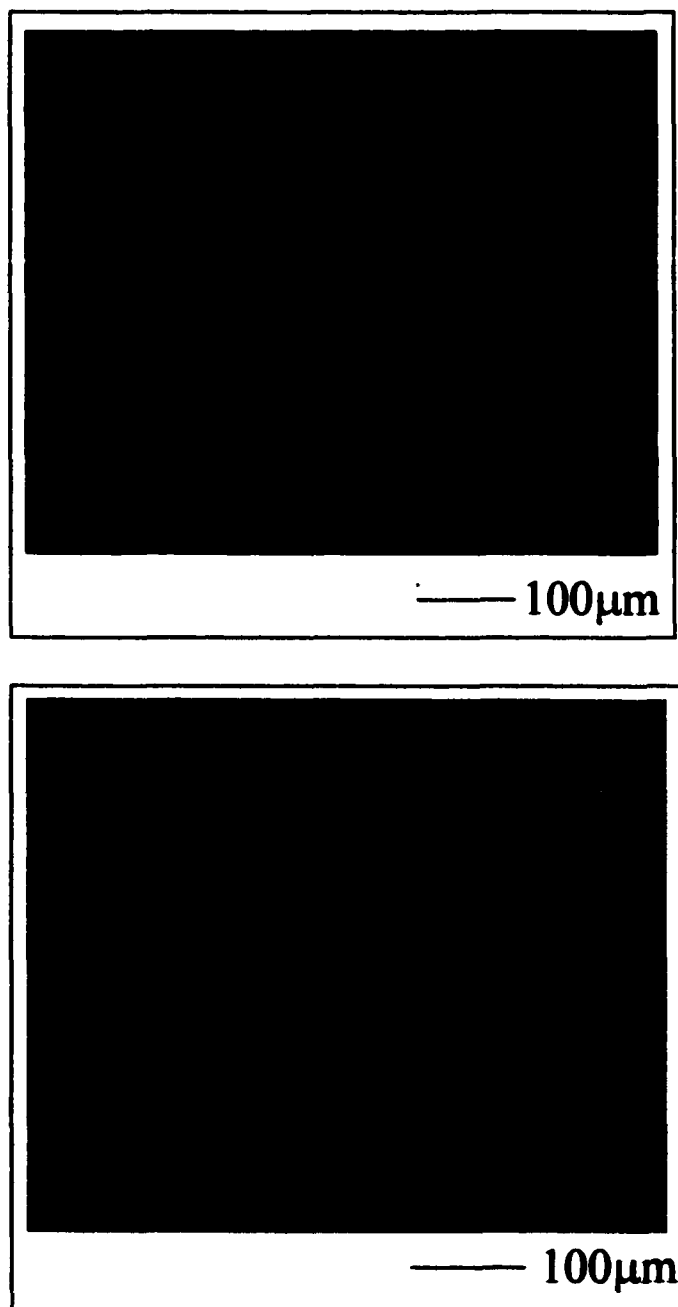
**Fig. 5-14. Nomarski micrographs of the 20 $\mu$ m and 40 $\mu$ m CdTe square arrays grown at 285 $^{\circ}$ C.**



**Fig. 5-15. Surface profiles of the 20μm and 40μm CdTe square arrays shown in Fig. 5-14.**



**Fig. 5-16. High magnification Nomarski micrograph of the 40 μm CdTe square arrays and the corresponding surface profiler plot in a more sensitive scale.**



**Fig. 5-17. Nomarski micrographs of the 20μm and 40μm CdTe square arrays grown at 190°C.**

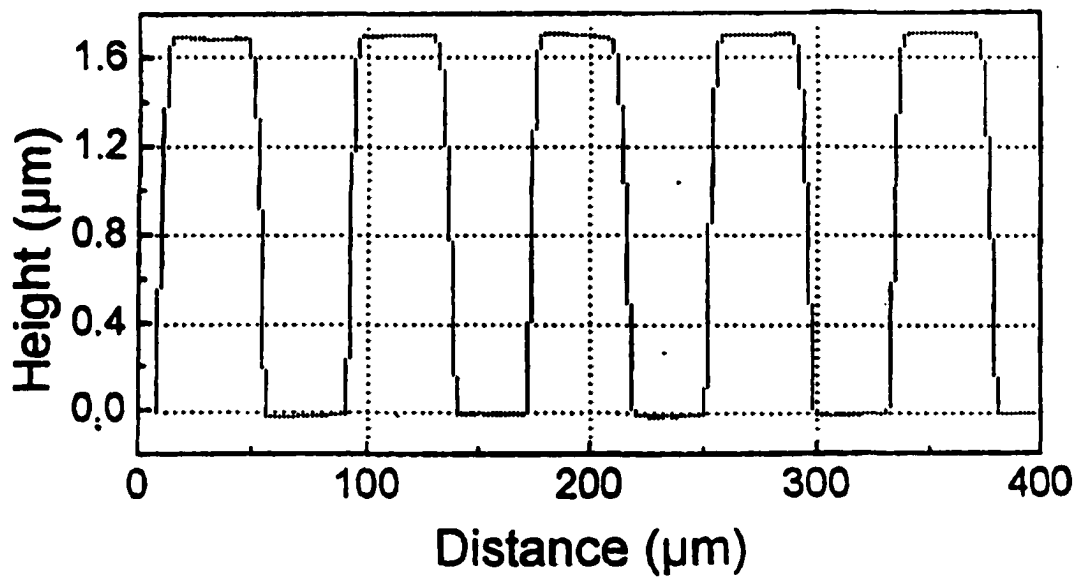
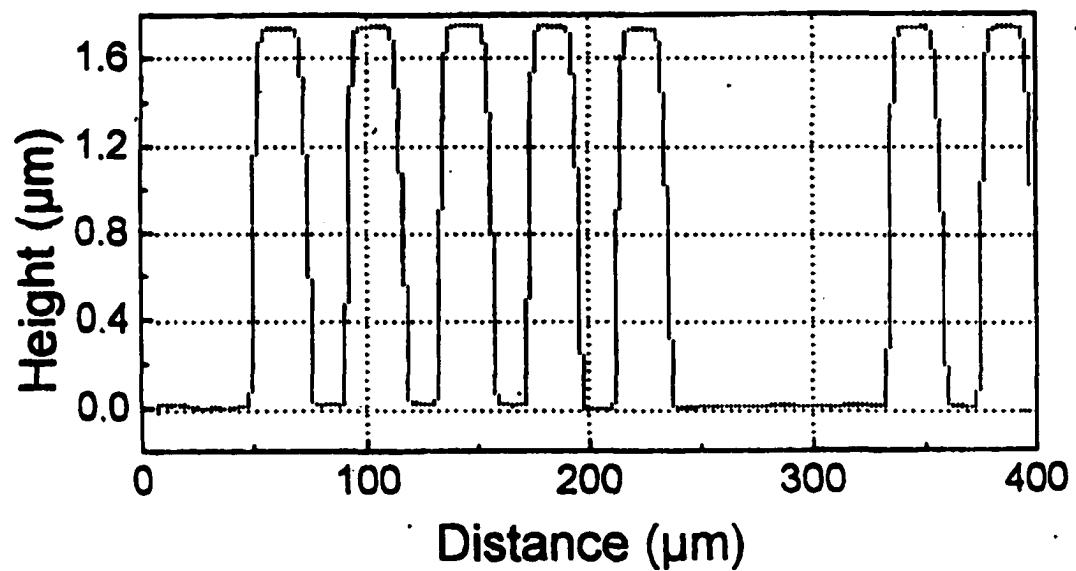
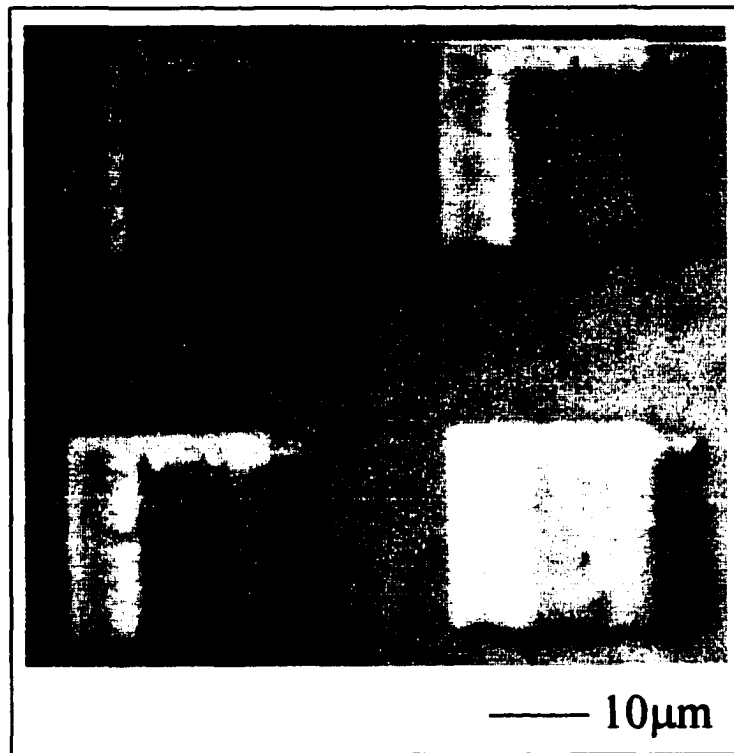


Fig. 5-18. Surface profiles of the 20µm and 40µm CdTe square arrays shown in Fig. 5-17.

therefore it might reduce the edge width of the mesas. However, we did not observe any obvious reduction in the mesa edge width. It appears that the pattern definition mostly depends on the placement of the mask to the substrate: the closer, the better. The growth rate at 190°C is approximately 1.7  $\mu\text{m/hr}$ , consistent with the larger sticking coefficient of Cd at the lower growth temperature. The difference of the atom migration between 270°C and 190°C is not sufficient to change the properties of the mesa patterns observed.

In one of the early samples grown with the new mask design, we observed an anisotropic growth of CdTe on the CdTe (211)B substrate. The edges of the mesas are broader in one direction than that in the other. It is particularly obvious in the 20 $\mu\text{m}$  squares (Fig. 5-19) since the breadth of the edges is significant compared to the small square size. This asymmetry was finally traced to the uneven placement of the mask.

Table 5-2 is the summary of our growth runs with the array like mask design. The numbers quoted are based on the average of 8-15 measurements. The slight concave shape of two of the samples' mesa tops (A541 and A564) which is similar as the one shown in Fig. 5-16 is believed to be related to the use of the new metal masks. They may have different emissivities from the substrate and this would result in the slight thickness variation of the grown



**Fig. 5-19. Nomarski micrograph of the 20µm CdTe squares exhibiting asymmetric side walls.**

<b>Sample No.</b>	<b>A541</b>	<b>A555</b>	<b>A564</b>	<b>A581</b>
<b>Mask</b>	<b>New</b>	<b>Used</b>	<b>New</b>	<b>Used</b>
<b>Rotation</b>	<b>No</b>	<b>Yes</b>	<b>No</b>	<b>No</b>
<b>Edge Width</b>	<b>5-6<math>\mu</math>m, 6-9<math>\mu</math>m</b>	<b>8-10<math>\mu</math>m</b>	<b>6-8<math>\mu</math>m</b>	<b>6-8<math>\mu</math>m</b>
<b>Mesa(20<math>\mu</math>m)Height</b>	<b>1.15<math>\mu</math>m</b>	<b>1.15<math>\mu</math>m</b>	<b>1.2<math>\mu</math>m</b>	<b>1.2<math>\mu</math>m</b>
<b>Mesa Top</b>	<b>Slightly concave <math>\pm 0.02\mu</math>m</b>	<b>Very flat</b>	<b>Slightly concave <math>\pm 0.02\mu</math>m</b>	<b>Very flat</b>
<b>Side wall symmetry</b>	<b>Asymmetric</b>	<b>Symmetric</b>	<b>Symmetric</b>	<b>Symmetric</b>
<b>Uniformity within an array</b>	<b>Good</b>	<b>Good</b>	<b>Good</b>	<b>Good</b>

Table 5-2. Summary of the growth runs with the array like mask.

mesas. However, this concave shape is nearly flat and it can be neglected. The sample grown with rotation has edges somewhat broader than the others grown without rotation. This is consistent with our earlier observations.

#### *5-2-4. Optical properties of the CdTe mesas*

Optical characterization of the CdTe mesas was performed by photoluminescence (PL). The PL measurements were done using a triple-grating micro-Raman/PL spectrometer (JY-Model T64000). The laser excitation used a focused CW argon ion (514.5nm) laser with a diameter of  $\sim 2 \mu\text{m}$  so that the excitation was focused into a single CdTe mesa. The laser intensity was  $\sim 3 \times 10^4 \text{ W/cm}^2$ . The excitation position, spot size and sample surface morphology were monitored by a video camera monitor. The signal from the single CdTe mesa was detected by a photomultiplier tube (PMT). A typical PL spectrum for a CdTe mesa grown at  $285^\circ\text{C}$  is shown in Fig. 5-20a. It was measured at room temperature with a backscattering geometry. The resolution is about  $8 \text{ cm}^{-1}$ . The PMT detector cut off is at 860nm. The PL spectrum shows a peak value of 1.506 eV and a full width at half maximum (FWHM) of 55 meV, which is comparable to the data reported in the literature for flat CdTe layers obtained by other research groups (Fig. 5-20b).<sup>[2]</sup> This suggests that no deleterious effects are introduced by the use of the metal mask.

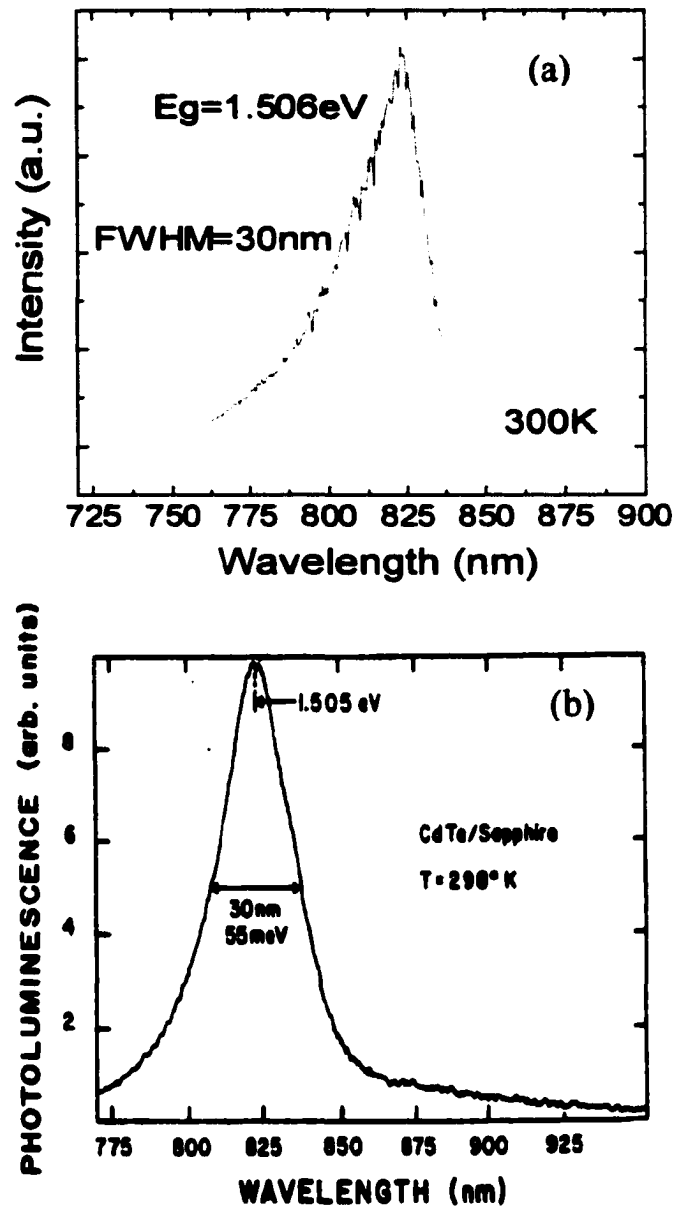


Fig. 5-20. Room temperature PL spectrum obtained from a CdTe mesa grown by SAE (a) and from flat CdTe obtained by other group (b, from N. C. Giles-Taylor, R.N. Bicknell, D.K. Blanks, T.H. Myer and J.F. Schetzina, *J. Vac. Sci. Technol. A.* 3, 76 1985)

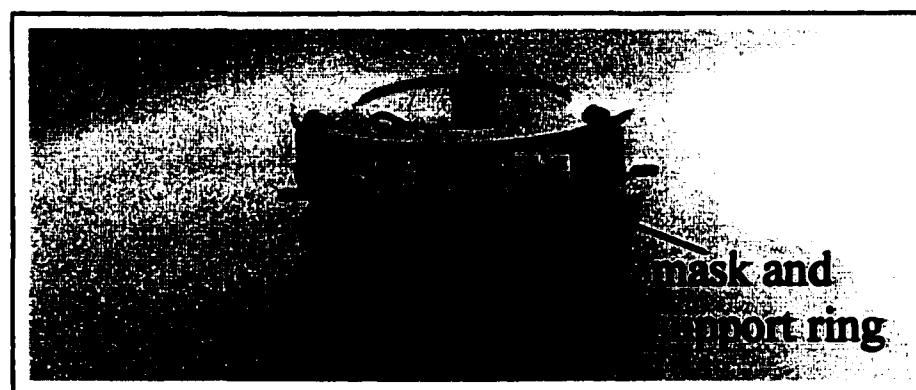
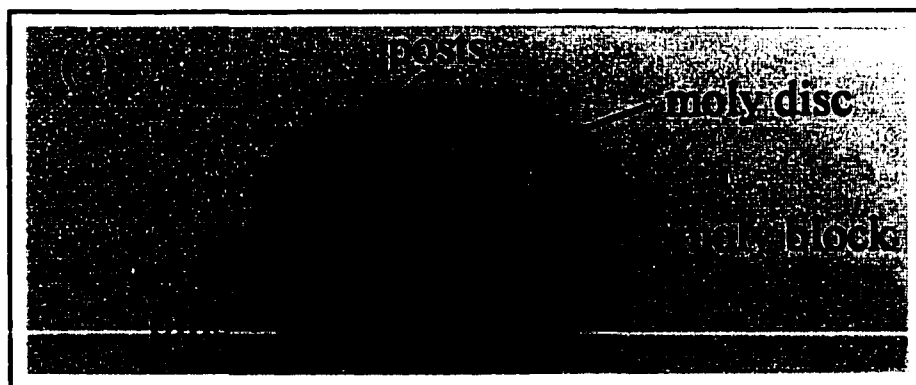
### **5-3. SAE growth using the *in situ* mask fixture**

Although excellent mesa pattern definition has been obtained with shadow mask SAE, there are some limitations with the *ex situ* mask fixture, such as: 1) the substrates are deoxidized while being covered with the mask on the top, so that the oxide desorption process can not be monitored and thus may not be complete, which may affect the quality of the epilayer; 2) different patterned structures at different stages of growth within the same sample (needed for complex device structures) can not be attained.

To overcome the aforementioned shortcomings of the *ex situ* mask fixture, we designed and fabricated an *in situ* mask fixture that allows the mask to be placed and removed within the vacuum system. With this, the oxide desorption can be performed without the presence of the mask. Patterned growth can be performed within the sample structure wherever desired and multiple step SAE can be carried out to achieve different patterned structures for more complex device fabrications.

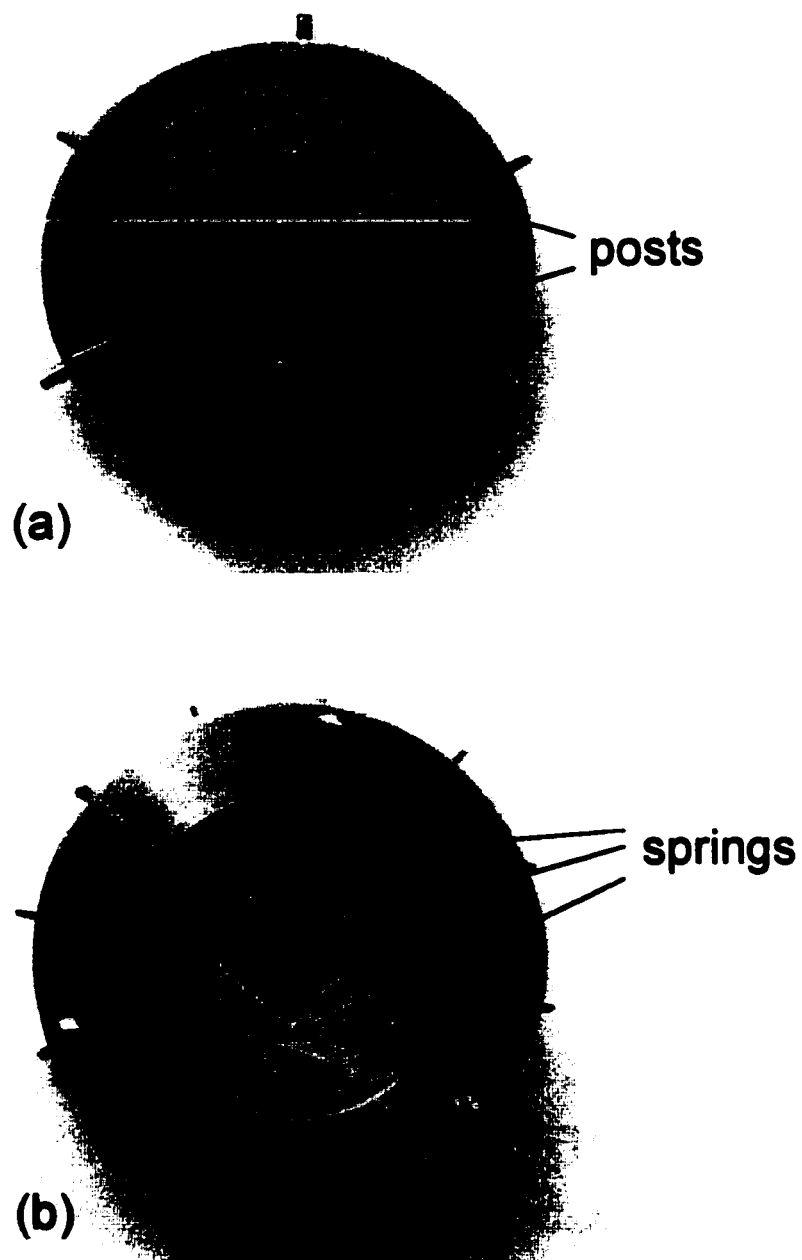
#### ***5-3-1. Description of the in situ mask fixture***

The *in situ* mask fixture consists of two parts. One is a modified substrate holder which has a smaller diameter disc attached to the surface of the regular Riber moly block (Fig. 5-21a). This disc has two posts on the top and three pins on the side. It is made out of molybdenum. The other part is a



**Fig. 5-21: Schematic of the *in situ* mask fixture:**  
 (a) substrate holder;  
 (b) mask holder;  
 (c) *in situ* fixture assembly ready for deposition.

mask holder (Fig. 5-21b). The mask is covered by the support ring and the two are held against the inner rim of the mask holder by three springs. There are two holes in both the mask and support ring, corresponding to the two posts in the substrate holder. The mask holder has three slots on the side. Like the moly block, the mask holder has six pins with which it can be placed in the cart or be transferred by the transfer rod inside the growth system. When we place the mask holder over the substrate holder, the posts fit into the holes of the mask and support ring. This avoids the relative movement between the mask and substrate so as to minimize the potential damage of scratching the substrate by the mask. These two posts also assist in placing the mask reproducibly on the substrate. After that, we can rotate the mask holder with the mask fixed in place by the posts to let the three pins in the disc of the substrate holder fit into the three slots in the mask holder. By pushing and rotating, the mask holder can be securely locked with the substrate holder (Fig. 5-21c). All these steps are carried out with the help of the three springs that keep the mask firmly pressed onto the substrate surface. The mask holder and support ring are made out of stainless steel and the springs are made out of tungsten. The top view of the substrate holder and the entire fixture are shown in Fig. 5-22a and 5-22b, respectively. The springs are clearly seen in Fig. 5-22b. With this *in situ* mask fixture, we can implement



**Fig. 5-22. Top view of the substrate holder (a) and the fixture assembly (b).**

the *in situ* device structure processing and integration using the shadow mask SAE technique.

### ***5-3-2. Growth using the in situ mask fixture***

To perform the growth, we first transfer the substrate with the substrate holder into the growth chamber and perform the oxide desorption. Unlike the situation with the *ex situ* mask holder, we can use RHEED to monitor the oxide desorption. This is one of the advantages of the *in situ* mask fixture. After the oxide desorption, we lower the substrate temperature and transfer the mask holder into the growth chamber. The mask is placed on top of the substrate and the mask holder is securely locked with the substrate holder. It takes some practice to place the mask holder over the substrate holder inside the growth chamber. One thing to watch is that the posts and the holes should be reasonably well aligned before transfer. Otherwise, the posts may not fit into the holes and will push out the mask and support ring instead. After growth, the mask holder is removed and then the substrate holder is also removed. When we place and remove the mask holder, care must be taken to make sure that the substrate holder remains on the manipulator and does not fall off.

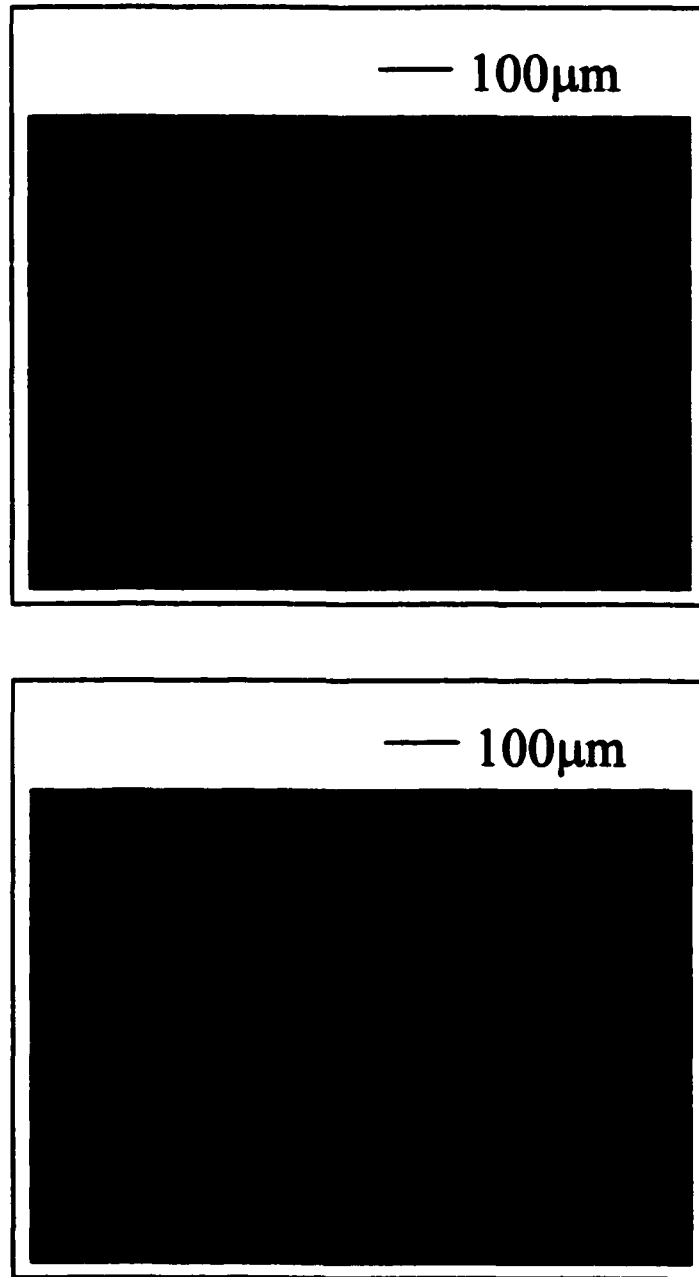
### ***5-3-3. Pattern definition obtained with the in situ mask fixture***

The Nomarski micrographs and alpha-step 200 surface profiler plots indicate that the epitaxial layers grown with the *in situ* mask fixture have good pattern definition (Fig. 5-23 and 5-24). The edges of the squares are sharp, the surfaces are flat and the separations between the squares are well defined. All the mesas in the patterned region are uniform. They are comparable to those obtained with the *ex situ* mask fixture.

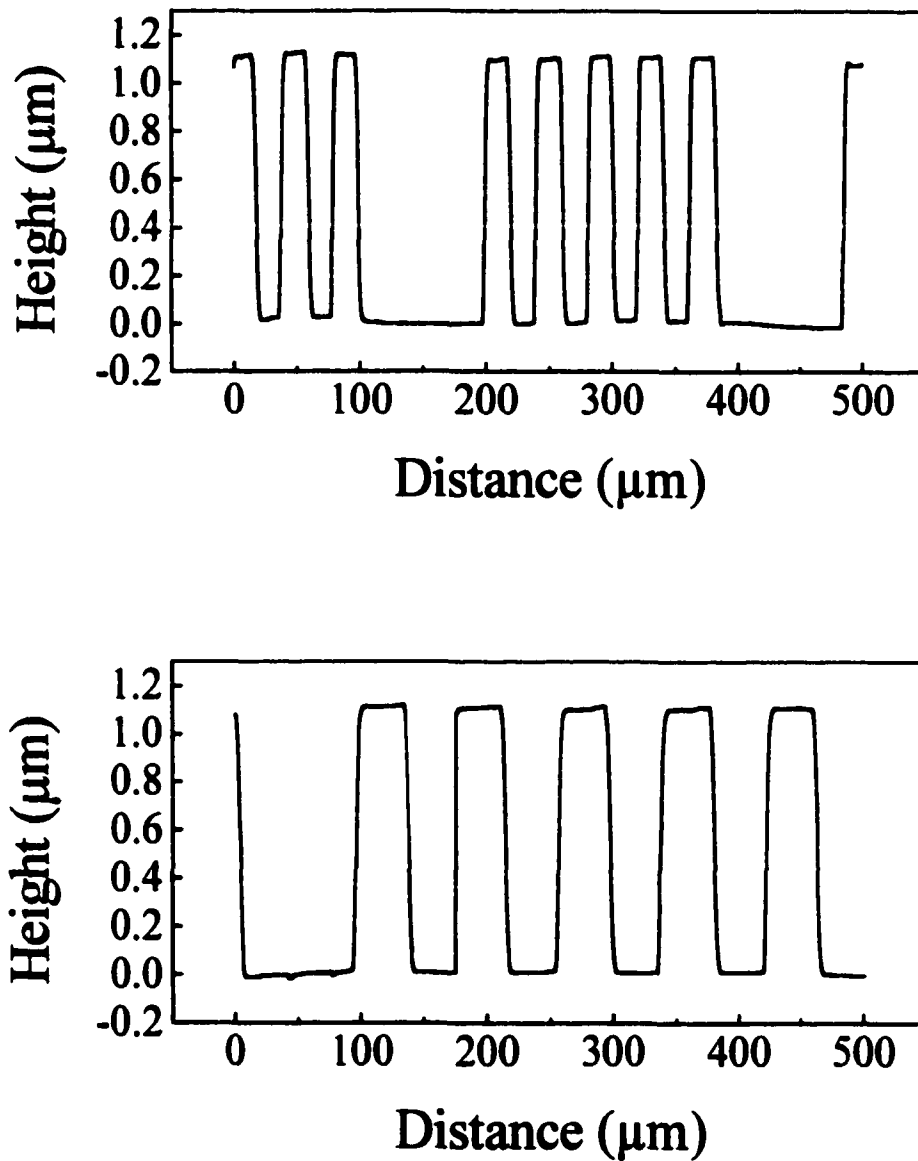
Unlike the *ex situ* mask fixture, we observed some scratches on some of the samples grown with the *in situ* mask fixture (Fig. 5-25). We believe that this was caused by the slight movement of the mask over the substrate while we placed or removed the mask holder. We also observed that there were none or very few scratches on the wafer surfaces when the new mask was used while the number of the scratches increased when we used the mask for the second or third time. The scratches were traced to the deformation of the metal mask after use. The mask patterned region became rough and it scratched the substrate surface. Hence we limited the times of using the mask to just once or twice. It should be noted that this limitation, although increasing the cost of the process, was not considered severe by our collaborators at Rockwell Science center

Table 5-3 summarizes the growth results using the *in situ* mask fixture.

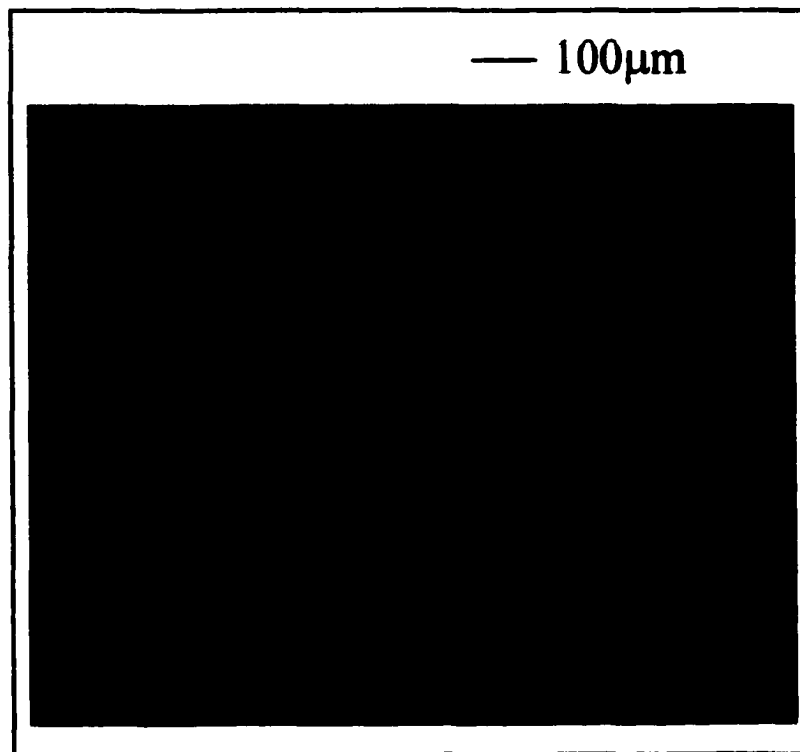
As can be seen, the three samples grown with a new mask have none or very



**Fig. 5-23: Nomarski micrographs of the CdTe square arrays of sizes and separations of 20 and 40  $\mu\text{m}$ ..**



**Fig. 5-24. Surface profiles of the CdTe squares arrays shown in Fig.5-23.**



**Fig. 5-25. Nomarski micrograph of the CdTe mesas grown with the in situ mask fixture. The surface was scratched by the deformed metal mask.**

<b>Sample No.</b>	<b>A642</b>	<b>A655</b>	<b>A663</b>	<b>A666</b>	<b>A669</b>	<b>A696</b>
<b>Mask</b>	New	Second time	New	Second time	Third time	New
<b>Rotation</b>	No	No	No	No	No	No
<b>Side Wall Appearance</b>	Non-symmetric	Symmetric	Non-symmetric	Symmetric	Symmetric	Symmetric
<b>Sidewall Width(<math>\mu\text{m}</math>)</b>	4-6 6-8	3.6-6.8	4.4-5.2 8.4-10	4-6.4	4.4-6.4	4-4.8
<b>Height(<math>\mu\text{m}</math>)</b>	~1.4	1.4	1.2-1.3	1.1	1.1	1.1
<b>Mesa Top</b>	flat	flat	flat	flat	flat	flat
<b>Scratches</b>	a few	a lot	one	a lot	a lot	None

Table 5-3. Summary of the growth results using the in situ mask fixture.

few scratches. From the table, we can also observe that the side walls of the mesas are sometimes not symmetric. We found out that the symmetry of the mesa pattern mostly depends on the three springs in the mask holder which help press the mask against the substrate: the more uniform the springs, the better the pattern definition. When the springs are new and the mask is placed flat and in intimate contact with the substrate, the resulting mesas are symmetric and the side walls are abrupt. Sample A696 is an example in which both the springs and the mask are good and the results are excellent. The mesa height variation shown in the table is due to the flux variation from run to run.

#### **5-4. Summary**

A shadow mask SAE growth technique has been developed using both *ex situ* and *in situ* mask fixtures. The *ex situ* mask fixture is valid for one step SAE growth and the whole structure will be patterned in the same manner since the mask is fixed on the substrate at the beginning of the growth. The *in situ* mask fixture, however, provides more versatility. The mask can be placed on the substrate in the middle of the growth process. Patterned layer can be grown within the sample structure and multiple step SAE with different mask or mask arrangement can be performed for more complex device structure fabrications. Since the *in situ* mask fixture provides more

**advantages over ex situ mask fixture for applications in device fabrication using shadow mask SAE, the studies described in the subsequent chapters were performed using the *in situ* mask fixture.**

**References:**

1. W.T. Tsang and M. Ilegems, *Appl. Phys. Lett.* 35, 792 (1979)
2. N. C. Giles-Taylor, R.N. Bicknell, D.K. Blanks, T.H. Myer and J.F. Schetzina, *J. Vac. Sci. Technol. A.* 3, 76 (1985)

## CHAPTER 6

### **In Situ Fabrication of Au/CdTe Device Like Structure – Application of Shadow Mask SAE in Device Processing**

#### **6-1. Introduction**

Conventional device structure fabrication typically involves the patterning of the flat epilayer into discrete structures and deposition of the metal contact on top of these patterned structures to fabricate individual device units. It is a complex process and many procedures are involved such as removing the samples from the vacuum growth system, coating with photoresist material, UV exposure by mask aligner, dry and/or wet etching, and reintroduction of the samples into the metallization chamber for metal contact deposition, etc. In the case of the HgCdTe detector array fabrication, it involves the post growth reticulation of the flat HgCdTe epilayers into square arrays and metal contact fabrication on the HgCdTe square arrays. Various photolithography and surface cleaning procedures are needed. Its complexity limits the producibility of HgCdTe detector arrays.

It has already been shown that shadow mask SAE is useful in the *in situ* patterning of the epilayers during material growth. The *in situ* mask fixture also allows us to place and remove the mask within the vacuum

system therefore multiple step SAE and *in situ* deposition of patterned metal contacts can be performed. To take full advantage of the *in situ* mask fixture and explore the feasibility of the shadow mask SAE technique for *in situ* device structure processing, we performed the *in situ* fabrication of Au/CdTe detector-array-like structures by combining the *in situ* patterning and *in situ* metallization. CdTe square arrays were grown in the MBE chamber using the shadow mask for CdTe (*in situ* patterning) and the patterned CdTe epilayers were then transferred into a metallization chamber within ultrahigh vacuum for patterned Au deposition using another shadow mask for Au (*in situ* metallization). Besides the greatly simplified fabrication processes, the *in situ* metallization provides additional benefits due to the reduced chance of contamination.

In this chapter, I will introduce the *in situ* fabrication of Au/CdTe detector-array-like structures using the *in situ* mask fixture. The advantages of the *in situ* metallization procedure are investigated and presented. The *in situ* fabrication process for Au/CdTe structures will be evaluated and the feasibility of the shadow mask SAE for greatly simplified *in situ* device structure processing will be addressed.

## **6-2. Optimization of the metallization**

Before we performed the *in situ* metallization process, we tested the performance of our metallization chamber by depositing Au on GaAs substrates and flat CdTe epilayers. Smooth, shiny golden surfaces were obtained. One problem we identified was that it was hard to control the metal deposition rate by adjusting the electron gun filament current. We therefore fixed the quartz crystal thickness monitor (Leybold Inficon Inc.) installed in the metallization chamber. By calibrating the tooling factor of the monitor, we obtained comparable thickness from both the thickness monitor and alpha-step 200 surface profilometer. Using the thickness monitor, we can better control the metal deposition rate and metal layer thickness.

### **6-3. Evaluation of the *in situ* metallization procedure**

The quality of the *in situ* metallization procedure was evaluated by the adhesion test and by secondary ion mass spectrometry (SIMS). The evaluations were performed on flat Au/CdTe layers. Three samples were investigated by these two techniques. One sample (A904) underwent *in situ* metallization, that is, after the CdTe epilayer was grown it was transferred in UHV to the metallization chamber for Au deposition. For the other two samples, the CdTe epilayers were removed from UHV and exposed to air after growth. One of them (A864) was exposed for 4 hours and then reintroduced into the metallization chamber for Au deposition. The other

sample (A891) was etched with HCl after 24 hour air exposure, rinsed, dried and immediately reintroduced into the metallization chamber for Au deposition. This HCl etching step was adopted because it is one of the surface cleaning steps used before metal contact layer deposition in the conventional HgCdTe device fabrication process.

The scotch tape adhesion test was performed to qualitatively measure the Au adhesion on the CdTe surface. Sample A864 having Au deposition after the CdTe epilayer was exposed to the air during 4 hours did not pass the test, which means that the Au layer was peeled off by the scotch tape. Sample A904 with the Au layer deposited *in situ* (without being exposed to the ambient) and sample A891 which was exposed to air and etched by HCl have better adhesion properties. In these, the Au was not peeled off by the scotch tape.

SIMS studies were carried out to evaluate the Au-CdTe interface contamination. The same three samples that underwent the scotch tape adhesion test were investigated using an Atomika 3000-30 SIMS system. A 20 nA 2 KeV argon primary ion beam was employed at 30° off-normal incidence. The negative secondary ions, Cl<sup>-</sup>, O<sup>-</sup>, C<sup>-</sup>, F<sup>-</sup>, CN<sup>-</sup>, were detected in the depth profile mode. The primary ion beam was rastered over a square area of 0.75mm width. The signal was collected from a gated square region

comprising 40% of the linear dimension of the crater to reduce crater edge effects. Substrate charging effect was negligible.

Fig. 6-1 shows the SIMS depth profiles for these three samples. Although Au, Cd or Te could not be monitored as an indication of the interface using our current instrument setup, we made sure that for all the samples we sputtered beyond the interface region. Besides the presence of the contaminant peaks at the interface, the presence of the interface could be established by a drop in the oxygen background level in going from the Au to the CdTe material due to the different ionization probabilities and sputtering rates in the different matrices. As shown in Fig. 6-1a, sample A864 with the exposed interface exhibits contamination in the form of C, N, Cl, F and a slight amount of O at the Au-CdTe interface. Based on the detection limit established in the polymeric samples under identical conditions, the carbon contamination is estimated to be on the order of a monolayer. For chlorine, the detection sensitivity is much higher, so its contamination level is actually lower than that of carbon. Sample A891, which was exposed and then etched with HCl, exhibits primarily a chlorine peak (Fig. 6-1b). The chlorine peak is believed to be caused by the residue of HCl etchant since air contamination by chlorine usually appears simultaneously with fluorine, which is undetectable here. By contrast, the SIMS depth profile for sample A904

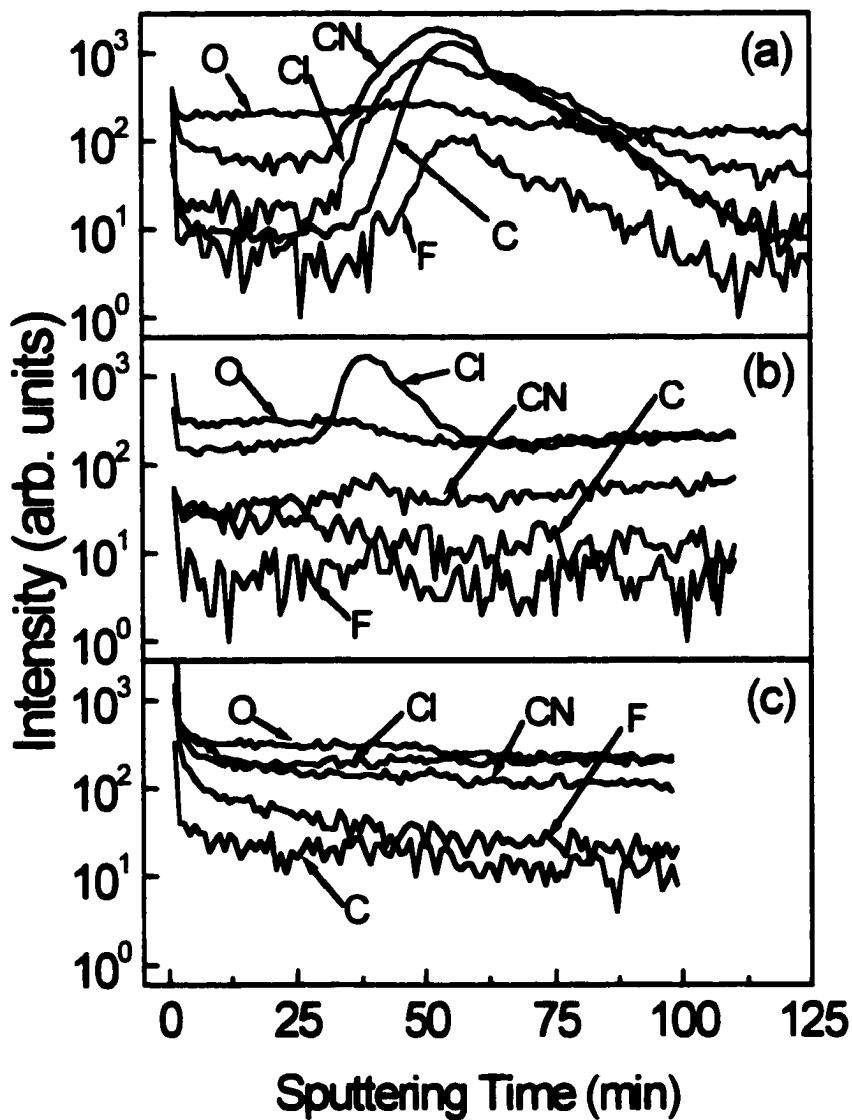


Fig. 6-1. SIMS depth profiles for the Au/CdTe structure:  
 (a) from sample A864 with the interface exposed to air for 4 hours;  
 (b) from sample A891 with the interface exposed and etched by HCl;  
 (c) from sample A904 with *in situ* Au deposition.

which has *in situ* metallization indicates that, within our detection limit, there is no detectable contamination of any of these ions at the interface (Fig. 6-1c). The carbon contamination in the *in situ* grown sample is at least 3 orders of magnitude lower than sample A864 (less than 0.001 monolayer) and below our detection limit.

The SIMS and adhesion test results indicate that the *in situ* metallization can reduce the interface contamination and improves the metal adhesion properties. Although HCl can etch and clean the exposed surface by removing C, O and N contamination, it may also introduce chlorine at the interface, which may affect the metal adhesion properties and possibly the electrical properties as well. Besides HCl etching, current HgCdTe detector array fabrication incorporates a plasma asher cleaning step immediately prior to the metal deposition to remove organic contamination. Our results suggest that neither of these steps is necessary with *in situ* metallization.

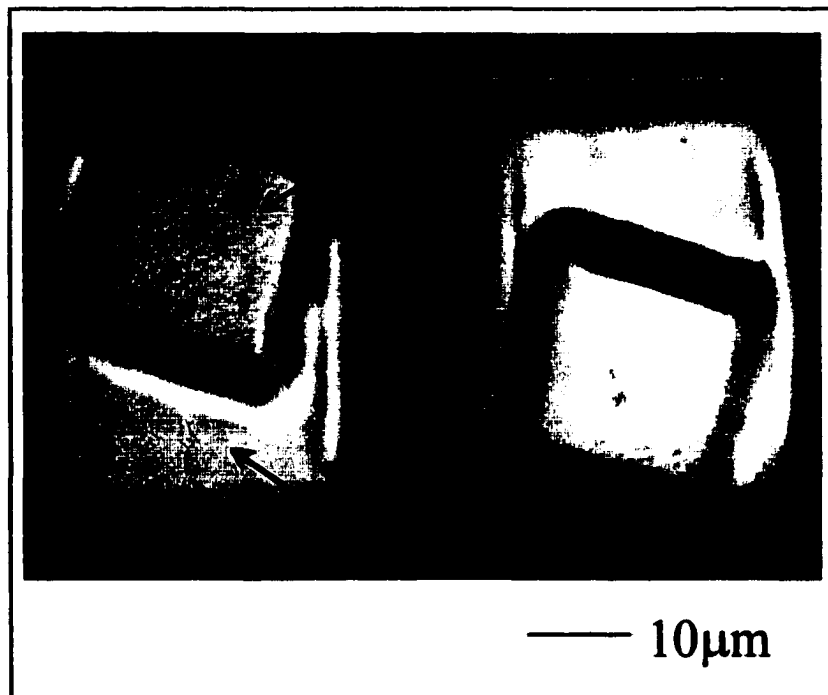
#### **6-4. In situ fabrication of Au/CdTe detector-array-like structures**

After assessing that *in situ* metallization is beneficial, we fabricated Au/CdTe detector-array-like structures using an all *in situ* process with the *in situ* mask fixture. To avoid the material cross contamination, two separate masks and mask holders were utilized, one for CdTe growth and one for metal deposition. The CdTe substrate was first transferred into the growth

chamber for oxide desorption. After that, the mask holder for CdTe growth was transferred in and placed on the substrate within UHV. The CdTe mask holder was removed after SAE growth and the substrate with the patterned CdTe mesas was transferred into the metallization chamber in vacuum. Another mask holder for Au deposition was placed on the patterned CdTe epilayer and patterned Au deposition was carried out at room temperature.

#### **6-5. Evaluation of the *in situ* processing of Au/CdTe detector-array-like structure**

Fig. 6-2 shows an optical micrograph of the CdTe mesas covered with Au pads obtained with the all *in situ* process demonstrating the feasibility of the shadow mask SAE for *in situ* device processing. Excellent pattern definitions of both the CdTe mesas and Au pads were obtained. Using conventional device processing technique, the fabrication of a comparable Au/CdTe detector-array-like structure would require complex procedures. After the CdTe flat layer is grown, it would be removed from the UHV growth chamber and covered with photoresist. Photolithography and etching would be performed to define the CdTe square arrays. The chemical cleaning would be needed to insure a clean surface for metallization before the sample with the CdTe square arrays would be introduced into the metallization chamber for Au deposition. By contrast, our *in situ* processing only employ



**Fig. 6-2. Nomarski micrograph of the Au/CdTe structures fabricated with an all in situ process using the in situ mask fixture.**

two steps, MBE growth of the CdTe square arrays and the *in situ* deposition of patterned Au contact. It greatly simplifies the fabrication process. Furthermore, the *in situ* metallization provides clean metal-semiconductor interface which results in good adhesion properties and possibly good electrical properties as well.

However, it should be noted that a registry problem was encountered. As shown in Fig. 6-2, although the Au pads are on top of the CdTe mesas, the two are not well aligned. This is because the holes in the mask are slightly larger than the posts in the substrate holder. The mask therefore can move slightly which results in the misalignment of the layers grown sequentially. Attempts have been made by improving the mechanical design of the mask fixture to improve the registration between masks in multiple step SAE and will be addressed in Chapter 9.

#### **6-6. Feasibility of the shadow mask SAE for *in situ* device processing**

The *in situ* fabrication of Au/CdTe detector-array-like structures demonstrates that shadow mask SAE is a promising approach for *in situ* device structure processing. It can greatly simplify the process and improve the metal-semiconductor interface. The registration of different patterned epilayers associated with our mask fixture design for the multiple step SAE might be an issue limiting its application in some device structures requiring

stringent registration. Therefore further improvement in the *in situ* mask fixture design is needed to make it more applicable for *in situ* device processing. We will present the approaches to enhance the performance of the *in situ* mask fixture in Chapter 9.

## CHAPTER 7

### **Integration of ZnCdSe Quantum Wells on a Single Substrate –**

### **Application of Shadow Mask SAE in Device Integration**

#### **7-1. Introduction**

Semiconductor lasers and light emitting diodes (LEDs) emitting in the visible spectrum have potential applications in high density digital recording, full color display and white light sources. Currently, LED-based full color display panels use different materials on different substrates for the three primary colors: red, green and blue (R-G-B). Green-blue lasers and LEDs made from the ZnSe based II-VI material systems<sup>[1,2]</sup> and from the GaN based III-V material systems<sup>[3]</sup> have been reported, while red lasers and LEDs are available from GaP based III-V materials.<sup>[4]</sup> It would be difficult to combine these materials on a single substrate for device integration since each of these materials require drastically different growth conditions and starting substrates.

The wide band gap (Zn,Cd,Mg)Se material system developed in our lab is a new quaternary material system that has potential applications in semiconductor lasers and LEDs.<sup>[5]</sup> The  $Zn_xCd_yMg_{1-x-y}Se$  layers can be grown lattice matched to InP substrate with a wide range of band gaps, from 2.18 to

~3.5 eV. Fig. 7-1 shows the relationship between the bandgap and lattice constant for these alloys. By using  $\text{Zn}_x\text{Cd}_y\text{Mg}_{1-x-y}\text{Se}$  layers of different bandgap as the cladding and waveguiding layers and a ZnCdSe layer as a active layer, we can design totally lattice matched or pseudomorphic laser and LED structures with emission throughout the entire visible spectrum, from blue to green to red. These structures grown on InP substrates also allow the growth of a lattice matched ZnSeTe alloy that can be easily doped *p* type for the formation of the ohmic contact without introducing defects due to lattice mismatch. Thus, red, green and blue emission can be achieved from almost identical structures where only the quantum well (QW) thickness and/or composition are varied.<sup>[6]</sup> Therefore, integrated full color display devices can be considered to be constructed by simply integrating ZnCdSe/ZnCdMgSe QWs.

We have previously grown laser structures based on this (Zn,Cd,Mg)Se material system for both electrical injection and optical pumping. Fig. 7-2 shows the separate confinement heterostructure (SCH) single QW laser structure. For optically pumped laser, none of the layers were doped and a ZnSe cap layer was used instead of a ZnSeTe cap layer. Figure 7-3 shows the threshold lasing spectra for three optically pumped lasers with emission wavelengths at 497, 540 and 604nm at room

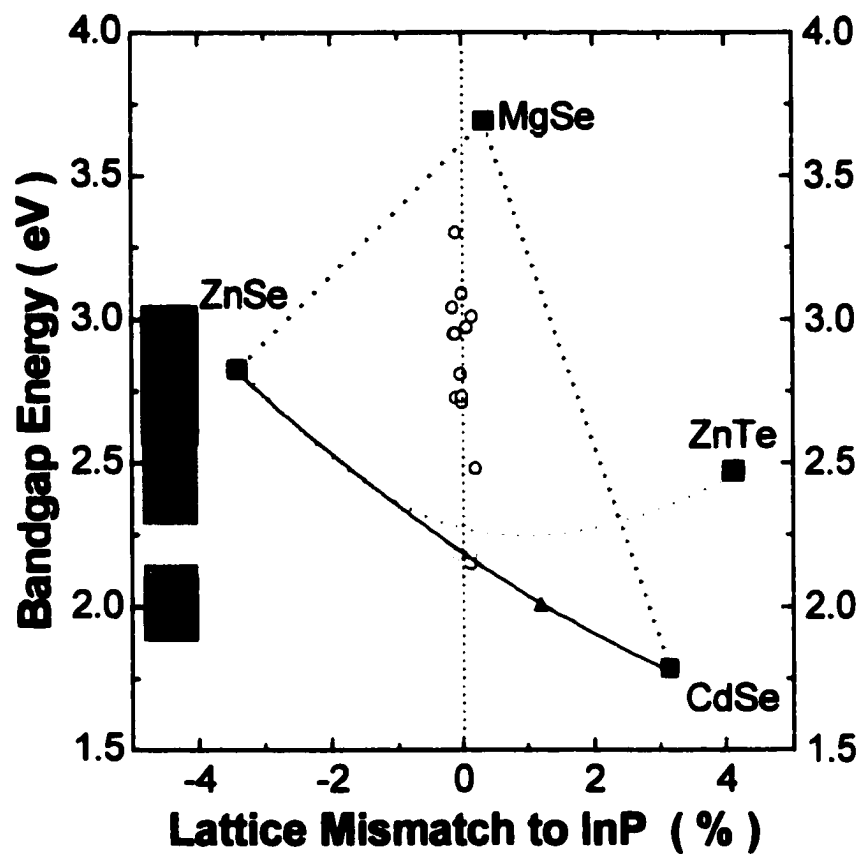


Fig. 7-1. The bandgap energy of the (Zn,Cd,Mg)Se alloys and their lattice mismatch to the InP substrate.

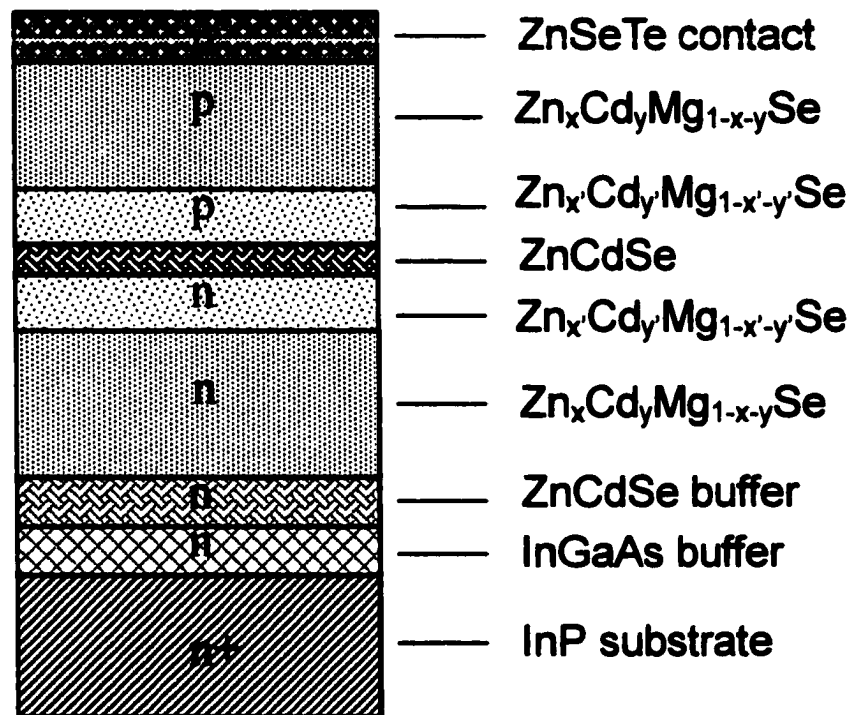
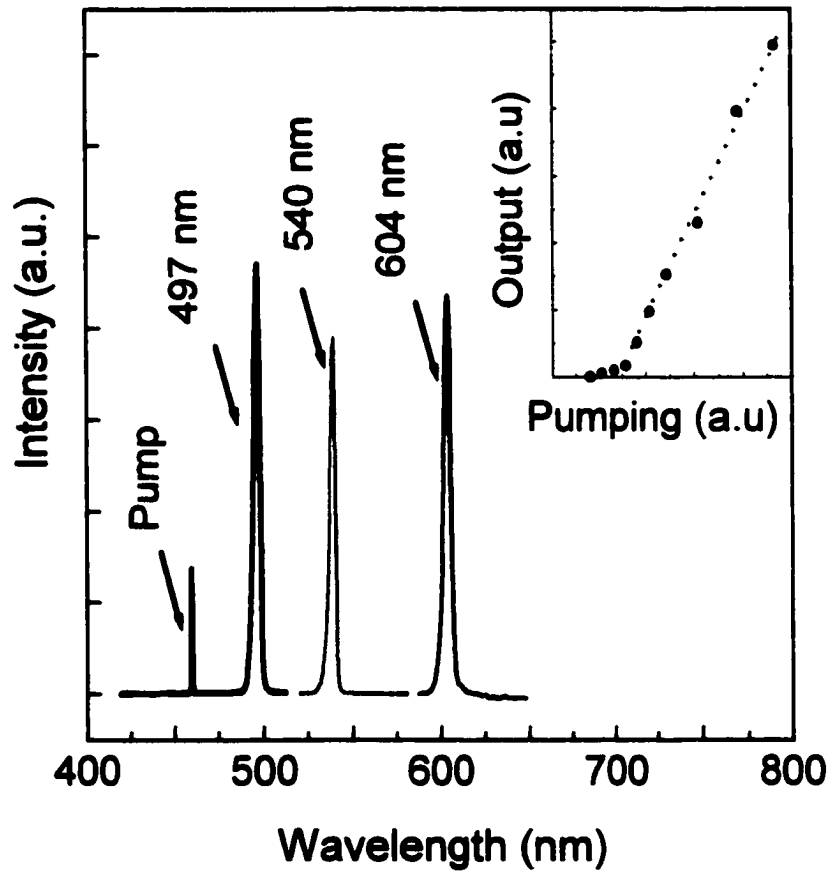


Fig. 7-2. Schematic of the separate confinement heterostructure single QW laser structure.



**Fig. 7-3. Threshold lasing spectra for the red, green and blue optically pumped lasers. The inset shows their typical turn-on characteristics.**

temperature, covering the range from blue to red. The inset in Fig. 7-3 shows the typical turn-on characteristic obtained with these structures. Although grown separately on three different InP substrates, these three structures are identical except for the composition and/or thickness of the ZnCdSe QW. Table 7-1 summarizes the ZnCdSe QW parameters of these three laser structures. The QW thickness and lattice-mismatch to InP were estimated from measurements on a thick reference layer grown under the same condition as the QW.

More recently we have succeeded in the n type doping of ZnCdMgSe and ZnCdSe layers<sup>[7]</sup> using chlorine as the dopant. Highly p type doped ZnSeTe contact layer using nitrogen as the dopant has also been obtained<sup>[8]</sup>. However, we are still limited by the low p type doping level in the ZnCdMgSe waveguiding and cladding layers and no satisfactory results with electrical injection laser have been obtained.

However, we succeeded in fabricating (Zn,Cd,Mg)Se based LEDs even with the low p-type doped ZnCdMgSe barrier layers. Fig. 7-4 shows the schematic of the LED structure. Blue, green, yellow and red LEDs have been fabricated<sup>[9]</sup> and their electroluminescence (EL) spectra are shown in Fig. 7-5. They were grown on separate InP substrates using identical structures where only the ZnCdSe QW thickness and composition were varied. Based on these

<b>Sample</b>	<b>QW thickness (nm)</b>	<b>QW Mismatch (%)</b>	<b>QW Emission wavelength at 77K (nm)</b>
<b>A</b>	<b>2.8</b>	<b>0</b>	<b>473</b>
<b>B</b>	<b>4.0</b>	<b>0</b>	<b>516</b>
<b>C</b>	<b>12.0</b>	<b>1.2</b>	<b>590</b>

**Table 7-1. QW parameters of the red, green, blue laser structures.**

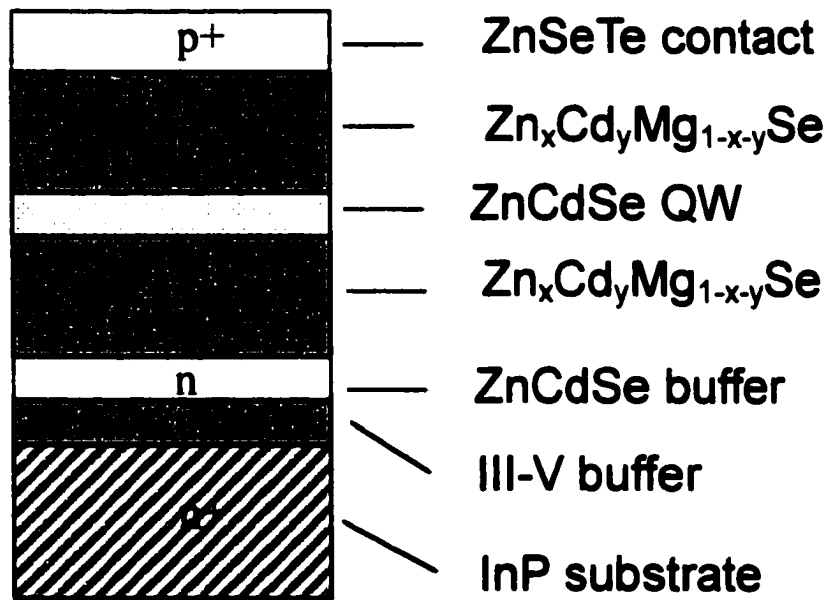


Fig. 7-4. Schematic of the LED structure based on the (Zn,Cd,Mg)Se material system.

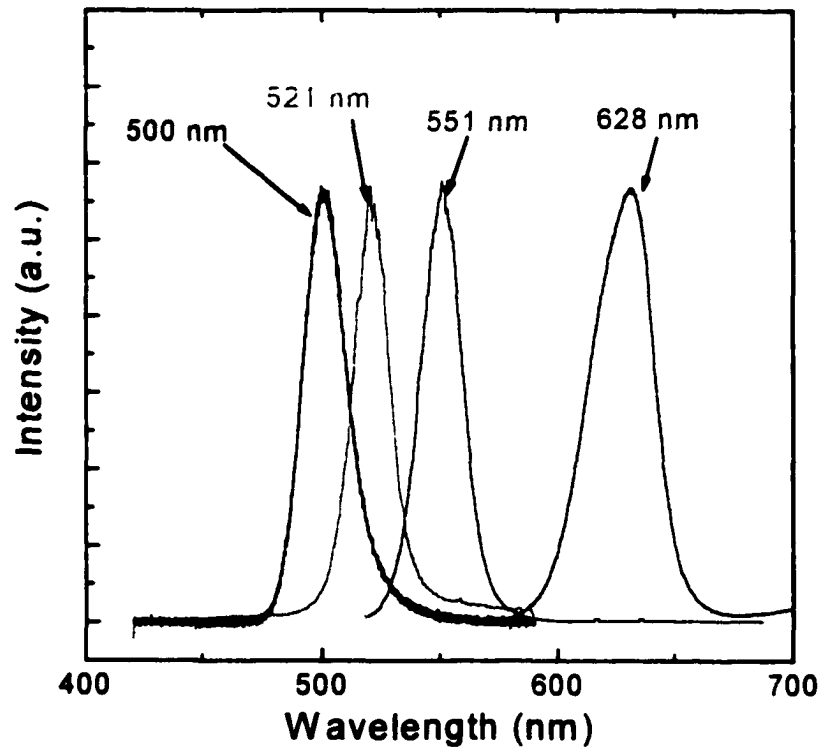
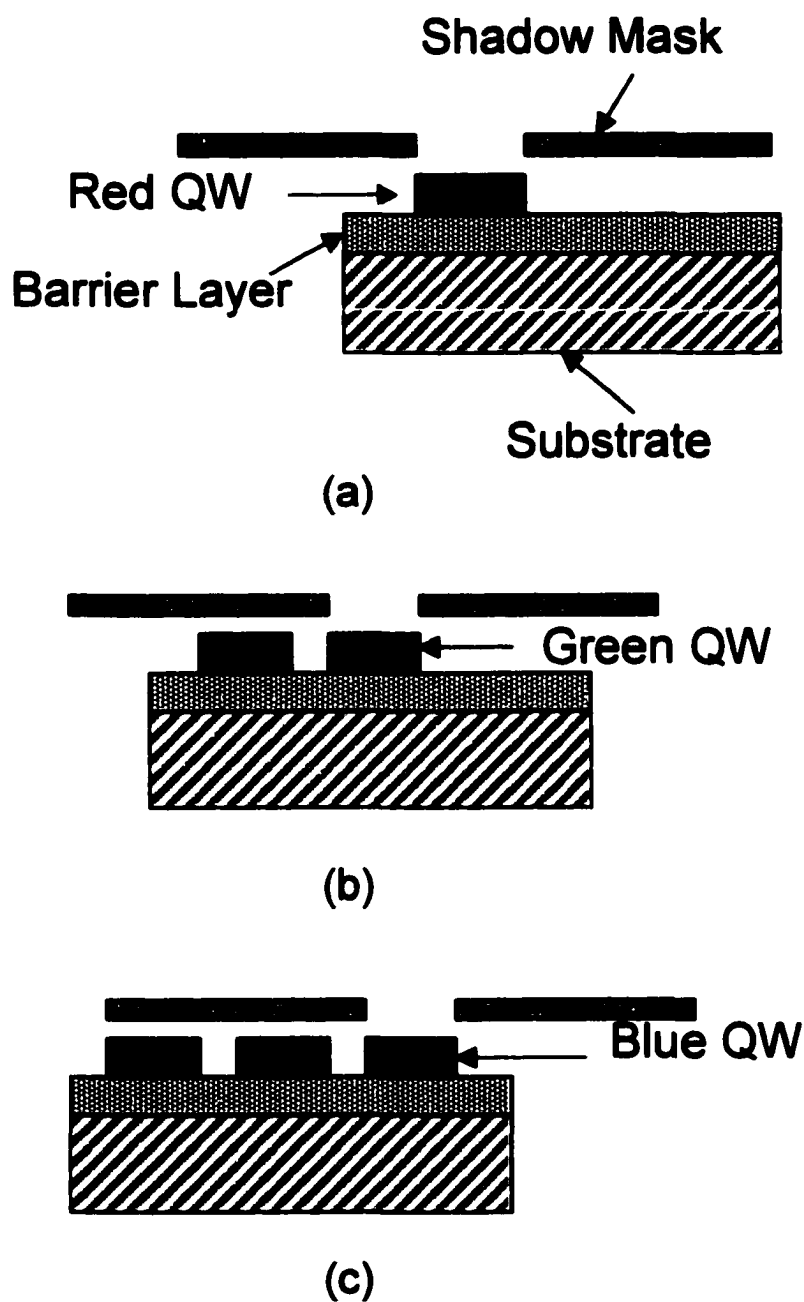


Fig. 7-5. EL spectra of the four color LEDs.

results we embarked on the attempts to integrate the three color (R-G-B) structures on a single InP substrate using selective area epitaxy.

Selective area epitaxy is a feasible approach for the integration of different device structures on the selected areas of the same substrate. It has been shown that by using a new susceptor design in MOCVD that allows relative motion between a GaAs substrate and a GaAs mask, GaAsP and GaAs based multiple detectors with different cutoff wavelengths and multiple color LEDs can be integrated on a single GaAs substrate.<sup>[10,11]</sup> Selective molecular beam epitaxy for integrated *npn/pnp* heterojunction bipolar transistor<sup>[12]</sup> and monolithic integration of multiple wavelength vertical-cavity surface emitting lasers<sup>[13]</sup> have been reported using either a moveable shadow mask or SiN<sub>x</sub> mask.

The mechanical shadow mask SAE technique we developed is promising for achieving integration of R-G-B LEDs based on the (Zn,Cd,Mg)Se material system. By using multiple step SAE, patterned ZnCdSe quantum wells with different thickness and/or composition can be deposited on a single InP substrate to produce one or two dimensional arrays of individually addressable emitters that are fully tunable throughout the visible range. Figure 7-6 illustrates this integration using the shadow mask SAE. After the growth of the flat bottom barrier layer, the shadow mask is



**Fig. 7-6. Illustration of the integration of different QWs on a single substrate.**

placed and one set of patterned ZnCdSe QW can be grown (7-6a). The mask can then be moved relative to the substrate and the second set of patterned ZnCdSe QW can be deposited adjacent to the first one.(7-6b). The third set of ZnCdSe QW can be grown in the same manner as the second one (7-6c). After that, the mask can be removed and the flat top barrier layer and contact layer can be grown on the whole substrate. In this way, multiple color LEDs can be integrated on a single substrate.

In this chapter, I will introduce the growth, characterization and integration of patterned ZnCdSe structures as a demonstration of the shadow mask SAE technique for device structure integration. Our ultimate goal is the integration of (Zn,Cd,Mg)Se based full color displays elements. The *in situ* mask fixture and silicon shadow mask were used for this study. We first performed growth of patterned ZnCdSe thick layers on GaAs substrates using ZnSe buffer layers, which is a simpler material system to grow, to look into the feasibility of the shadow mask SAE technique for the ternary ZnCdSe material. Patterned ZnCdSe/ZnSe QWs were grown and studied. Finally ZnCdSe QWs of different thickness and Cd composition were integrated on a single GaAs and InP substrate with emissions at different wavelengths as a demonstration of the shadow mask SAE technique for the integration of (Zn,Cd,Mg)Se based full color display elements.

## **7-2. Growth and characterization of patterned ZnCdSe thick layers**

The growth of ZnCdSe material involves three source cells: Zn, Cd and Se. They are directed to the substrate at slightly different angles. Therefore mask shadowing effect might be an issue for the SAE growth of this ternary material. To look into the feasibility of the shadow mask SAE technique for the ZnCdSe growth, we first performed growth and characterization of patterned ZnCdSe thick layers on GaAs substrates using ZnSe buffer layers. We moved the Zn, Cd and Se source cells to the center ports of the MBE source flange to ensure better shadow mask SAE growth.

Patterned ZnCdSe layers were grown on GaAs substrates using ZnSe buffer layers. After the growth of  $\sim 3000\text{\AA}$  thick ZnSe buffer layer (following the growth procedure of ZnSe described in chapter 2), the substrate temperature was lowered to  $170^\circ\text{C}$  and the mask was transferred in and placed on top of the ZnSe layer. The substrate temperature was raised back to  $250^\circ\text{C}$  and the patterned ZnCdSe layer ( $\sim 0.5\mu\text{m}$ ) was grown. After growth, the substrate temperature was lowered and the mask holder and the substrate holder were removed from the chamber in sequence. Fig. 7-7 shows the schematic of the patterned ZnCdSe thick layer structure.

Fig. 7-8 is a high magnification SEM micrograph of the end of a  $60\mu\text{m}$  ZnCdSe stripe. It exhibits smooth, featureless surface and well defined side

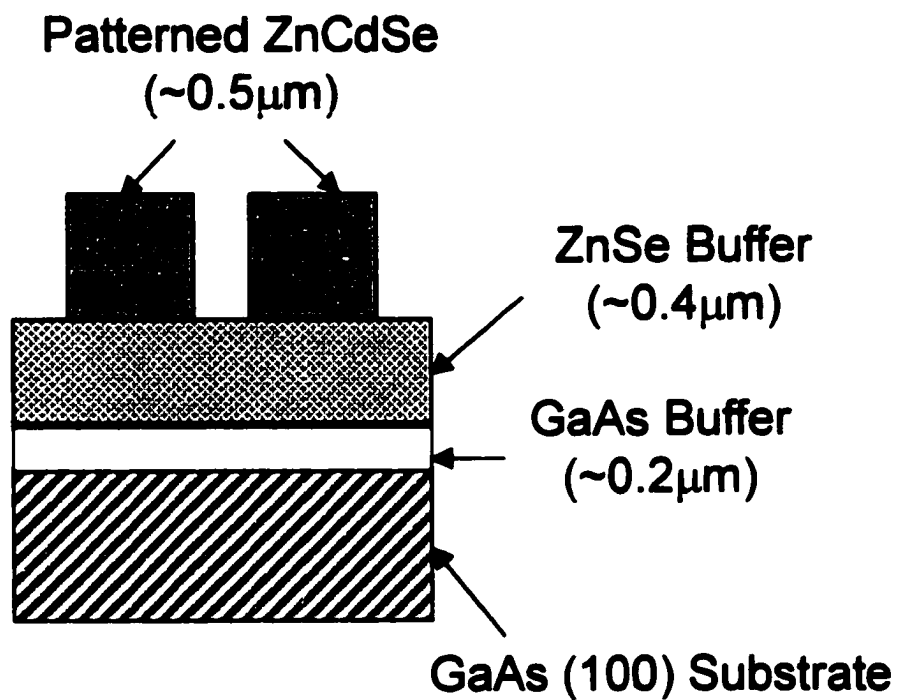
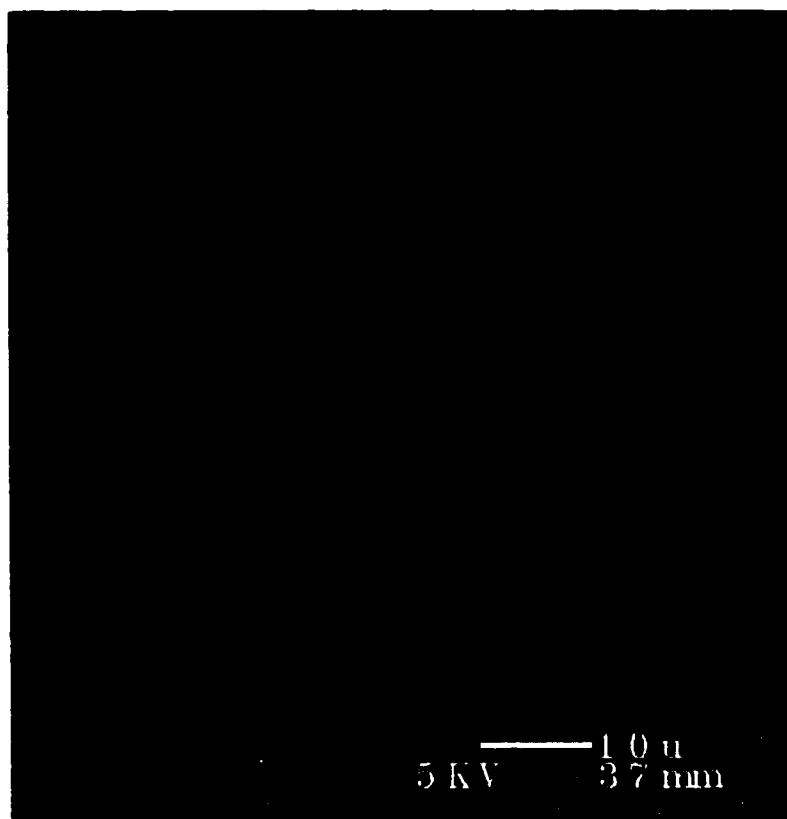


Fig. 7-7. Schematic of the patterned ZnCdSe thick layer.



**Fig. 7-8. SEM micrograph of the end of a 60 $\mu$ m wide ZnCdSe stripe. It is at 60° tilt.**

walls. The ZnSe region covered by the mask during ZnCdSe SAE growth remains clean and featureless, which enables the deposition of subsequent patterned or planar layers without any surface preparation.

Photoluminescence measurements were performed to evaluate the patterned ZnCdSe thick layers. Fig. 7-9 shows a PL spectrum obtained from a 40 $\mu\text{m}$  wide ZnCdSe stripe. The ZnCdSe band-edge emission is at 2.446eV with a full width at half maximum (FWHM) of 23meV. It is only slightly broader than that obtained from a *lattice matched* ZnCdSe layer grown on InP substrate, which is at 18meV range. The small peak near 2.8eV originates from the nearby ZnSe region which was also excited by the laser since the laser excitation spot used in the conventional PL set up is large, at least in the tens of microns range. Fig. 7-10 shows a PL spectrum collected from the region with only ZnSe buffer layer. One sharp ZnSe band-edge emission at 2.767eV with FWHM of 21meV was observed. It is similar as that obtained from flat ZnSe layer grown on GaAs substrate. No deep level emission was observed. These optical measurements indicate that excellent ZnCdSe material have been deposited using shadow mask SAE and that no deleterious effects are caused by the use of the shadow mask on the patterned ZnCdSe or the masked flat ZnSe buffer layer region.

### **7-3. Growth and characterization of patterned ZnCdSe quantum wells**

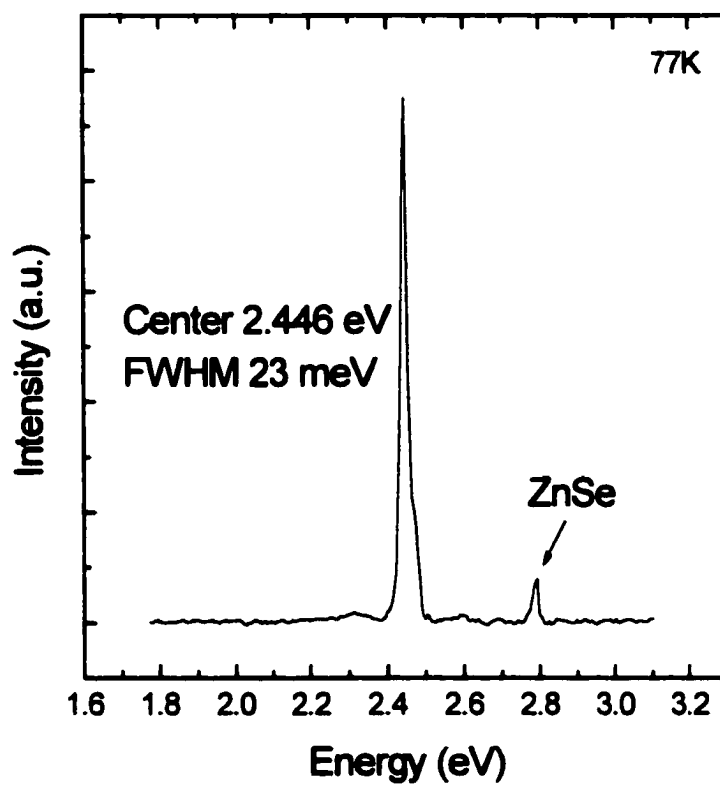


Fig. 7-9. PL spectrum obtained from a 40 $\mu$ m wide ZnCdSe stripe. The small peak near 2.8meV originates from the nearby ZnSe.

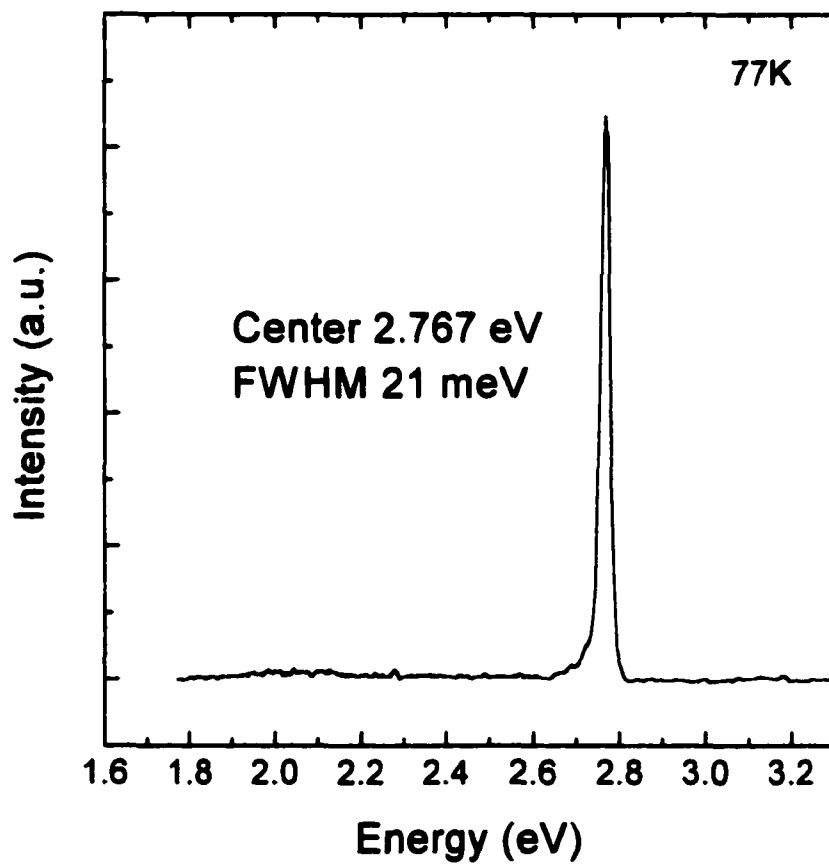
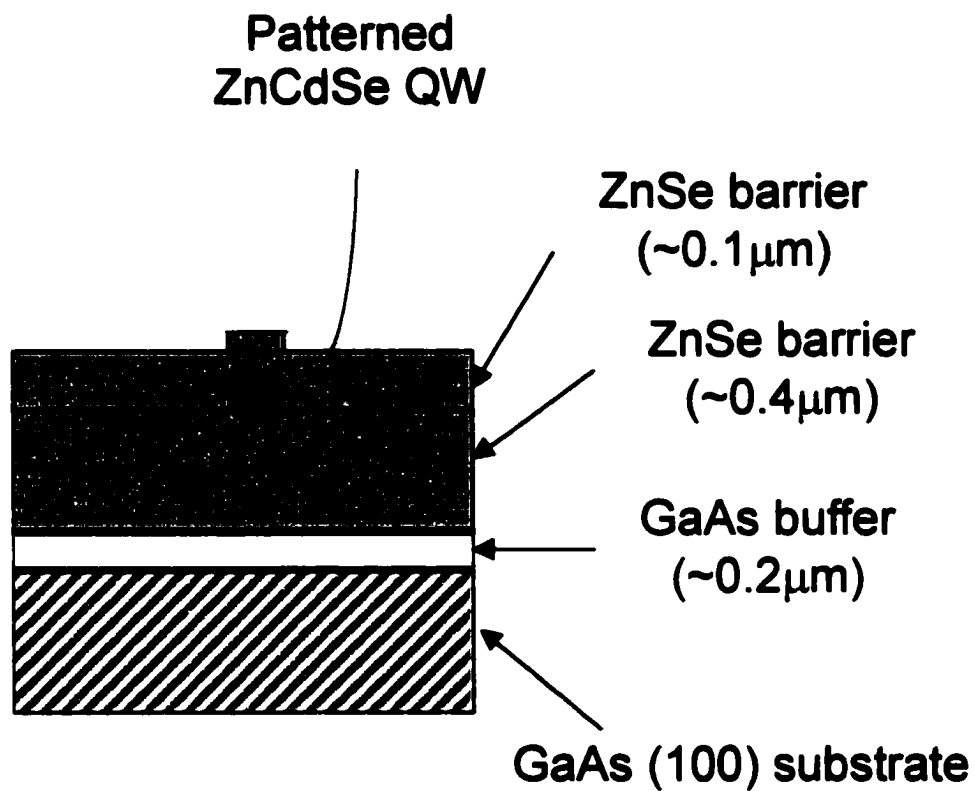


Fig. 7-10. PL of the ZnSe buffer layer which was covered by the mask during the SAE growth of patterned ZnCdSe.

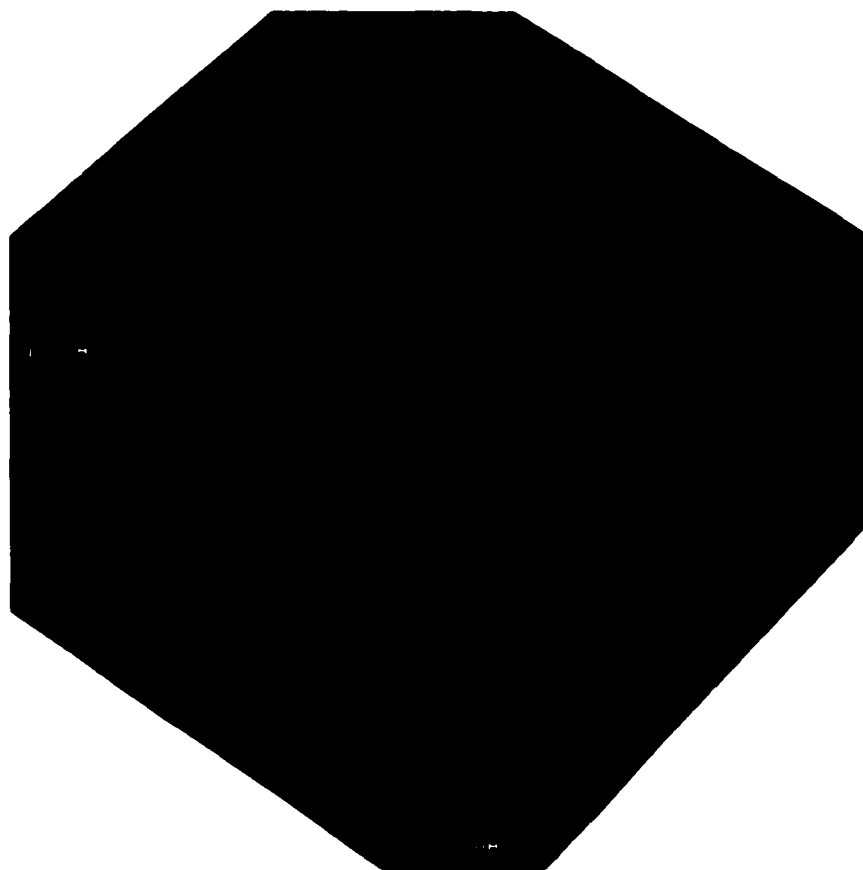
After we obtained good results from patterned ZnCdSe thick layers, we performed growth of patterned ZnCdSe/ZnSe QWs on GaAs substrates.

The growth of ZnCdSe/ZnSe QW is similar to that of the patterned ZnCdSe thick layer, except that the ZnCdSe layer is thinner, in the range of tens of angstroms. After the growth of the patterned ZnCdSe thin layer, the mask holder was removed and a top flat ZnSe barrier layer was deposited. Figure 7-11 illustrates the schematic of the ZnCdSe/ZnSe QW structure.

Although the ZnCdSe QWs are very thin, the patterned structures can still be identified from the top surface by the naked eyes or with an optical microscope due to the interference of the light. This feature makes the subsequent characterizations much easier. AFM surface topography measurements were performed to investigate the pattern definition of these thin patterned QWs. Fig. 7-12 shows an AFM image of a square shaped ZnCdSe QW ( $\sim 140\text{\AA}$  thick) without the top ZnSe barrier layer. It exhibits a well defined shape with sharp sidewalls. The surface of the patterned QWs with and without a ZnSe cap layer show similar lateral and vertical dimensions, suggesting that the patterned QW shape is preserved well after the flat ZnSe layer overgrowth. More detailed studies such as cross sectional transmission electron microscopy (TEM) are needed to fully characterize the growth habits of ZnSe layer on non-planar structure. The surface roughness of



**Fig. 7-11. Schematic of the patterned ZnCdSe/ZnSe QW.**

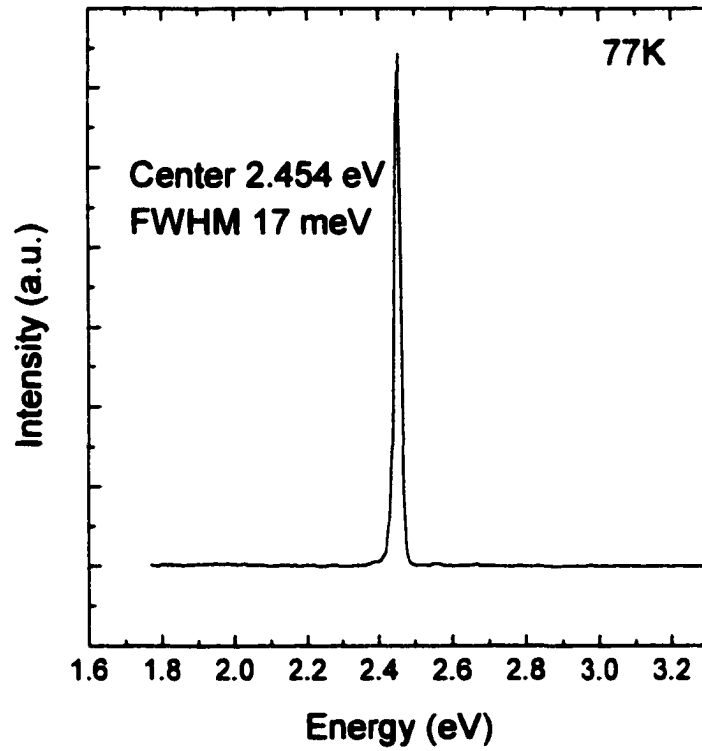


**Fig. 7-12. AFM micrograph of a square-shaped ZnCdSe QW without the top ZnSe barrier layer.**

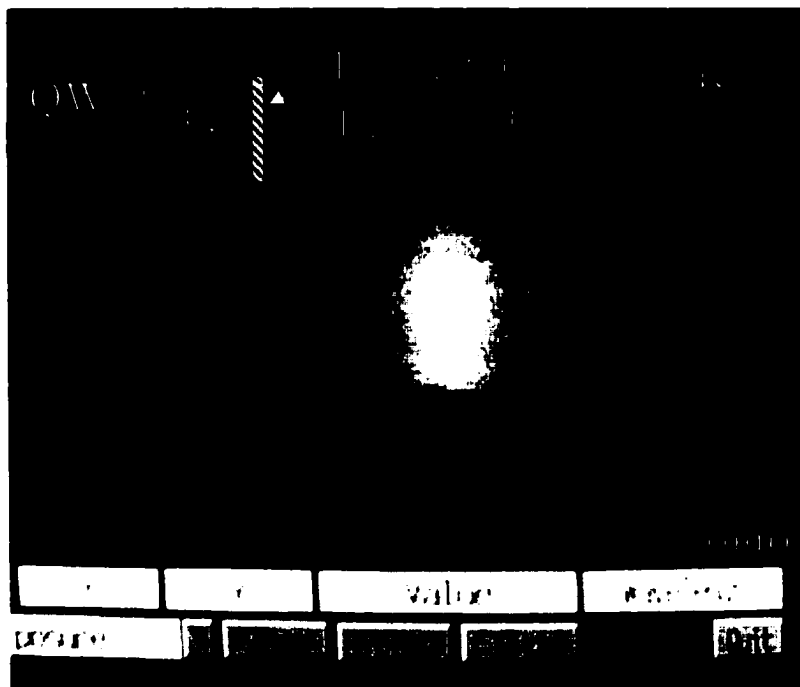
these patterned QWs was measured by AFM and compared to that of corresponding flat layers grown under the same conditions. Comparable surface roughness was observed indicating that the use of the silicon shadow mask does not perturb the growth.

The patterned ZnCdSe QWs exhibit strong and narrow QW emissions as evidenced from the 77K PL measurements. Fig. 7-13 shows a PL spectrum obtained from a 50 $\mu$ m wide ZnCdSe QW stripe (nominally 60 $\text{\AA}$  thick with ~35% Cd) with emission at 2.454eV and a FWHM of 17meV. The QW linewidth is comparable to that obtained from flat QWs grown under similar conditions which is around 16-17meV. A similar PL spectrum as that shown in Fig. 7-10 was observed from the non-patterned (ZnSe only) region. All these results indicate that high quality patterned ZnCdSe QWs have been grown and the use of the shadow mask and the additional growth interruption needed during the placement and removal of the shadow mask did not affect the optical quality of the QWs and the overgrown ZnSe barrier layers.

The uniformity of the QW emission from these patterned structures was assessed using a PL setup employing an OMA as described in chapter 2. Fig. 7-14 shows a PL image obtained at room temperature from a section of a 50 $\mu$ m wide QW stripe. The inset in the figure illustrates where the image was



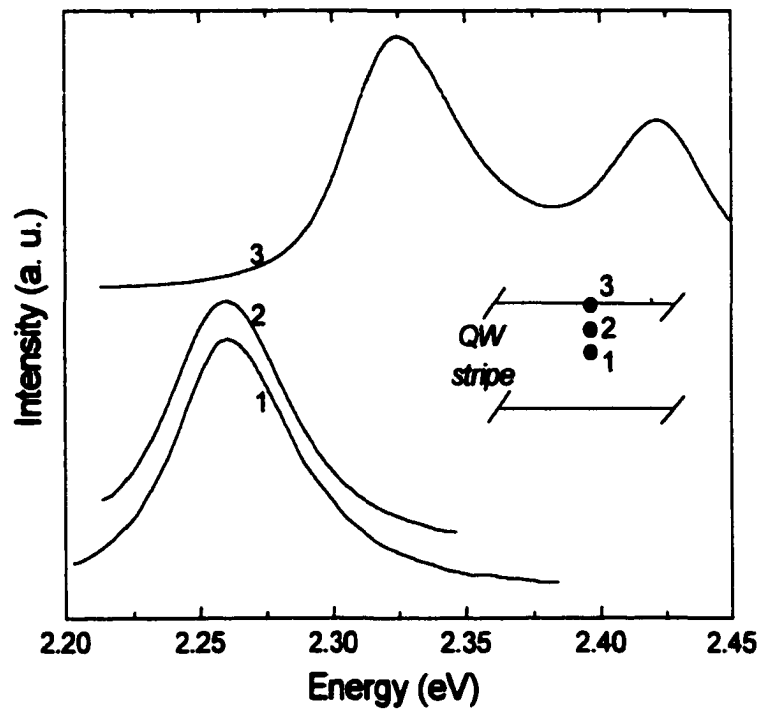
**Fig. 7-13. PL spectrum obtained from a 50 $\mu$ m wide ZnCdSe/ZnSe QW stripe.**



**Fig. 7-14. Spatially resolved PL image obtained from a ZnCdSe/ZnSe QW stripe using the PL set up with OMA.**

recorded. The width of the bar along which the spectra are collected is only  $1\mu\text{m}$ , corresponding to the entrance slit of the OMA. The horizontal axis in the figure is the wavelength (shown) in nm while the vertical direction represents the position along the bar where the measurements were taken. The brightness corresponds to the intensity of the QW luminescence. The QW exhibits uniform emission centered at  $\sim 520\text{nm}$  at room temperature. The ZnSe layer outside the QW region in the same measurement bar has emission wavelength below  $470\text{nm}$ , therefore, its luminescence can not be seen in this image. The spatial resolution of this measurement along the vertical axis is estimated to be less than  $1\mu\text{m}$  based on the magnification lenses used.

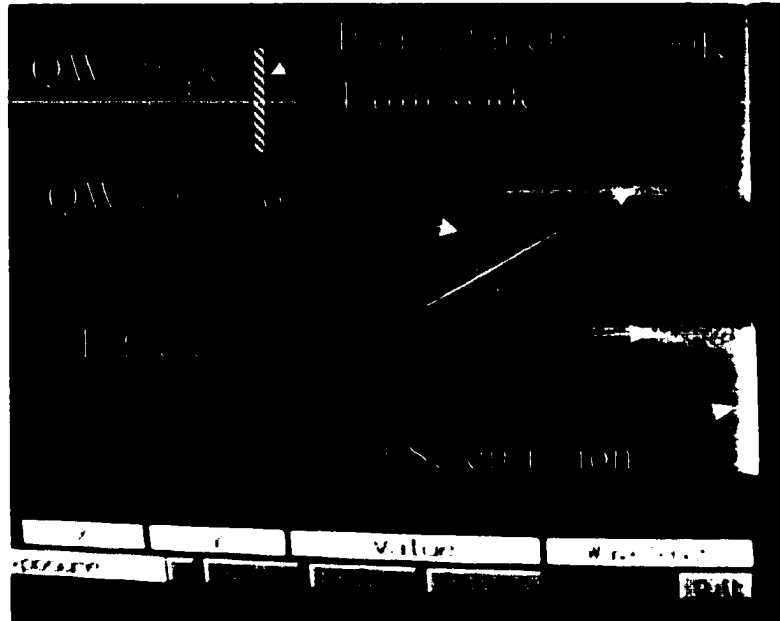
In some of the early samples we observed additional high energy PL peaks near the main QW emission when conventional PL measurements were made. These extra peaks were more prominent in the smaller size features suggesting that they might be associated with the pattern edges. Spatially resolved micro-PL measurements were carried out at  $300\text{K}$  to investigate this phenomenon. Fig. 7-15 shows a set of micro-PL spectra taken from several spots in a  $40\mu\text{m}$  wide ZnCdSe QW stripe. The inset shows a schematic of the stripe pattern indicating the position where the spectra shown in the figure were taken. The experiments show that the additional peaks are only seen



**Fig. 7-15.** PL spectra obtained from several different positions in a  $40\mu\text{m}$  wide ZnCdSe/ZnSe QW stripe exhibiting extra peaks near the pattern edge using a micro-PL setup.

when the PL is collected *exactly* on the pattern edge while the QW emission away from the edge is very uniform and exhibits only one QW emission peak. Fig. 7-16 is a PL image obtained also at room temperature with the OMA from a similar QW stripe having extra PL peaks. Bright “tails” at shorter wavelengths are seen near the edge of the QW stripe indicating luminescence emission at higher energy. No such tails are present away from the edge within the patterned stripe. These data are consistent with those obtained from the micro-PL measurements. Furthermore, by comparing this PL image to the image in Fig. 7-14, a lower QW luminescence intensity in the patterned region is evident suggesting that the extra peaks occur in samples with weaker QW emission. We propose that these high energy peaks may be related to the structural imperfections near the pattern edge due to strain and/or thickness variations and they are associated with sample quality. None of the ZnCdSe QWs grown in the subsequent growth runs exhibit these high energy “tails” while much stronger PL emission are typically seen. This suggests our assessment that the “tails” are only present in poor quality samples and are not an intrinsic problem associated with the shadow mask SAE technique.

#### **7-4. Integration of ZnCdSe/ZnSe QWs on a single GaAs substrate**



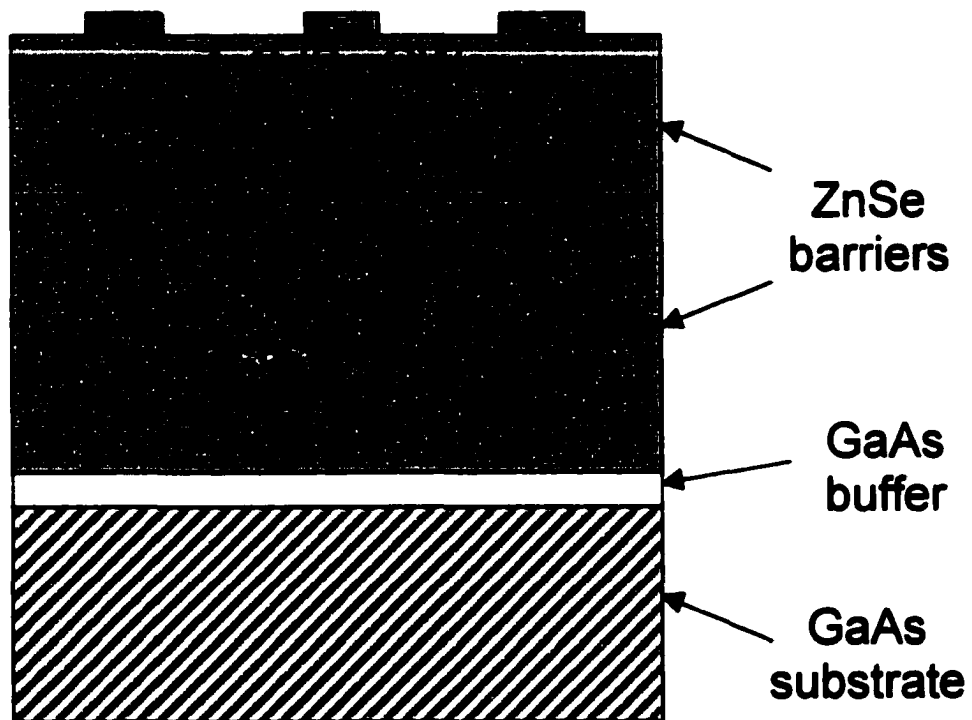
**Fig. 7-16. PL image obtained from a ZnCdSe/ZnSe QW stripe exhibiting high energy peaks near the edge of the stripe.**

The integration of different ZnCdSe QWs was initially performed on a single GaAs substrate using a ZnSe barrier layer. Three sets of patterned ZnCdSe QWs each having different thickness and Cd composition were integrated. It was done by performing sequential SAE during the growth of ZnCdSe thin layers. After the growth of one patterned ZnCdSe thin layer, the substrate temperature was lowered to 170°C and the mask holder was released from the substrate. The mask holder was immediately placed back on the substrate after being rotated 120° relative to the substrate. The substrate temperature was then raised back to 250°C and a second patterned ZnCdSe thin layer with different thickness and Cd composition was deposited on the different area of the same substrate. The third patterned ZnCdSe thin layer was grown in the same manner as the second layer. After that, the substrate temperature was lowered and the mask holder was removed. A top flat ZnSe barrier layer of ~1000Å was grown on the whole wafer after the substrate temperature was raised back to 250°C. The QWs' thickness and composition were adjusted by varying the growth time and Zn flux while keeping Cd flux fixed. The thickness of the QWs is nominally adjusted to be ~60Å. However, their exact composition and thickness are not known since no reference samples were grown.

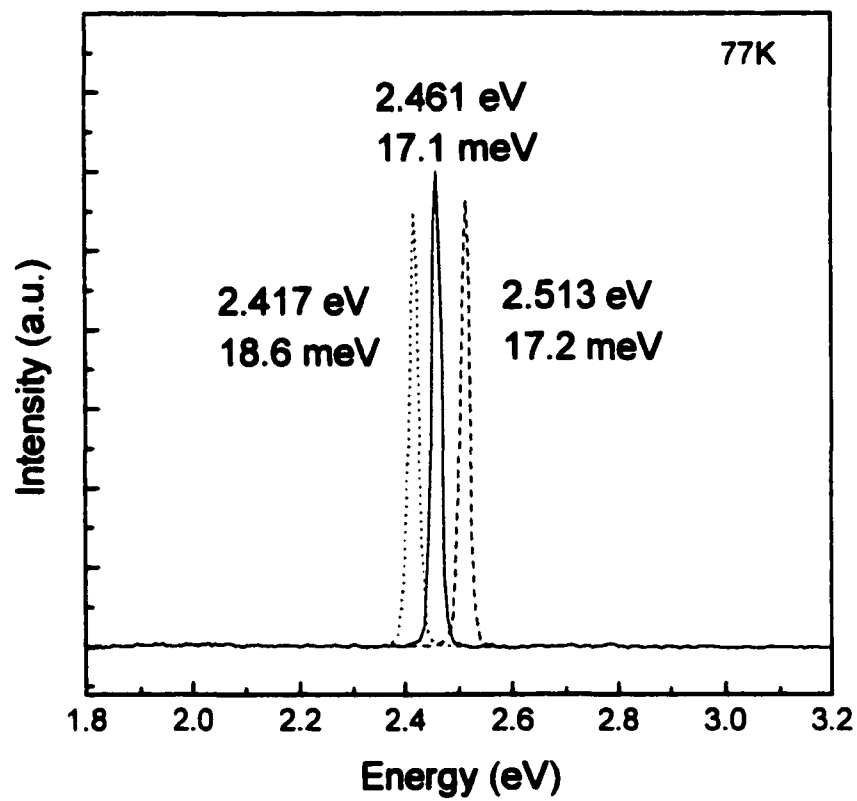
Fig. 7-17 illustrates the schematic of three integrated ZnCdSe/ZnSe QWs. The 77K PL spectra of these QWs are shown in Fig. 7-18. They are centered at 2.513eV, 2.461eV, 2.417eV with FWHM at 17meV, 17meV and 19meV respectively. The PL measurements indicate that the three QWs grown sequentially by multiple step SAE are of comparable good quality. This result demonstrates that the multiple step SAE using a shadow mask is a feasible approach to combine QWs of different composition and/or thickness on a single substrate.

#### **7-5. Integration of full color ZnCdSe/ZnCdMgSe QWs on a single InP substrate**

To demonstrate the application of the shadow mask SAE in integrated (Zn,Cd,Mg)Se based full color displays, we performed integration of ZnCdSe/ZnCdMgSe QWs on a single InP substrate. We first calibrated the growth conditions for lattice matched ZnCdMgSe and ZnCdSe on InP substrates. The Zn and Cd flux were adjusted to fine tune the composition of the ZnCdMgSe and ZnCdSe layers so that they were lattice matched to InP substrate and with desired bandgap. After that, three patterned ZnCdSe/ZnCdMgSe QWs were integrated on a single InP substrate using multiple step SAE. They were grown in the same way as the integration of the three ZnCdSe/ZnSe QWs described above except that the ZnCdMgSe barrier



**Fig. 7-17. Schematic of the three integrated ZnCdSe/ZnSe QWs on a single GaAs substrate.**



**Fig. 7-18.** PL spectra of three integrated ZnCdSe/ZnSe QWs on a single GaAs substrate.

layer was used. Two ZnCdSe QWs were grown having same ternary composition, lattice matched to InP, but with different thickness. They were expected to emit at blue and green region. The third QW was grown with higher Cd concentration in order to obtain red emission.

Fig. 7-19 shows the schematic of three ZnCdSe/ZnCdMgSe QWs integrated on a single InP substrate. 300K PL spectra obtained from these three QWs were shown in Fig. 7-20. They were measured by the micro-PL setup. The QW emissions are centered at around 540, 580 and 630nm with FWHM at ~30nm at room temperature. The two lattice matched ZnCdSe QWs have emission at green and yellow, which are deviated from what we originally designed. It suggests that the growth rate we used for the thickness estimate was not quite accurate. Fig. 7-21 shows a photograph of three square shaped ZnCdSe QWs close to each other on a single InP substrate, exhibiting emission at red, yellow and green. It was taken by camera while the sample surface was exposed to the excitation laser light. The color of the three squares is a little distorted compared to the spectra in Fig. 7-20, possibly due to the exposure of the film.

The integration of different ZnCdSe/ZnCdMgSe QWs on a single InP substrate demonstrates the feasibility of using shadow mask SAE to fabricate integrated full color displays based on the (Zn,Cd,Mg)Se material system. If

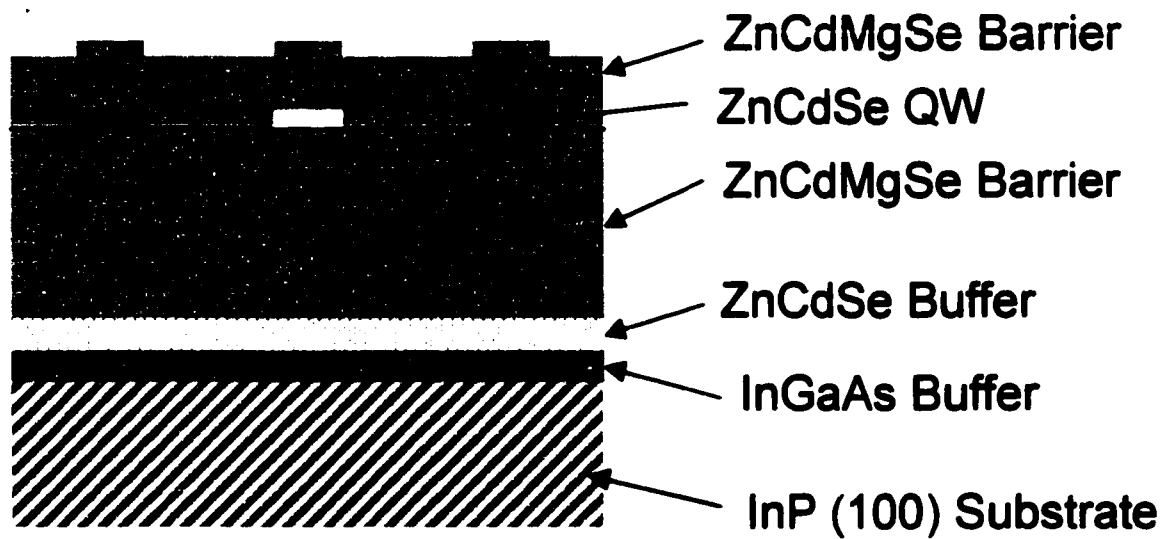
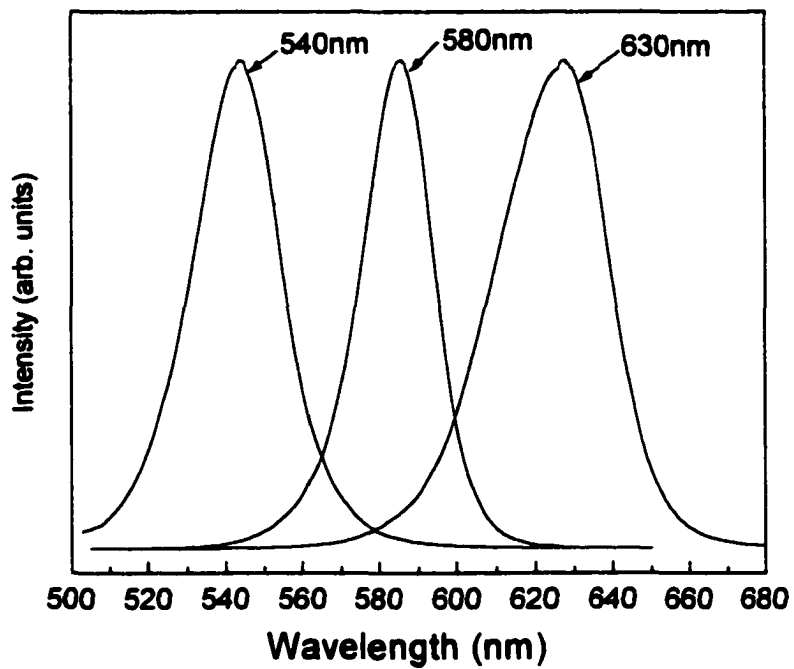
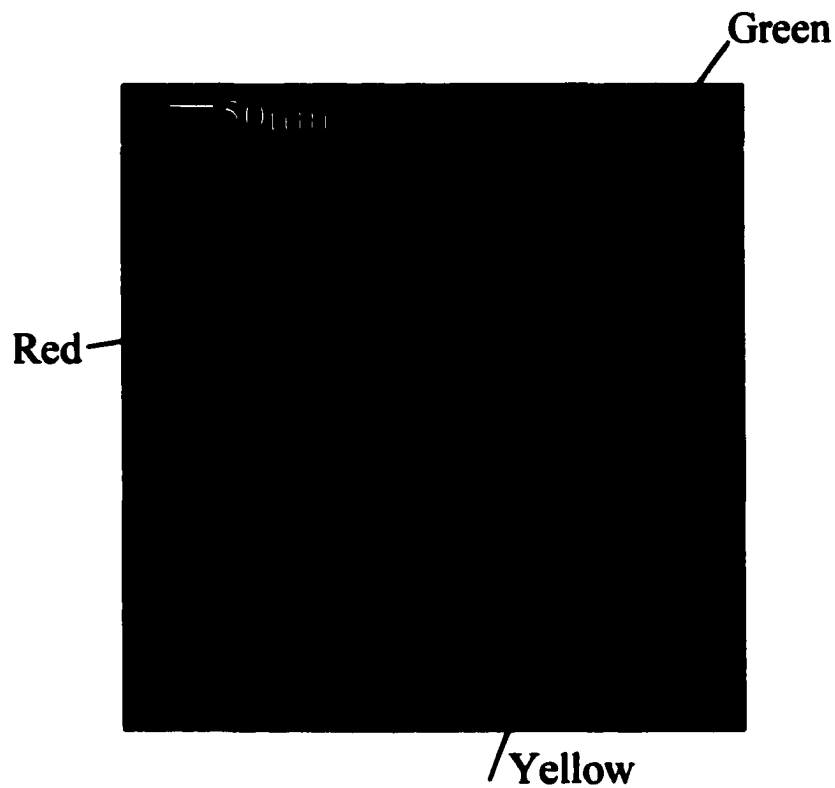


Fig. 7-19. Schematic of three integrated ZnCdSe/ZnCdMgSe QWs on a single InP substrate.



**Fig. 7-20.** PL spectra of three patterned red, yellow and green ZnCdSe/ZnCdMgSe QWs integrated on a single InP substrate.



**Fig. 7-21. Photograph of the PL emissions from square shaped red, yellow and green ZnCdSe/ZnCdMgSe QWs on a single InP substrate.**

the two barrier layers were doped, one n-type and one p-type, and a top p-type ZnSeTe contact layer were grown, the units shown in Fig. 7-21 could be fabricated into full color display elements. Compared to the conventional device fabrication using complicated post growth process, this integration is accomplished in a much simpler semiconductor epitaxial growth procedure.

### **7-6. Summary**

Growth of patterned ZnCdSe thick layers and buried QWs has been performed using shadow mask SAE. Excellent pattern definition and good optical properties were obtained. Patterned ZnCdSe/ZnSe QWs with different thickness and Cd compositions, and therefore different emission wavelengths, have been integrated on a single GaAs substrate to demonstrate the potential of this shadow mask SAE technique for device integration. We have also applied this technique to the (Zn,Cd,Mg)Se based material system and integrated green-yellow-red ZnCdSe/ZnCdMgSe QWs on a single InP substrate. Further work would be to grow (Zn,Cd,Mg)Se based LED structures with patterned ZnCdSe QW in order to integrate R-G-B LEDs on a single InP substrate and fabricate full color display elements.

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## **CHAPTER 8**

### **Influence of Shadow Mask SAE on Material Defect Density**

#### **8-1. Introduction**

An important figure of merit of the material quality is the defect density. It has been shown that in a lattice mismatched system the defect (misfit dislocation) density can be greatly reduced and the critical thickness can be increased when the growth is performed on a limited area via patterning the substrate or using oxide mask.<sup>[1-6]</sup> Since shadow mask is an alternative way to limit the growth area, it would be interesting to investigate if there is a similar defect reduction effect associated with the shadow mask SAE in the materials we have investigated.

In this chapter, I will first briefly introduce the kinds of defects observed in the crystals. The relationship between lattice mismatched epitaxy and misfit dislocation will be described and the defect reduction mechanisms with limited growth area will be discussed. The defect studies we performed on the shadow mask SAE growth of CdTe/GaAs and ZnSe/GaAs material systems will then be presented.

#### **8-2. Defects in crystals**

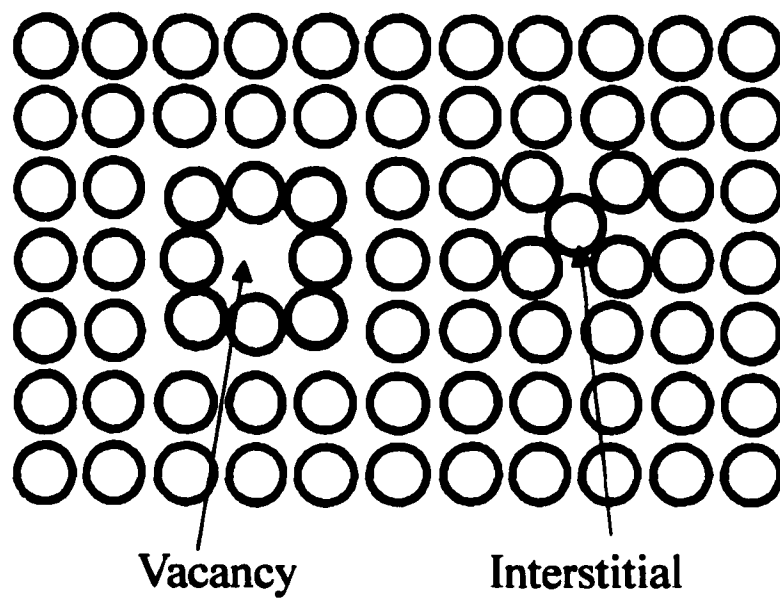
There are three types of defect in crystalline materials: point defects, stacking faults and dislocations.

### *8-2-1. Point defect*

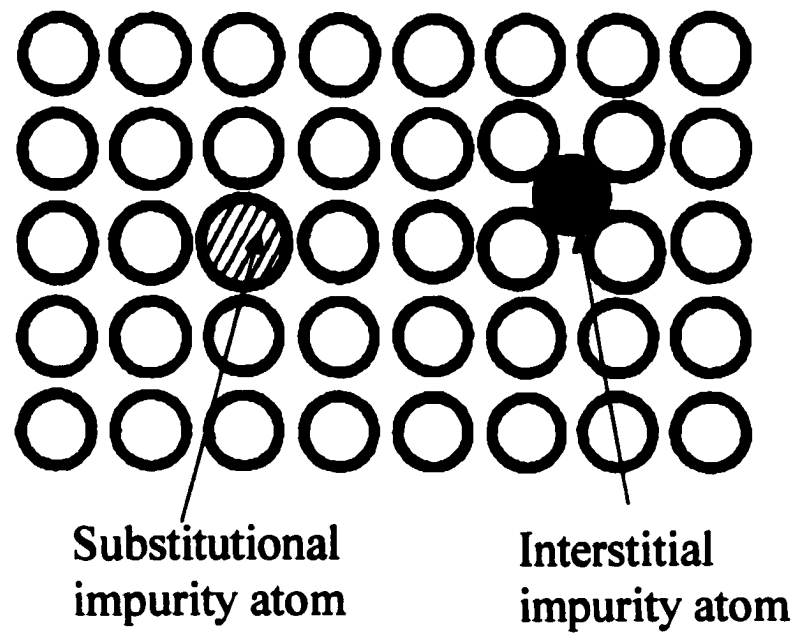
The atoms in a perfect crystal lattice are at specific atomic sites. The removal of the atom from an atomic site and the introduction of the atom into a non-atomic site cause vacancy point defect and interstitial point defect, respectively. Fig. 8-1 illustrates these two defects for a simple cubic structure. There is a considerable amount of experimental evidence suggesting that vacancies and interstitials can be produced in materials by plastic deformation and high energy particle irradiation, and that a high density of vacancies can be retained in a crystal by rapid quenching from a high temperature.<sup>[7]</sup>

Impurity atoms in a crystalline material can be considered as point defects and they play a very important role in the physical and mechanical properties of all materials. Impurity atoms can take up two different types of sites, as illustrated in Fig. 8-2, (a) substitutional, in which an atom of the parent lattice lying in a lattice site is replaced by the impurity atom, and (b) interstitial, in which the impurity atom is at a non-atomic site similar to the interstitial point defect referred to above.

All the point defects produce a local distortion in the otherwise perfect lattice. The amount of distortion and hence the amount of additional



**Fig.8-1. Illustration of the vacancy and interstitial point defects.**  
(From D. Hull, *Introduction to Dislocation*, P13, Pergamon Press, 1965)



**Fig. 8-2. Illustration of the substitutional and interstitial impurity atoms. (From D. Hull, Introduction to Dislocation, P14, Pergamon Press, 1965)**

energy in the lattice due to the defects depends on the amount of “space” between the atoms in the lattice and the “size” of the atoms introduced.

### 8-2-2. *Stacking fault*

The perfect crystal lattice can be described as a stack of identical atom layers arranged in a regular sequence. A stacking fault is a surface defect and as its name implies, it is a local region in the crystal where the regular sequence has been interrupted. Stacking faults are not expected in planes with ABABAB...sequences in body centered or face centered cubic lattices because there is no alternative site for an A layer resting on a B layer. However, for ABCABC...stacking of the close packed lattices there are two possible positions of one layer resting on another. A close-packed layer of atoms resting on an A layer can rest equally well in either a B or a C position and geometrically there is no reason for the selection of a particular positions. There are two types of stacking fault, referred to as *intrinsic* and *extrinsic*. They are best described by considering the change in sequence resulting from the removal or introduction of an extra layer. These two defects are illustrated in Fig. 8-3. In Fig. 8-3(a) part of a C layer is removed which results in a break in the stacking sequence. This is an *intrinsic* fault and it can be seen that the lattice patterns above and below the fault plane are continuous right up to the fault plane. In Fig. 8-3(b) an extra A layer has been introduced between a B

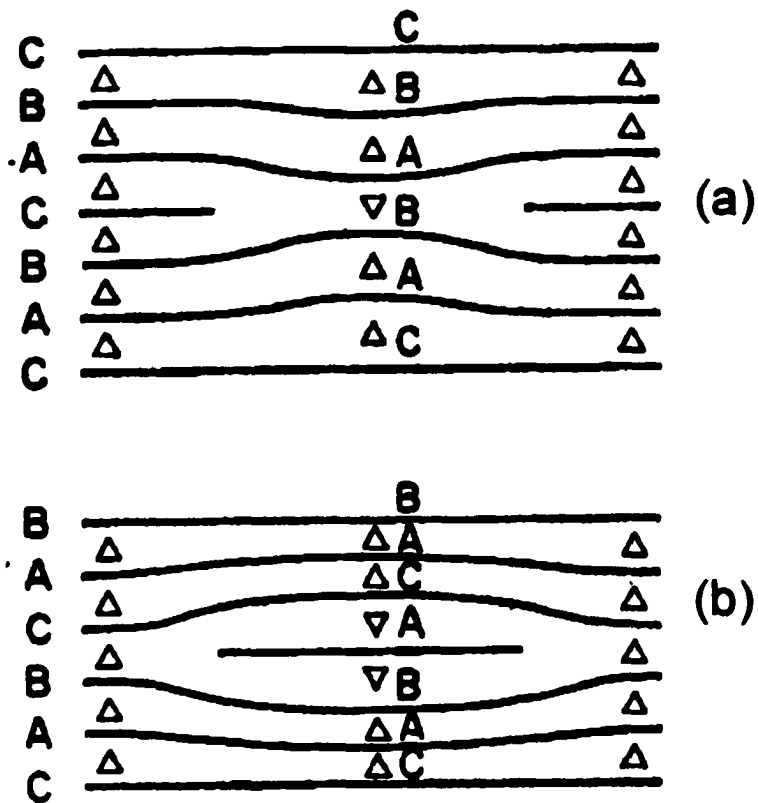


Fig. 8-3. Illustration of the intrinsic (a) and extrinsic (b) stacking faults. (From D. Hull, *Introduction to Dislocation*, P16, Pergamon Press, 1965)

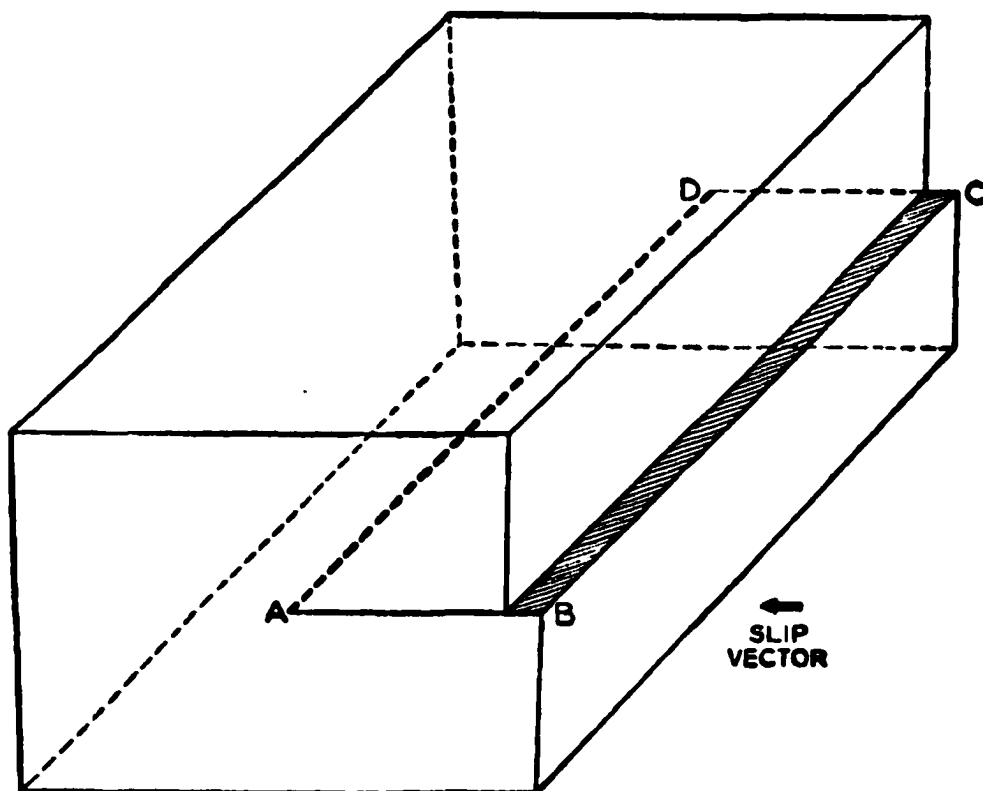
and a C layer. There are two breaks in the stacking sequence and it is referred to as an *extrinsic* fault. The extra layer does not belong to the continuing pattern of either the lattice above or below the fault.

Stacking faults have a characteristic energy per unit area called the stacking fault energy. Because of the additional lattice discontinuity associated with an *extrinsic* fault it is expected to have a higher stacking fault energy than an *intrinsic* fault.

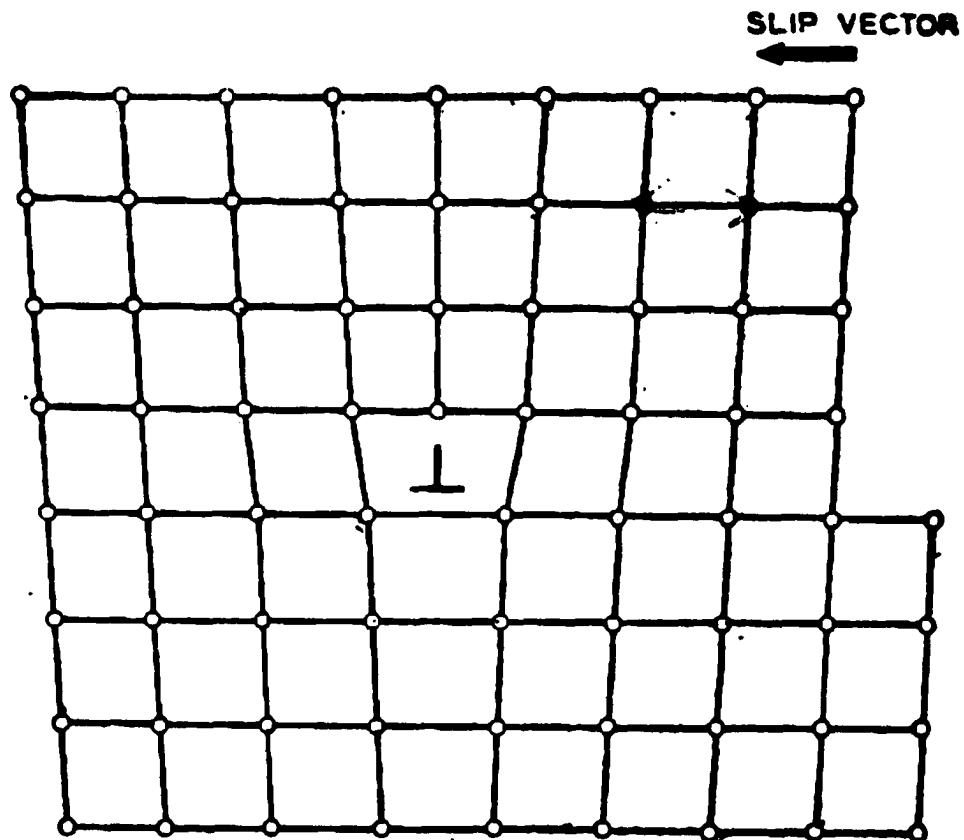
### *8-2-3. Dislocation*

Dislocations are line defects that result when part of a crystal slips relative to another part, forming the boundary within the crystal of a slipped area. The driving force behind such a slip is due to the elastic strain energy of the crystal. There are two kinds of dislocations: edge dislocation and screw dislocation.

Fig. 8-4 illustrates an edge dislocation. Such dislocation would arise, for example, if stress is applied so that the lower half of the crystal moves to the right with respect to the upper half. An entire line of atoms (along AD in the figure) then has a broken bond along the lower plane. The line imperfection AD is called a dislocation line and it is perpendicular to the slip vector. Fig. 8-5 shows a plane of atoms normal to the line of AD in Fig. 8-4, illustrating one approximation of the atomic arrangement along the



**Fig. 8-4. Illustration of an edge dislocation.**  
(From W.T. Read, *Dislocations in Crystals*,  
P2, McGraw-Hill, 1953)



**Fig. 8-5.** An approximate arrangement of the atoms in a plane normal to the AD line in Fig. 8-4.  
(From W.T. Read, *Dislocations in Crystals*, P3, McGraw-Hill, 1953)

dislocation. A crystal deforms by planes of atoms sliding over one another. There is one unit of slip on a slip plane if every atom on one side of that plane has moved into a position originally occupied by its nearest neighbor in the direction of slip. Thus unit slip leaves the atoms in registry across the slip plane and does not disturb the crystal perfection.

A screw dislocation has a dislocation line parallel to the slip vector, as shown in Fig. 8-6. Fig. 8-7 shows the arrangement of atoms around the screw dislocation, explaining why this dislocation is called screw: the crystal is not made up of parallel atomic planes one above the other, rather it is a single atomic plane in the form of helicoid, or spiral ramp.<sup>[8]</sup>

### **8-3. Dislocations and lattice mismatched epitaxy**

In a lattice matched system, the natural lattice constants of the layer being epitaxially grown (epilayer) and the substrate are the same. An example is the growth of GaAs epilayers on GaAs substrates. In a lattice mismatched system on the other hand, the natural lattice constants of the epilayer and substrate are different. If  $a$  and  $b$  are the natural lattice constants of the substrate and the epilayer, respectively, then the lattice mismatch (misfit  $\epsilon$ ) is characterized by the quantity  $\Delta a/a = (a-b)/a$ . When a lattice mismatched epilayer (also known as a strained epilayer) is grown on a substrate, the

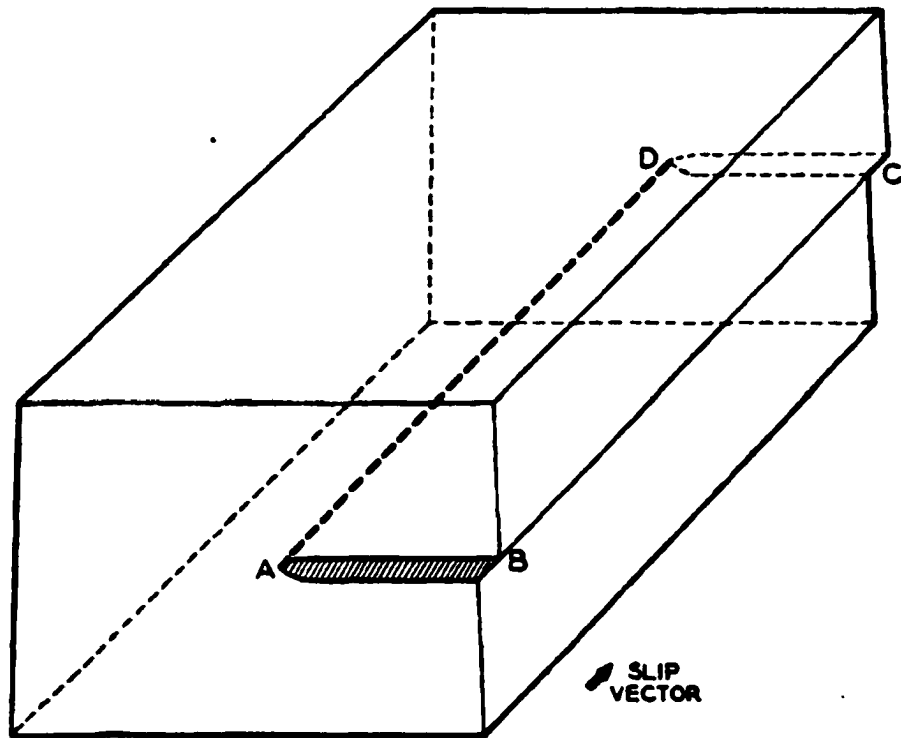
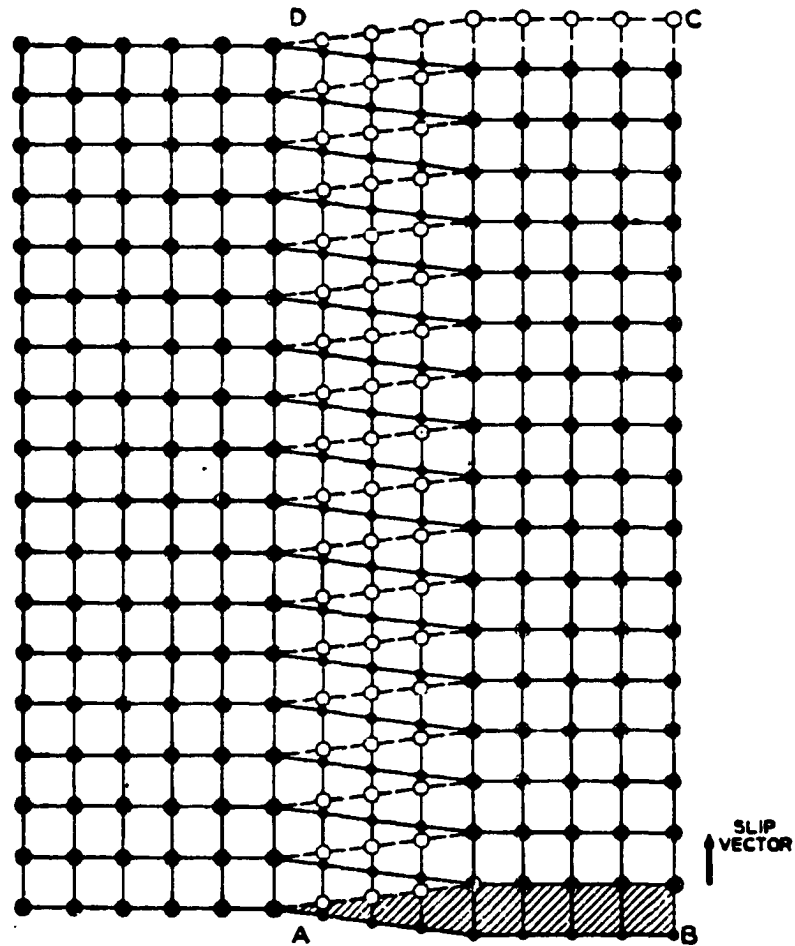


Fig. 8-6. Illustration of a screw dislocation.  
(From W.T. Read, *Dislocations in Crystals*,  
P15, McGraw-Hill, 1953)



**Fig. 8-7. Arrangement of the atoms around the screw dislocation shown in Fig. 8-6. (From W.T. Read, *Dislocations in Crystals*, P17, McGraw-Hill, 1953)**

presence of mismatch induced strain results in the formation of strain induced defects such as dislocations.

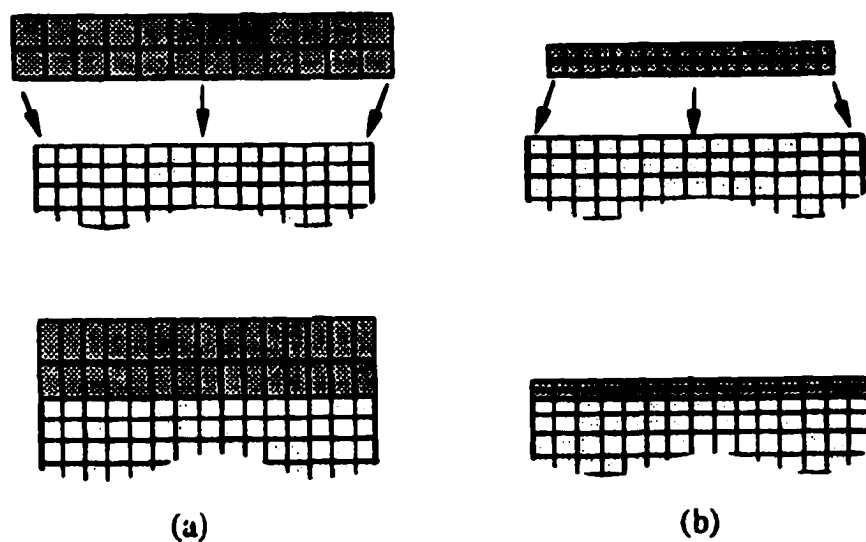
There are basic conclusions regarding the thermodynamic equilibrium state of a strained overlayer deposited on a substrate with misfit  $\epsilon(\Delta a/a)$ :<sup>[9]</sup>

1. if  $\epsilon$  is less than  $\sim 10\%$ , the first monolayer has no dislocation. If  $\epsilon$  lies between  $\sim 10\%$  and  $14\%$ , the lowest energy state of a monolayer has dislocation running along the monolayer, although the dislocations may not be generated in a metastable state. If  $\epsilon$  is greater than  $14\%$ , dislocations will be always generated in the very first monolayer and the thick overlayer may continue growth in a different orientation than the substrate.
2. For  $\epsilon < \sim 10\%$ , it is possible to divide the overlayer thickness into two regimes. When  $d < d_c$  (critical thickness), the overlayer grows in coherence with the substrate (i.e. no dislocations are produced), and  $d > d_c$  where dislocations are produced at the interface and overlayer grows with its own bulk lattice constant.

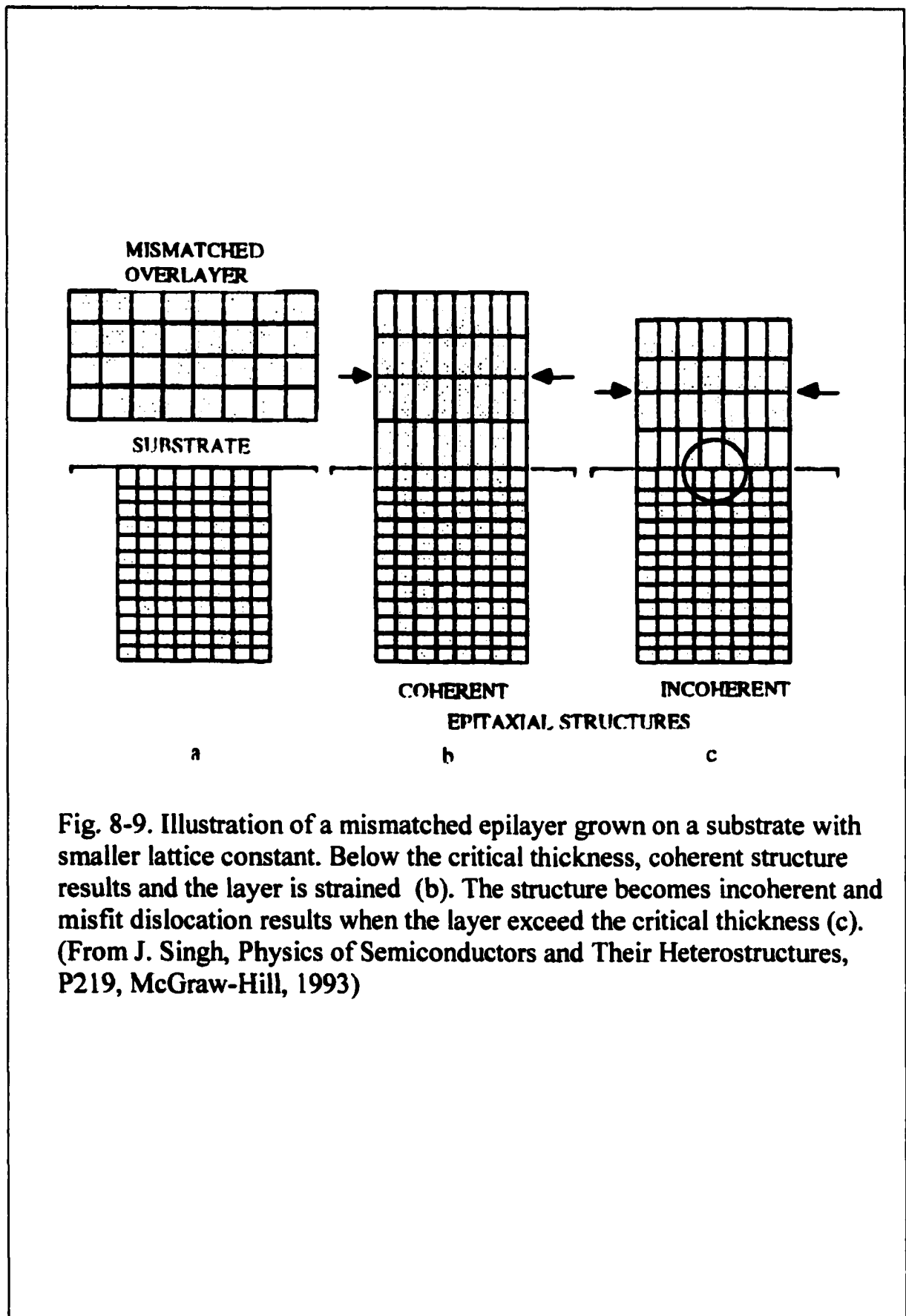
In essence, these theories show that as long as the lattice misfit is below approximately  $10\%$ , it is possible to grow an epitaxial film which is in complete registry with the substrate. However, this epitaxial layer is strained

or pseudomorphic, the lattice constant of the overgrown layer in the direction parallel to the interface is forced to be equal to the lattice constant of the substrate. Beyond the critical thickness, dislocations are produced and the strain relaxes. It is important to note that the pseudomorphic films below critical thickness are thermodynamically stable, i.e., even though they have strain energy, the relaxed state with dislocation has a higher free energy. This allows one to have large built-in strain without serious concern that the film will somehow “disintegrate” after some time. If the parallel lattice constant is forced to shrink, or a compressive strain is applied, the perpendicular lattice constant will grow. Conversely, if the parallel lattice constant of the epitaxial layer is forced to expand under tensile strain, the perpendicular lattice constant will shrink. These two cases are depicted in Fig. 8-8.

Fig. 8-9 shows how an overlayer with a lattice constant larger than the substrate grows. Below the critical thickness, a coherent structure results although the layer is strained (8-9b). If the overlayer is thick enough (over critical thickness), the incoherent structure results and the mismatch will partially be accommodated by lattice strain and partially by the introduction of misfit dislocation (8-9c). The lattice strain will be gradually released and the epilayer will eventually become fully relaxed when the film grows thicker and thicker.



**Fig. 8-8. Illustration of the strained epilayers grown on the substrate with smaller lattice constant (a) and larger lattice constant (b). In (a), the perpendicular lattice is forced to grow since the parallel lattice constant is forced to shrink. In (b), the perpendicular lattice is forced to shrink since the parallel lattice is forced to expand. (From J. Singh, *Physics of Semiconductors and Their Heterostructures*, P227, McGraw-Hill, 1993)**



**Fig. 8-9. Illustration of a mismatched epilayer grown on a substrate with smaller lattice constant. Below the critical thickness, coherent structure results and the layer is strained (b). The structure becomes incoherent and misfit dislocation results when the layer exceed the critical thickness (c). (From J. Singh, *Physics of Semiconductors and Their Heterostructures*, P219, McGraw-Hill, 1993)**

#### **8-4. Effect of growth area on misfit dislocation**

It was first proposed by Matthews and co-workers that a source of misfit dislocation (MD) generation in lattice mismatched growth is the density of threading dislocations present on the starting substrate.<sup>[10-12]</sup> Threading dislocations from the substrate and substrate surface inhomogeneities like dust particles or precipitates are examples of misfit dislocation nucleation sources which can be defined as localized defects with a fixed areal density. In small areas, if the density of sources is low enough, it is possible to have areas with few active nucleation sources and thus few misfit dislocations. Furthermore, the misfit line length generated by the fixed number of sources, and hence the amount of strain relieved, is limited by the growth area. Misfit dislocations run to the edges of the area and stop. Therefore growth on finite substrates would result in a reduction in the misfit dislocation density.

Fig. 8-10 schematically illustrates the effect of growth area on the formation of misfit dislocation based on above arguments. It shows an array of nine separated small growth areas of  $L^2$ . Four nucleation sites (stars) are randomly placed in each small area. One misfit dislocation segment is nucleated by each source and it stops at the edge without propagating into the adjacent area. The misfit segment runs in two directions away from the source, as would be expected for nucleation of a dislocation half-loop. The

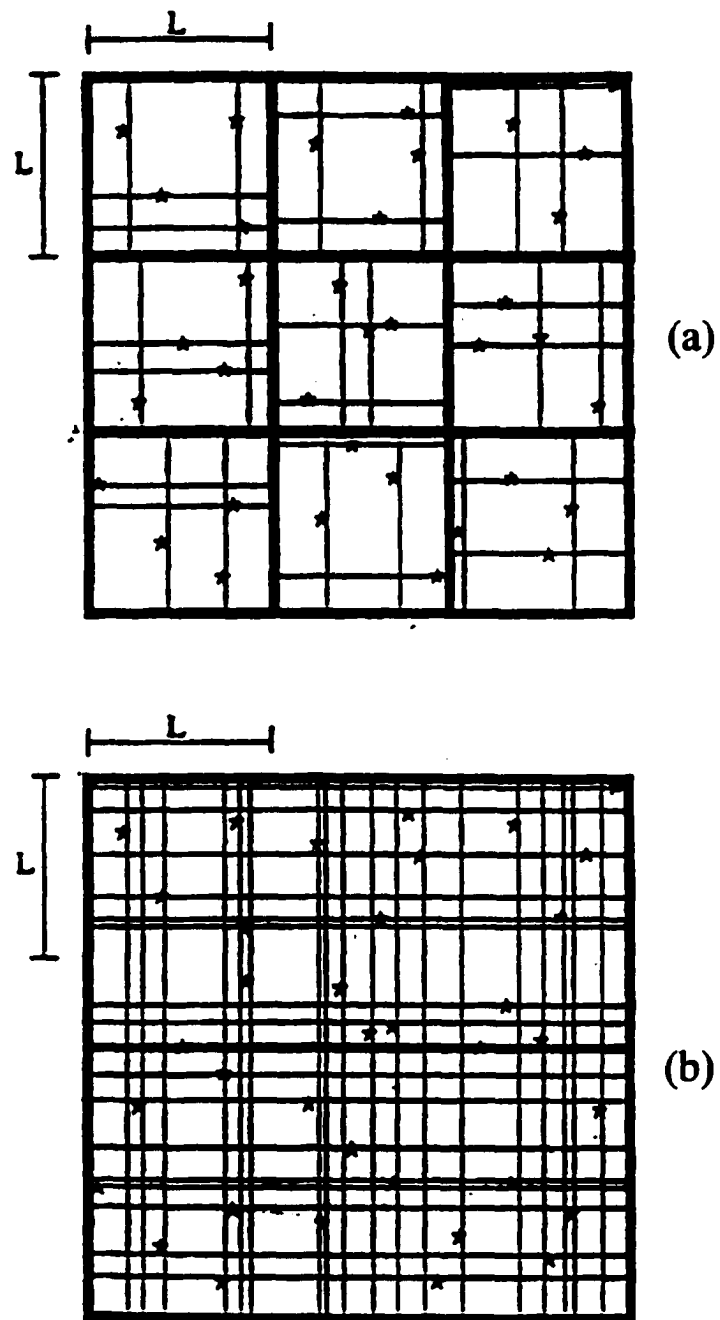
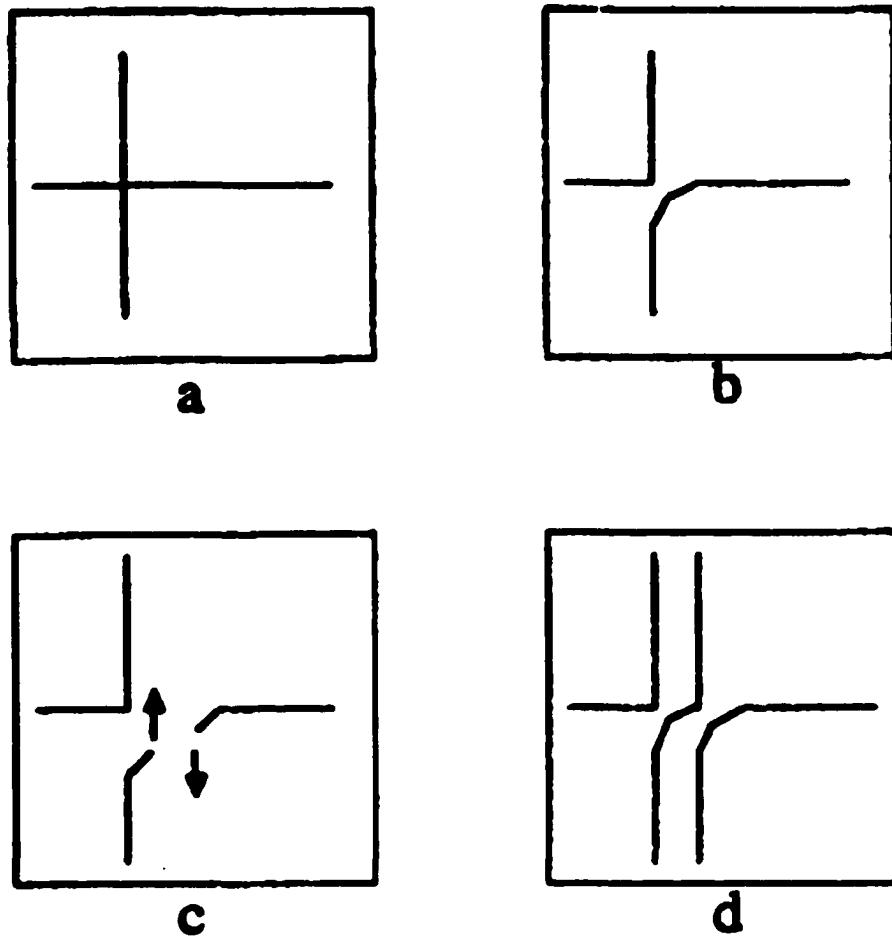


Fig. 8-10. Illustration of the growth area on the misfit dislocation density. (From Noble et al, Appl. Phys. Lett. 56(1), 51, 1990)

misfit dislocation can produce misfit segments that are three times as long if in one large area of  $9L^2$  and the linear dislocation density can be increased by a factor of 3.

Fitzgerald and co-workers observed a significant reduction in misfit dislocation densities for the growth of InGaAs on patterned GaAs (100) substrates which were finite in two directions with typical dimensions of 20-400 $\mu\text{m}$  and which were created via optical lithography.<sup>[1-3]</sup> They attributed their results to the proposition of Matthews et al. described above and to the occurrence of reduced dislocation multiplication due to a reduction in the lengths of the MDs caused by patterning. The reduction in lateral dimension reduces the interface dislocation density by decreasing the number of active nucleation sites within that area and by preventing dislocation multiplication by minimizing the distance a dislocation must travel to reach a free edge. The dislocation multiplication mechanism was first described by Hagen and Strunk.<sup>[13]</sup> It is shown schematically in Fig. 8-11. This mechanism is effective in thin films where the  $\{111\}$  segment can reach the surface, creating two new free-ended dislocations. Dislocation multiplication is expected to increase the misfit dislocation density dramatically since two new misfit dislocations are produced for every multiplication event. This mechanism is unlikely to occur for thick overlayers, since the driving force for the  $\{111\}$



**Fig. 8-11. Illustrate of the dislocation multiplication mechanism described by Hagen and Strunk. (From E.A. Fitzgerald, *J. Vac. Sci. Technol. B* 7(4), 782, 1989)**

segment to reach the specimen surface becomes low as the film thickness increases. Other multiplication mechanisms may be active besides that described by Hagen and Strunk. Dislocation multiplication can be sharply reduced when the growth area is reduced due to the escape of the dislocations at the edge of the small growth area.

As opposed to the above MD defect reduction arguments dealing with extrinsic effects, there are also intrinsic features based on intrinsic strain energy considerations and strain relief at the finite mesa edges - an effect that can be anticipated from the original work of Frank and Van der Merwe.<sup>[14]</sup> The first of these, by Luryi and Suhir, involves calculation of the stored strain energy of a perfectly crystalline lattice mismatched epilayer on a mesa finite in one lateral dimension.<sup>[15]</sup> Their findings indicate that the decreasing stored strain energy with decreasing mesa size permits growth to increasingly higher thickness without the need for MDs. In contrast to thermodynamic ground state approaches based on internal energy considerations alone, Ghaisas and Madhukar have, via computer simulations, examined the consequences of the underlying atomistic kinetic processes.<sup>[16]</sup> They have argued that the strain relief at the edges of clusters (two or three dimensional) formed as an integral part of the growth process provides a kinetic barrier for atom incorporation at cluster coalescence boundaries, thus creating a tendency for defect formation

at the very initial stage of growth. Such defects may cause subsequent misfit dislocation formation. As a result, for growth on finite substrates of dimensions comparable to or smaller than the effective migration length (which controls the average cluster size) and the dislocation strain field range, two processes become operative: (i) a propagation of the strain relief at the edges of the cluster to the mesa edge thereby giving a reduced probability for defect formation at the cluster coalescence boundaries; (ii) a reduced number of cluster coalescence boundaries if the mesa dimensions are smaller than the effective atom migration length. Both of these kinetically controlled processes would indicate a reduction in the misfit dislocation density for growth on finite substrates.

Based on above arguments on intrinsic effect that a reduction in MD should result provided the mesa size is reduced below the effective migration length of the growth controlling species and the typical range of dislocation strain fields, experimental evidence of MD density reduction in the growth of InGaAs on GaAs (100) substrates patterned with mesas elongated along one direction but having widths in the range of 0.6-1.3 $\mu\text{m}$  have been reported by Guha et. al.<sup>[4,5]</sup> A virtual absence of MDs running perpendicular to the mesa width is found.

In addition to the InGaAs/GaAs material system, the misfit dislocation density reduction in SiGe films grown by CVD on patterned Si substrate using oxide mask has been observed.<sup>[6]</sup> The suppression of dislocation accumulation in GaAs film grown on Si substrate has been reported by combination of impurity doping and selective area growth using post growth patterning.<sup>[17,18]</sup>

#### **8-5. Defect reduction investigation on shadow mask SAE growth of CdTe on GaAs(211)B substrate**

Our initial defect reduction study of shadow mask SAE was performed on the CdTe/GaAs material system. The use of GaAs and Si substrates for HgCdTe epitaxial growth is highly desirable for the manufacturing of large focal plane arrays using the hybrid approach. These HgCdTe multilayer structures make it possible to integrate signal processing and infrared detection in a monolithic structure. One of the major problems in obtaining high quality HgCdTe films on GaAs substrates is the high defect density generation that takes place because of the large lattice mismatch (14.5%) between the CdTe buffer layer and the GaAs substrate. Dislocations affect the HgCdTe infrared detector dark currents for devices operating at low temperatures because they are thought to produce mid-gap states in the bandgap. The shadow mask SAE growth of CdTe on GaAs was therefore

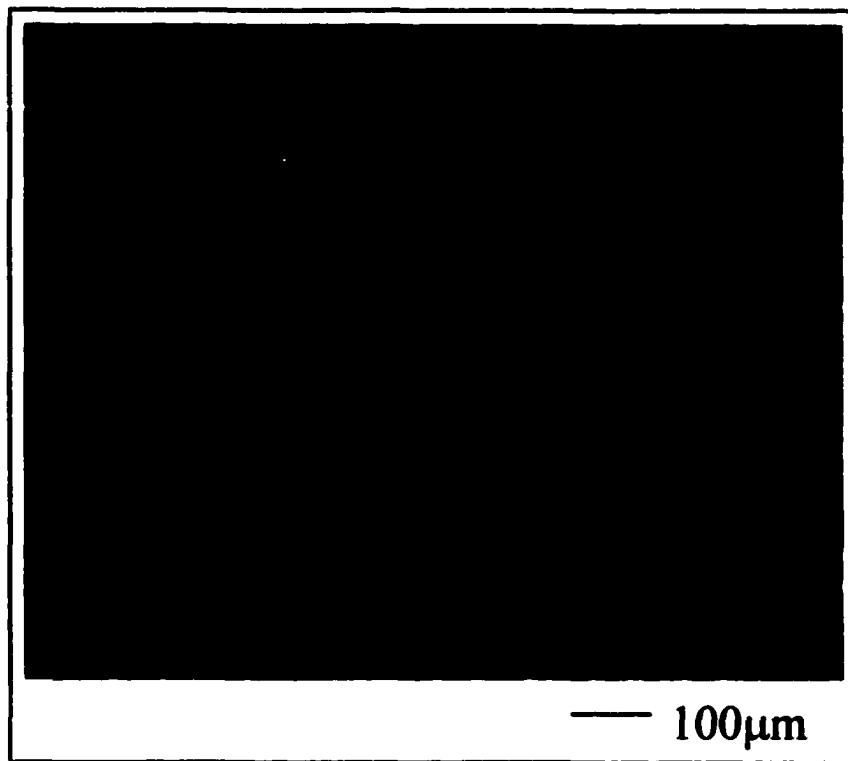
performed to investigate if there is any defect reduction effect associated with the shadow mask SAE growth and if we can improve the CdTe epilayer quality grown on GaAs substrate.

We first performed growth of flat CdTe epilayers on GaAs (211B) substrates. The (211)B orientation is chosen because the CdTe grown on this orientation has smooth surface, is free of hillocks, oval defects and antiphase domains (laminar twins) which are common growth defects present on other orientations such as (100), (111)B or (110) that degrade device performance.

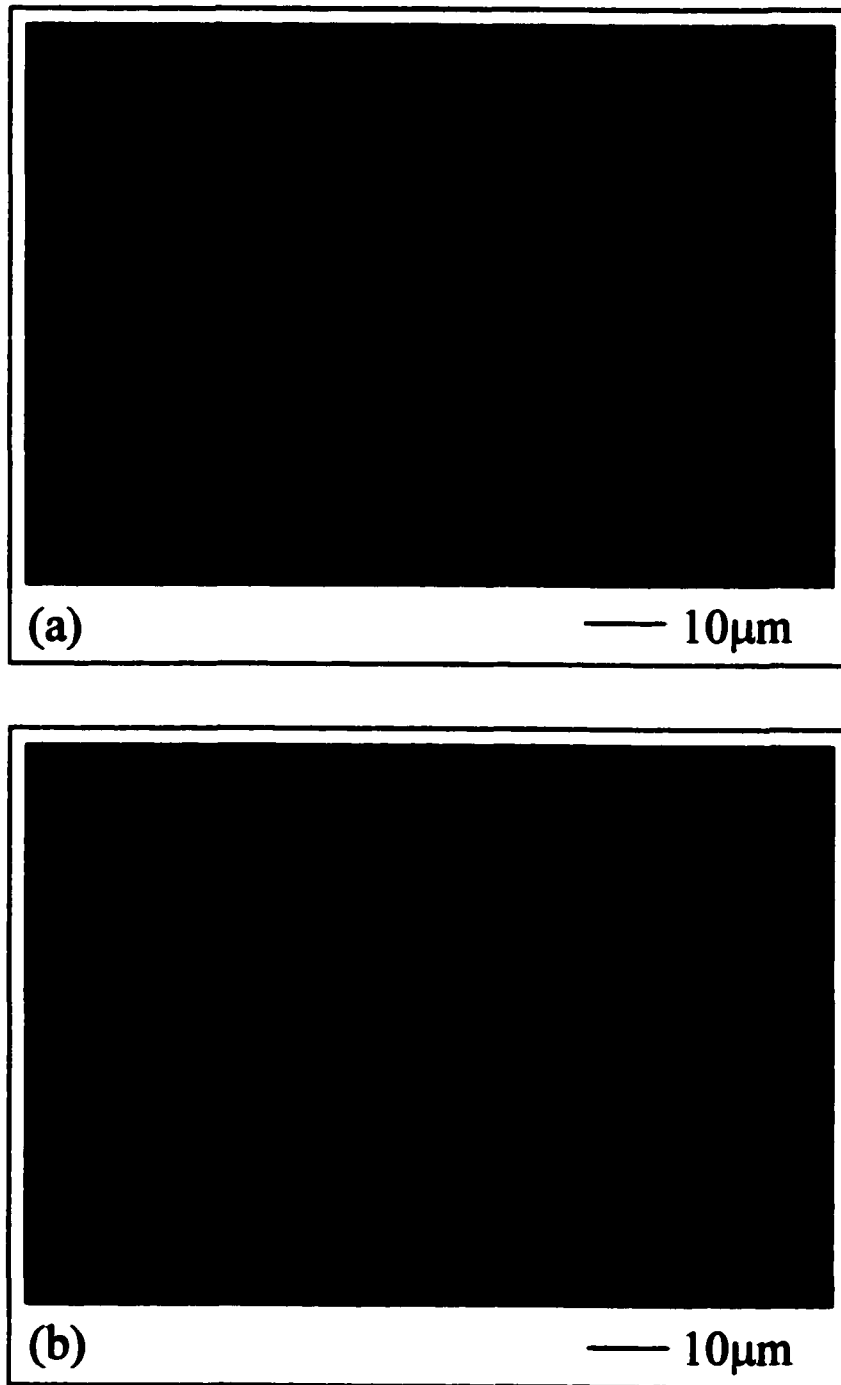
GaAs (211)B substrates were ex situ cleaned in the same way as with the GaAs(100) substrates (see chapter 2). We initially deoxidized the GaAs substrate in the III-V chamber with As impingement and grew 15 min of GaAs buffer layer ( $\sim 2000\text{\AA}$ ) before transferring the substrate into the II-VI chamber. The growth of CdTe in the II-VI chamber was performed at  $285^\circ\text{C}$  as with the growth of CdTe on CdTe and CdZnTe substrates. We found that the CdTe epilayers grown in this way were prone to twinning as observed from RHEED. The RHEED pattern was spotty and each spot actually consisted of two small spots. It was due to the excess As and the resulting surfaces were very rough. In situ thermal cleaning was therefore carried out in the II-VI growth chamber directly by heating the substrates to  $560\text{-}580^\circ\text{C}$  without As passivation. After that, the substrates were cooled down to  $285^\circ\text{C}$

for the growth of CdTe. The surface morphology was still very rough (Fig. 8-12) for the first few growth runs although we no longer observed twinning in the RHEED pattern. It was difficult to make etch pit defect density measurement due to the roughness of the surface. After we increased the growth rate from  $\sim 1\mu\text{m/hr}$  to  $\sim 1.5\text{-}2\mu\text{m/hr}$  through increasing the CdTe cell temperature, better surface morphology was obtained. We managed to make defect density measurement using chemical etching as described in chapter 4. Fig. 8-13(a) shows a CdTe epilayer surface before etching and Fig. 8-13(b) shows the surface after etching with EPD in the  $2 \times 10^7/\text{cm}^2$  range. The CdTe epilayer quality was still a little worse than that reported by other research groups without any post growth defect reduction treatments such as thermal annealing<sup>[19]</sup>. To further improve the surface morphology and material quality, we tried CdTe growth using Te passivation after the GaAs substrate oxide desorption.<sup>[20]</sup> The surface morphology was improved but the defect density is still in the  $10^7/\text{cm}^2$  range (Fig. 8-14).

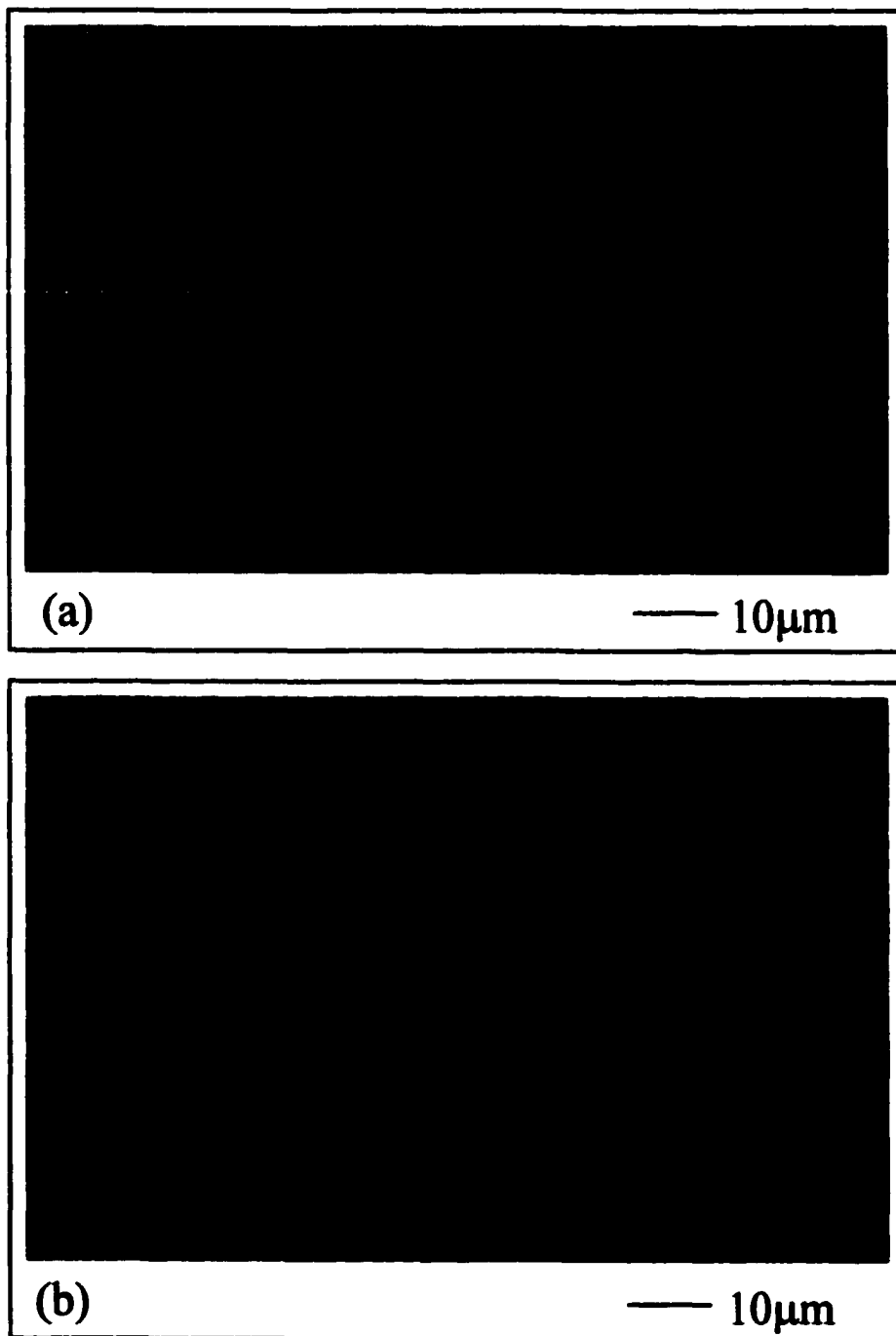
The patterned growth of CdTe on GaAs has been carried out once, before we optimized the flat layer growth. The surface of the CdTe mesas is very rough and therefore no defect reduction effect can be measured (Fig. 8-15).



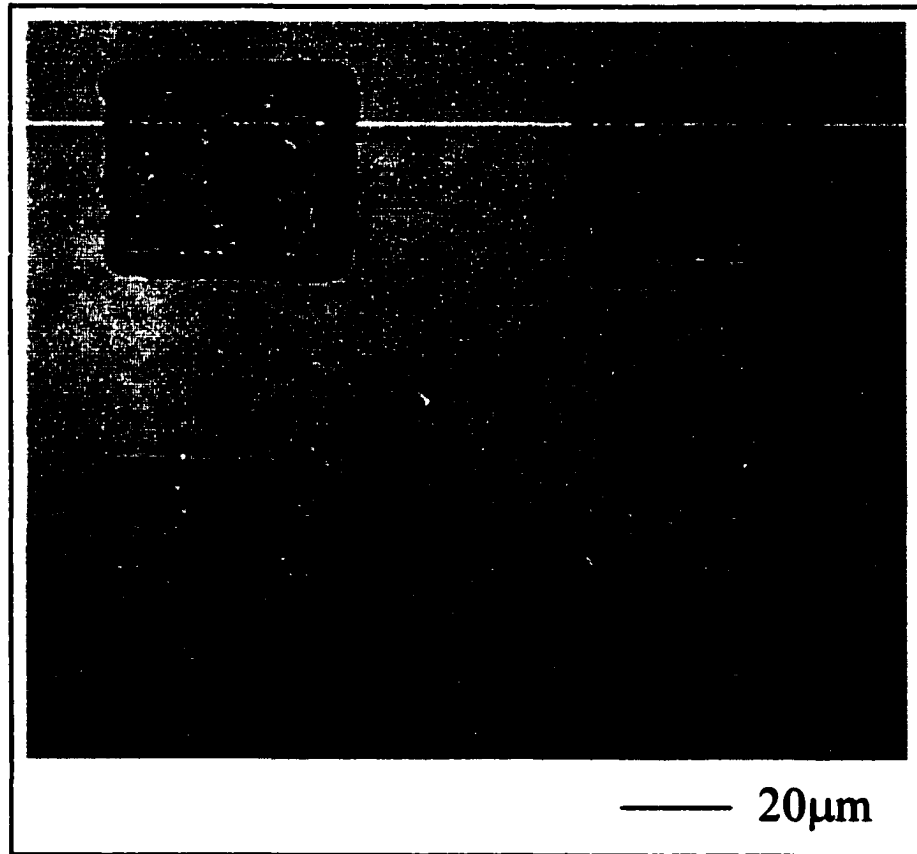
**Fig. 8-12. Rough surface morphology of the CdTe epilayer.**



**Fig. 8-13. Nomarski micrographs of the CdTe epilayers before etching (a) and after etching (b).**



**Fig. 8-14. Nomarski micrographs of CdTe epilayers grown with Te passivation: (a) before etching and (b) after etching,  $EPD \approx 3 \times 10^7 \text{ cm}^{-2}$**



**Fig. 8-15. Nomarski micrograph of the patterned CdTe exhibiting rough surface.**

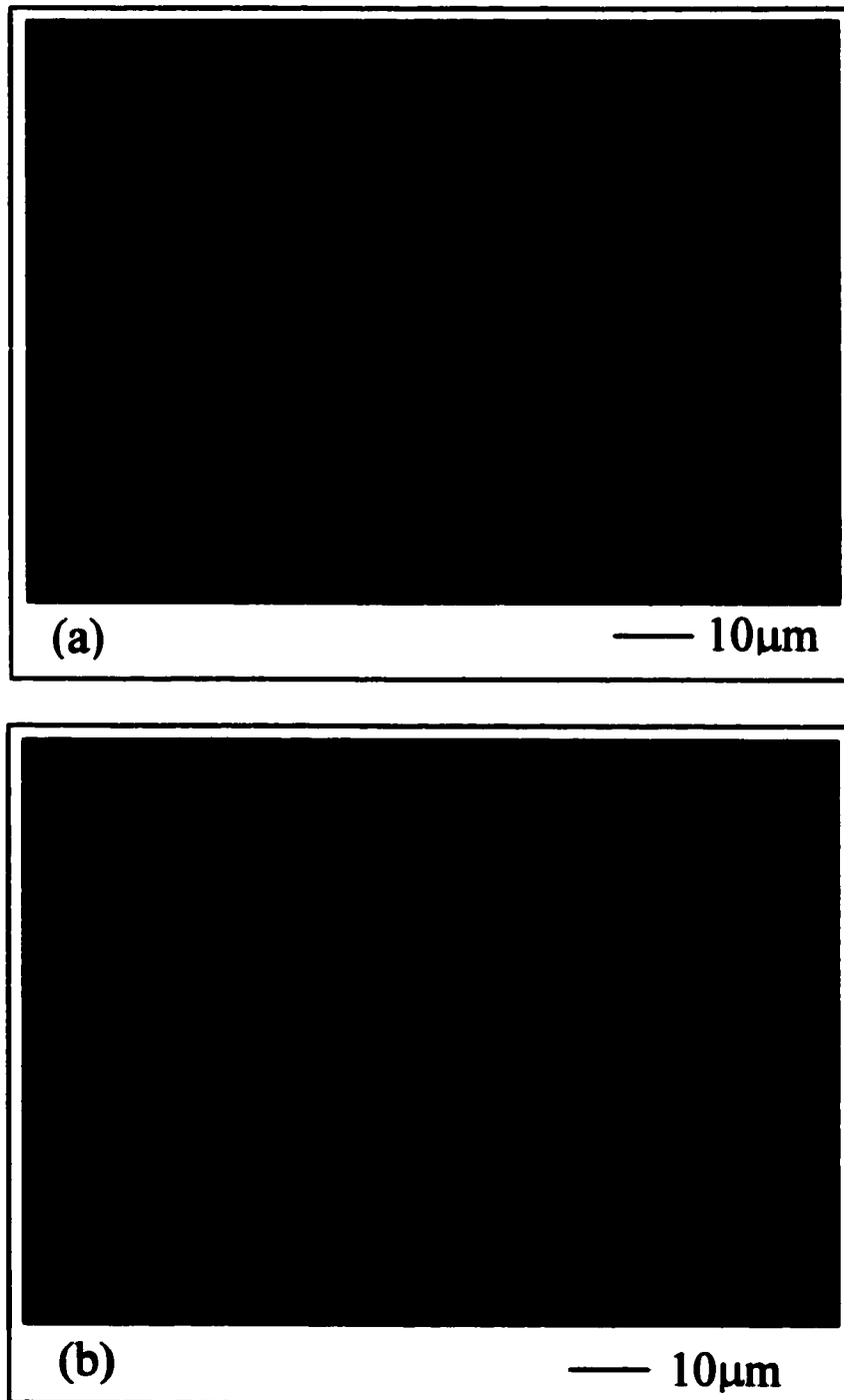
The difficulty in growing high quality CdTe epilayer on GaAs substrate lead us to realize that this material system is not ideal for the defect reduction study. The large lattice mismatch between CdTe and GaAs causes initial three-dimensional (3D) growth which results in rough epilayer surface and it is hard to make defect density measurement using chemical etching. Other than that, this 3D growth mode is not favorable for the defect reduction study according to the island coalescence theory based on the intrinsic effect of the dislocation generation mechanisms. Therefore we gave up this material system for the defect reduction study with shadow mask SAE.

#### **8-6. Defect reduction investigation on shadow mask SAE growth of ZnSe on GaAs(100) substrate**

In recent years, the ZnSe/GaAs based heterojunctions have been of great interest due to their potential optoelectronic applications in the blue-green lasers and LEDs.<sup>[21,22]</sup> One of the directions in this research is to reduce the as-grown defects. These defects act as non-radiative recombination centers during device performance and are responsible for the laser and LED device failure.<sup>[23-25]</sup> It would be interesting to look into the defect density of patterned ZnSe using shadow mask SAE growth to investigate the presence of defect reduction effect with the shadow mask SAE and to improve the ZnSe material quality as well. However, there are a few issues associated

with this material system. First of all, stacking fault is a major defect in the ZnSe epilayer grown on the GaAs substrate. The effect of limited area on this type of defect is not known. Furthermore, stacking fault interplays with the misfit dislocation.<sup>[26-31]</sup> Secondly, the lattice mismatch between ZnSe and GaAs is relatively low, only 0.27%, which results in low misfit dislocations density. This makes its defect reduction study more difficult. However, the high technical impact of the defect reduction in this material system lead us to perform a series of studies using shadow mask SAE.

Growth of flat ZnSe epilayers on GaAs substrates was carried out prior to the shadow mask SAE growth. The growth of ZnSe was performed following the procedure described in chapter 2 and the growth time varied from 15 minutes to 2 hour. The defect density of ZnSe epilayers was measured by chemical etching using Br<sub>2</sub>/Methanol etchant as described in chapter 4. The EPD of our flat ZnSe epilayers vary from low 10<sup>6</sup> to mid 10<sup>7</sup>/cm<sup>2</sup>. The thick layers have relatively higher defect density than the thin layers due to the gradual strain relaxation along with the increase in the layer thickness which result in dislocation generation. Fig. 8-16 shows a micrograph of a thin ZnSe epilayer (~4000Å) having a defect density at low 10<sup>6</sup>/cm<sup>2</sup> and a thick ZnSe epilayer (~8000Å) having a defect density at high 10<sup>6</sup>/cm<sup>2</sup>. By performing Zn-Be co-irradiation<sup>[34]</sup> on the GaAs buffer layer

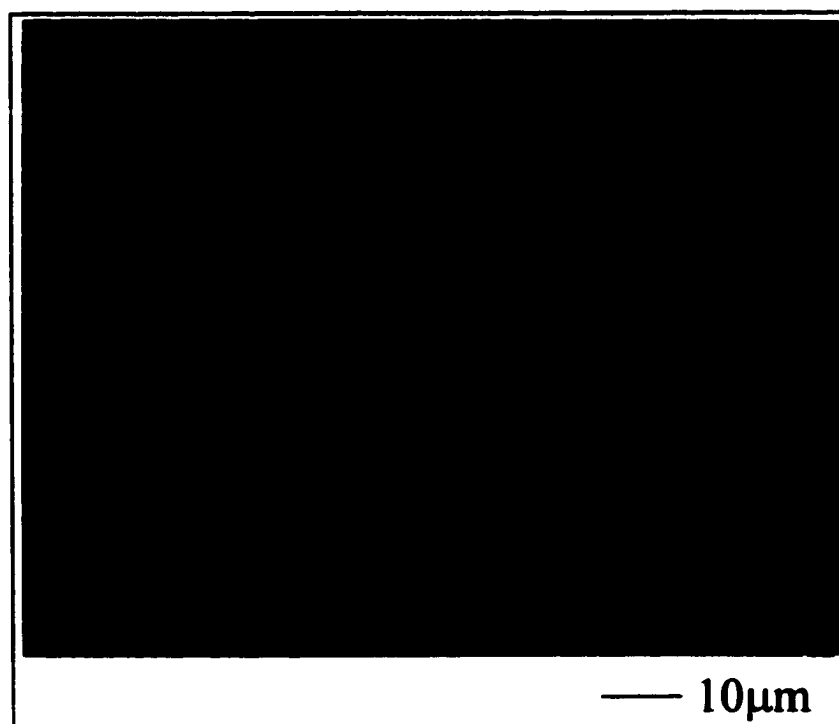


**Fig. 8-16. Nomarski micrographs of the ZnSe thin epilayer with EPD at  $3-4 \times 10^6/\text{cm}^2$  (a) and thick ZnSe epilayer with EPD at  $8-9 \times 10^6/\text{cm}^2$  (b).**

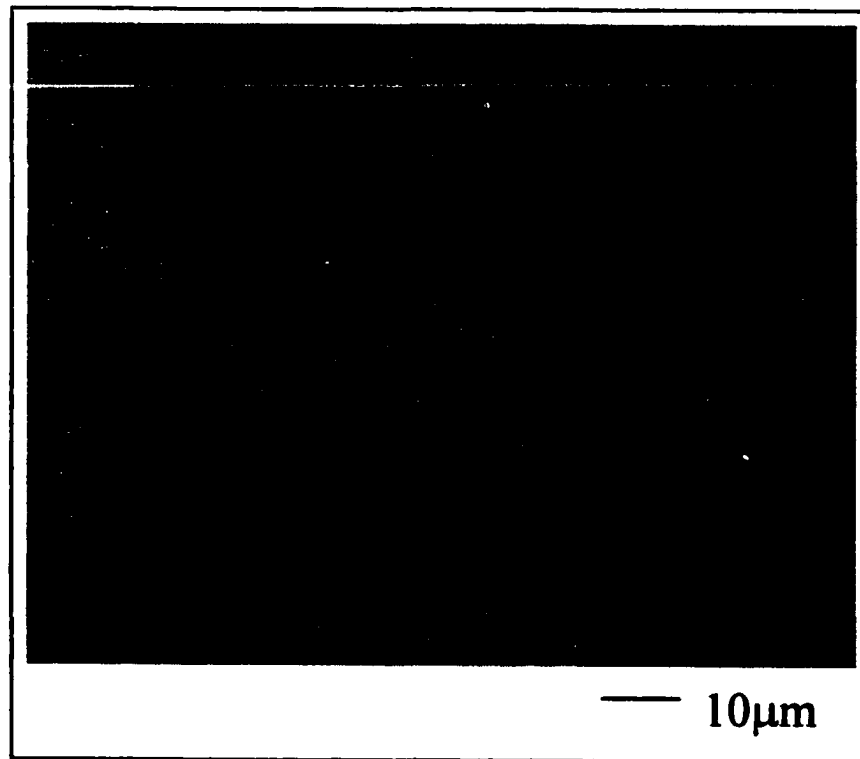
before the growth of the ZnSe epilayer, we were able to reduce the defect density down to mid  $10^5 \text{ cm}^{-2}$  in the ZnSe epilayer of  $\sim 7000\text{\AA}$  thick (Fig. 8-17). The Zn-Be co-irradiation was performed by exposing the GaAs buffer layer to the Zn and Be flux at  $170^\circ\text{C}$  for 20 sec. After that, the substrate temperature was raised to  $250^\circ\text{C}$  and the growth of ZnSe was carried out.

Patterned ZnSe growth was initially performed by using the *in situ* mask fixture with metal mask. After the substrates were deoxidized and the buffer layers were grown in the III-V chamber, the substrates were transferred into the II-VI chamber. The in situ mask holder was then placed on the substrates and the growths were performed in the same manner as the flat layer. The patterned ZnSe epilayers ( $\sim 6000\text{\AA}$ ) grown without Zn-Be co-irradiation in the early samples exhibit EPD in the mid  $10^6 \text{ cm}^{-2}$ , which is comparable to that of flat ZnSe epilayer. Fig. 8-18 shows a micrograph of the patterned ZnSe epilayer after chemical etching.

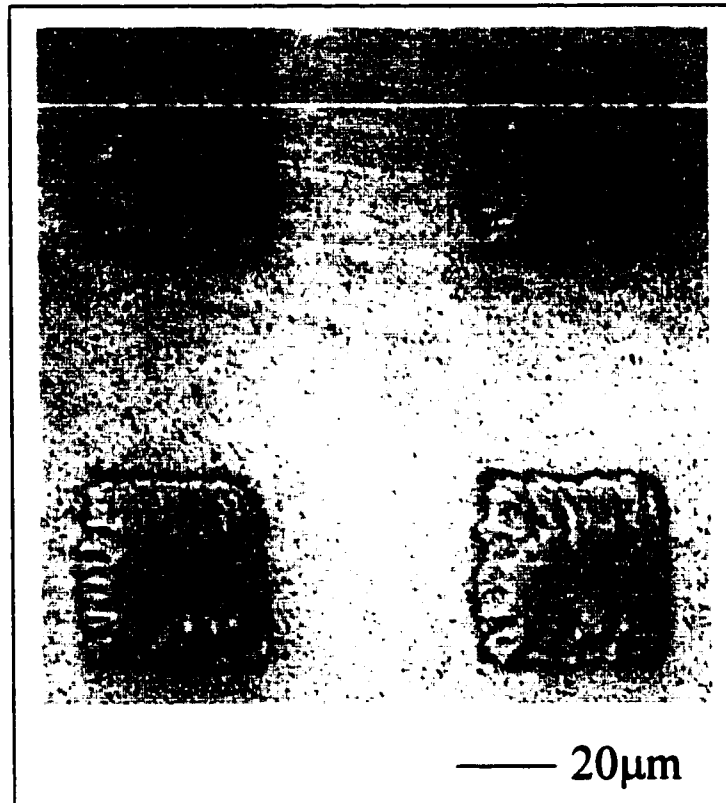
One problem we identified with the patterned ZnSe growth was that the metal mask can be easily coated by the ZnSe material which eventually blocks the openings in the mask. The patterned ZnSe layer grown with the used metal mask (only once or twice) exhibits very poor pattern definition (Fig. 8-19). Therefore a silicon mask was fabricated and used for the SAE growth of ZnSe. We observed much less coating of the ZnSe material on the



**Fig. 8-17. Nomarski micrograph of the ZnSe epilayer grown with Zn-Be co-irradiation, exhibiting EPD in the range of  $4-5 \times 10^5 \text{ cm}^{-2}$ .**



**Fig. 8-18. Nomarski micrograph of the patterned ZnSe epilayer exhibiting EPD at  $\sim 4\text{-}6 \times 10^6 \text{ cm}^{-2}$ .**

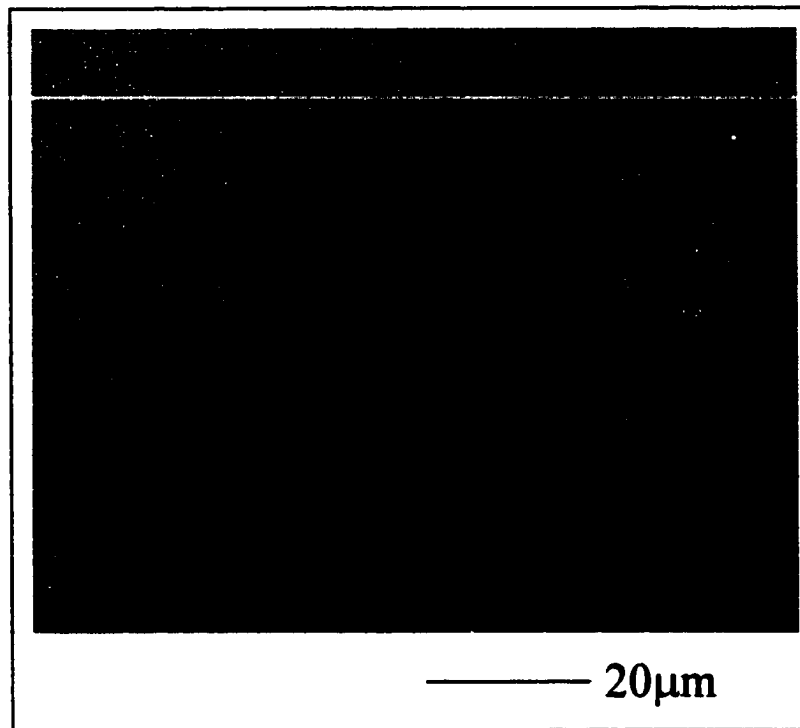


**Fig. 8-19. Poor pattern definition of ZnSe square arrays grown with used metal mask.**

silicon mask. The Si shadow masks can be used for more growth runs and they can be easily cleaned by using  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:8:10) etchant. Similar defect density was observed in the patterned ZnSe layer grown with Si mask as with the metal mask.

Further studies were performed by the SAE growth of patterned ZnSe layers with Si mask and Zn-Be co-irradiation. We initially performed the Zn-Be co-irradiation with the mask attached on the GaAs substrate. We observed defect density in the mid  $10^6 \text{ cm}^{-2}$  in the thin ZnSe layers, which is higher than the corresponding flat ZnSe layer. Since the Be cell is placed in the outer port of the MBE source flange, we suspected that the shadow mask may have blocked the arrival of the oblique Be flux and therefore the influence of Zn-Be co-irradiation on ZnSe defect density was diminished. Subsequent growth was performed by placing the mask on the substrate after Zn-Be co-irradiation. We obtained even higher ZnSe EPD (Fig. 8-20) which suggests that the interruption for the placement of the mask after Zn-Be co-irradiation is not favorable for the SAE growth of ZnSe layers and the Zn-Be co-irradiation process was discarded for the later studies.

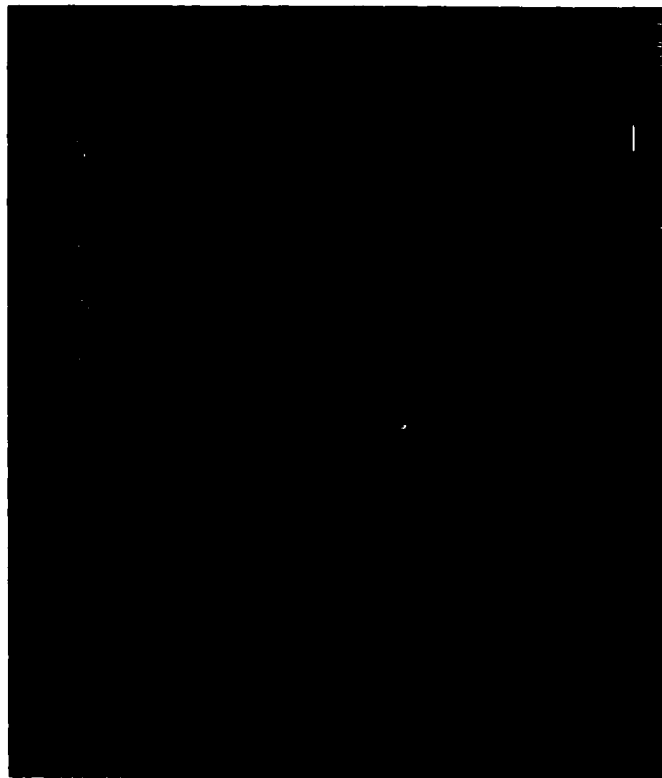
Since both stacking fault and misfit dislocation exist in the ZnSe epilayer, it would be necessary to separate them and look for defect reduction effects on each of them individually. This is a simplification since the two



**Fig. 8-20. Nomarski micrograph of a 50µm ZnSe square having EPD at low  $10^7/\text{cm}^2$ .**

defects interplay with each other. Nevertheless, we used SEM to attempt to specify the shapes of the etch pits since there are three types of etch pits in the etched ZnSe epilayer corresponding to defects of different origins (chapter 4).<sup>[32,33]</sup>

Fig. 8-21 shows a SEM micrograph of a 20 $\mu$ m ZnSe square grown with silicon shadow mask after chemical etching. Two types of etch pits are seen, one is singular and one is doublet which corresponds to the type II pits in the literature. The type I and type III singular pits mentioned in the literature are not quite distinguishable in our case. Therefore for simplicity we assigned the singular type etch pits to both type I and type III and they are related to misfit dislocations while type II doublet pits are related to stacking faults. The interactions between stacking fault and misfit dislocation are neglected. A sample grown with the silicon shadow mask was studied in detail by this technique. The defect density at the different regions of the ZnSe squares and stripes were collected and evaluated statistically. Table 8-1 summarizes the result of this study. Each average was based on 7-9 measurements. From this summary, we can see that there is no obvious reduction of either misfit dislocation or stacking faults in the patterned epilayer and the average defect density of the patterned epilayer is comparable to that of flat epilayer.



**Fig. 8-21. SEM micrograph of the ZnSe epilayer after chemical etching. Two types of etch pits are seen, one is singular and one is doublet.**

<b>Stripe size (<math>\mu\text{m}</math>)</b>	<b>Average EPD of type II pits (<math>10^6/\text{cm}^2</math>)</b>	<b>Average EPD of type I+III pits (<math>10^6/\text{cm}^2</math>)</b>	<b>II/(I+III)</b>	<b>Total EPD (<math>10^6/\text{cm}^2</math>)</b>
<b>20</b>	<b>2.4</b>	<b>1.6</b>	<b>1.5</b>	<b>4</b>
<b>30</b>	<b>3.2</b>	<b>1.7</b>	<b>1.9</b>	<b>4.9</b>
<b>40</b>	<b>2.3</b>	<b>0.6</b>	<b>3.8</b>	<b>2.9</b>
<b>50</b>	<b>3.0</b>	<b>2.0</b>	<b>1.5</b>	<b>5.0</b>
<b>60</b>	<b>2.5</b>	<b>1.9</b>	<b>1.3</b>	<b>4.4</b>
<b>flat</b>	<b>1.9</b>	<b>1.3</b>	<b>1.5</b>	<b>3.2</b>

**Table 8-1. Summary of the EPD studies of the ZnSe stripes and flat layer grown with Si mask.**

We conclude that due to the small lattice mismatch between ZnSe and GaAs which gives rise to a small MD density, and due to the presence of a high density of stacking faults whose behavior under limited area growth area is not known, the ZnSe/GaAs material system is not ideal for initial defect reduction study with shadow mask SAE. Furthermore, EPD measurement although convenient, is perhaps not sophisticated and qualitative enough for detecting defect origins and defect densities. Nevertheless, our studies indicate that the patterned ZnSe epilayer have similar defect density as that of flat epilayer suggesting that the growth with shadow mask does not degrade the material quality. Our studies also established a mechanism for performing this type of important study using either the simple EPD method or more sophisticated tools such as Transmission Electron Microscopy (TEM) or Cathodoluminescence (CL) if the appropriate material system was selected.

### **8-7. Summary**

Due to the simple characterization technique we employed and to the non-ideal material system we studied, we are unable to identify if there is any defect reduction effect associated with the shadow mask SAE. However, our studies indicates that the materials grown with shadow mask SAE have at least comparable defect density as that of the flat epilayer grown under the similar conditions. Our studies also established a mechanism for the defect

reduction investigation with shadow mask SAE. Further studies can be performed by using TEM to really look into the origin, propagation and interaction of defects in the ZnSe/GaAs material system or by pursuing other material systems that may be well suited for the defect reduction study. Such a material system may be the lattice mismatched ZnCdSe/ZnCdMgSe QW needed for the red light emission in the (Zn,Cd,Mg)Se based LEDs which will be mentioned as a direction for future work in chapter 10.

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## CHAPTER 9

### Enhancements of the *in situ* Mask Fixture

#### 9-1. Introduction

As described in previous chapters, the *in situ* mask fixture we designed presents some limitations. For example, we experienced difficulty in placing the mask over the substrate if the posts and holes in the mask fixture assembly were not reasonably well aligned. This is because the mask and support ring may move relative to each other during transfer, which results in the misalignment of the holes in these two pieces. The posts will eventually fail to go through these holes and will push out the mask and support ring away from the substrate instead. Another more fundamental problem is related to the registration of the masks in successive SAE steps for growth of different patterned epilayers in multiple step SAE. A better mask alignment mechanism is needed to improve the registration of multiple layers grown by sequential shadow mask SAE, as needed for most device structure fabrications.

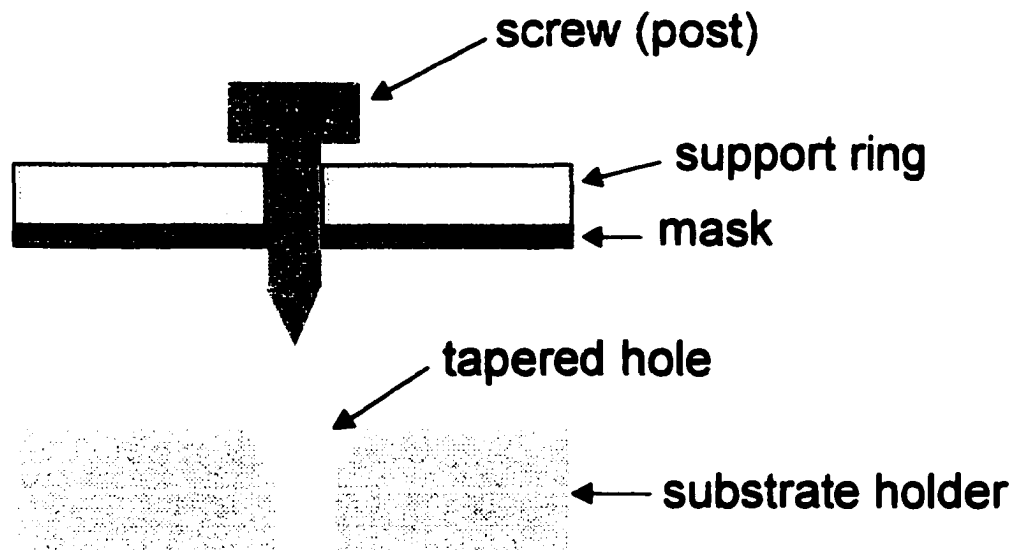
In this chapter, some of our attempts to solve the aforementioned two design problems will be introduced. Two kinds of modifications were proposed and implemented to improve the performance of the *in situ* mask

fixture. One approach was to use three posts (rather than two) attached to the mask and support ring assembly and use three holes in the substrate holder. Another approach involves the use of grooves and knife edges which gives better mask registration mechanism.

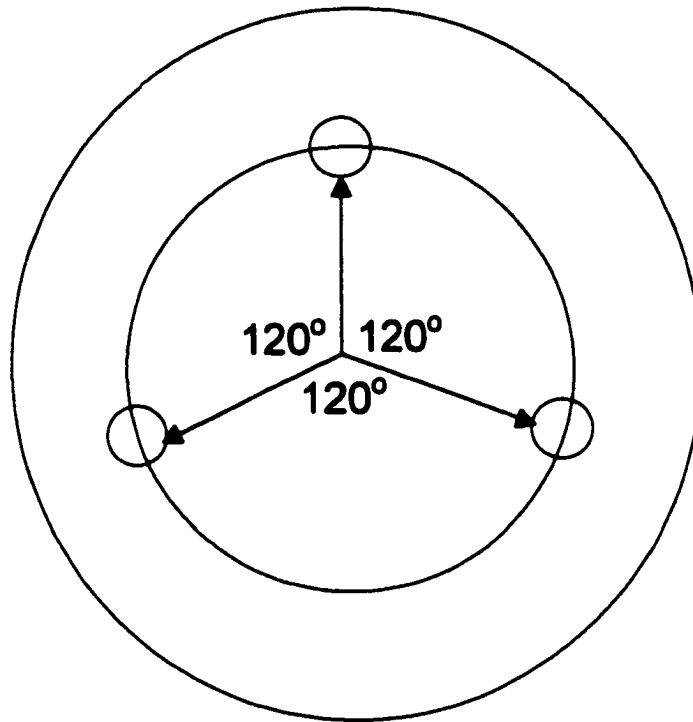
### **9-2. Modification using three posts and holes**

Since three points can define position better than two, it would be reasonable to consider that the use of three posts and holes in the *in situ* mask fixture would result in better alignment for multiple step SAE. To avoid the relative movement between the mask and support ring during transfer, it is also preferred to fix these two pieces together. Therefore, we proposed to use three posts attached to the mask and support ring assembly and three holes in the substrate holder to improve the performance of the *in situ* mask fixture.

In the real *in situ* mask fixture fabrication, we used screws to fix mask and support ring. This solves the first problem of the *in situ* mask fixture described in the introduction. The screws act as the posts as well. The ends of these screws were pointed so that they can easily slide into the holes. The top of the holes in the substrate holder was also tapered to provide more clearance for the posts to fit into the holes. Fig. 9-1 illustrates above modifications. The posts and holes are 120° apart in the same circle as shown in Fig. 9-2.



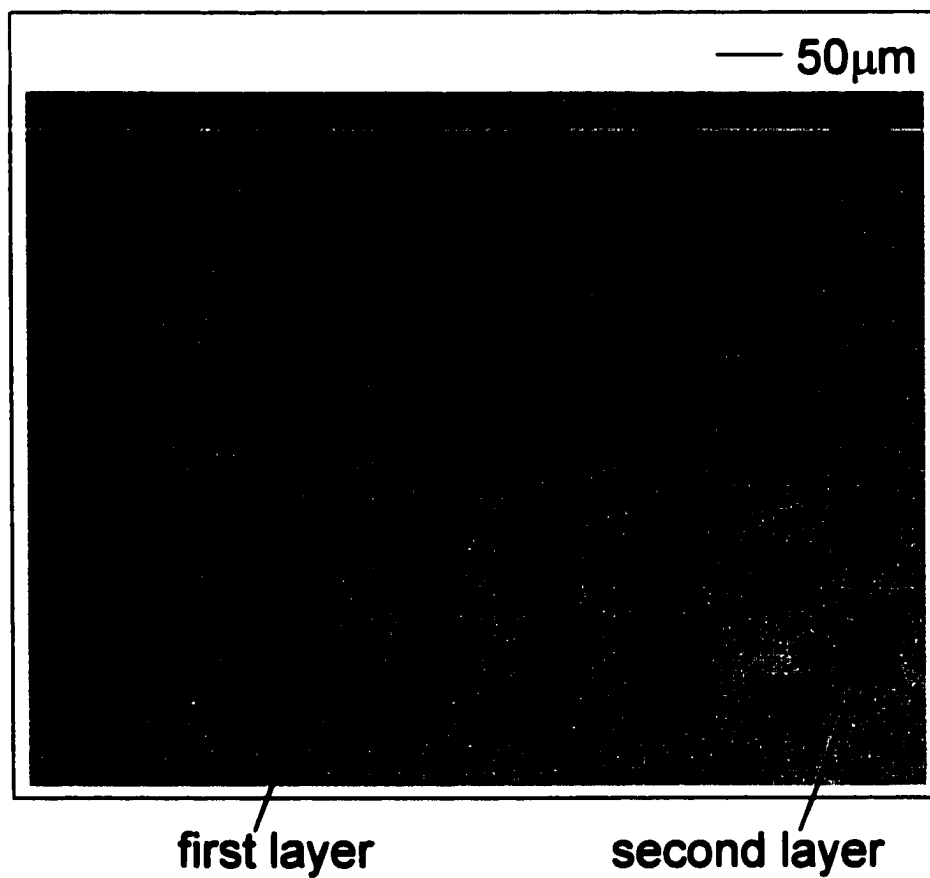
**Fig. 9-1. Illustrate of the modifications using screw to attach the mask and support ring. The screw also act as post to fit into the tapered hole in the substrate holder.**



**Fig. 9-2. Illustration of the distribution of the three posts and holes. They are 120° apart in a same circle.**

We used this design and tested its performance by growing two patterned CdTe epilayers sequentially. After the growth of the first patterned CdTe epilayer using the *in situ* mask fixture, we simply removed the mask holder and then placed it back to grow another patterned epilayer. The placement of the mask on the substrate is much easier in this new design since one can see the relative position of both the holes and posts from the viewing port outside the MBE chamber.

In spite of using three posts, we still observed a slight shift between the two sequentially grown epilayers with this new design. Fig. 9-3 shows the micrograph of two CdTe layers grown in this way. The two CdTe layers are shifted from each other by approximately 50 $\mu\text{m}$  in one direction and 80 $\mu\text{m}$  in the other. There are two possible reasons to account for this misalignment. One is due to the movement of the mask relative to the posts. The mask can not be fixed in place by the screws since it is very thin. Welding the posts to the mask and support ring would be a better approach. The other reason may be that the holes in the substrate holder are actually slightly bigger than the posts since some clearance is needed for the posts to successfully fit into the holes. A slight movement in the positioning of the mask (even though in the micron range) becomes significant in the resulting grown layers as the size and separation of the semiconductor structures are in the range of microns.

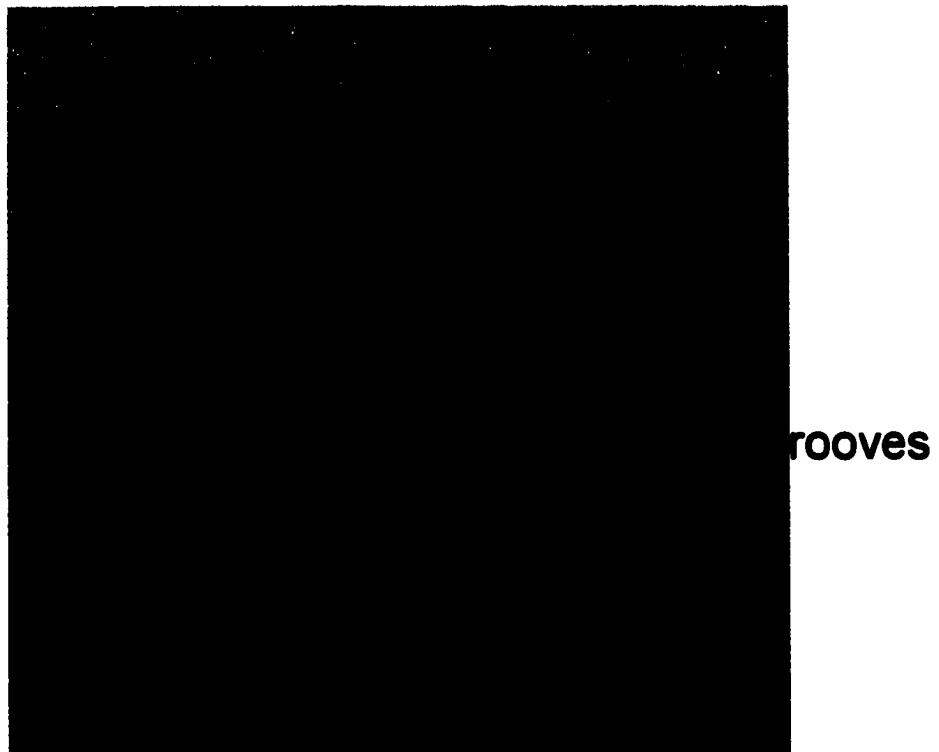
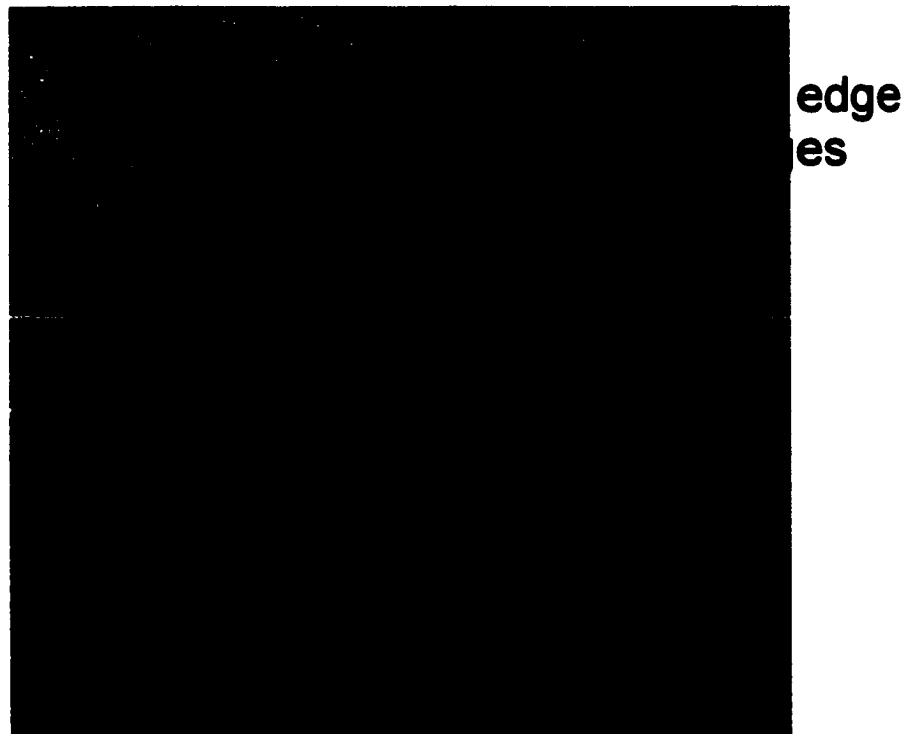


**Fig. 9-3. Nomarski micrograph of the two patterned CdTe epilayers grown sequentially with the modified in situ mask fixture using three posts and holes.**

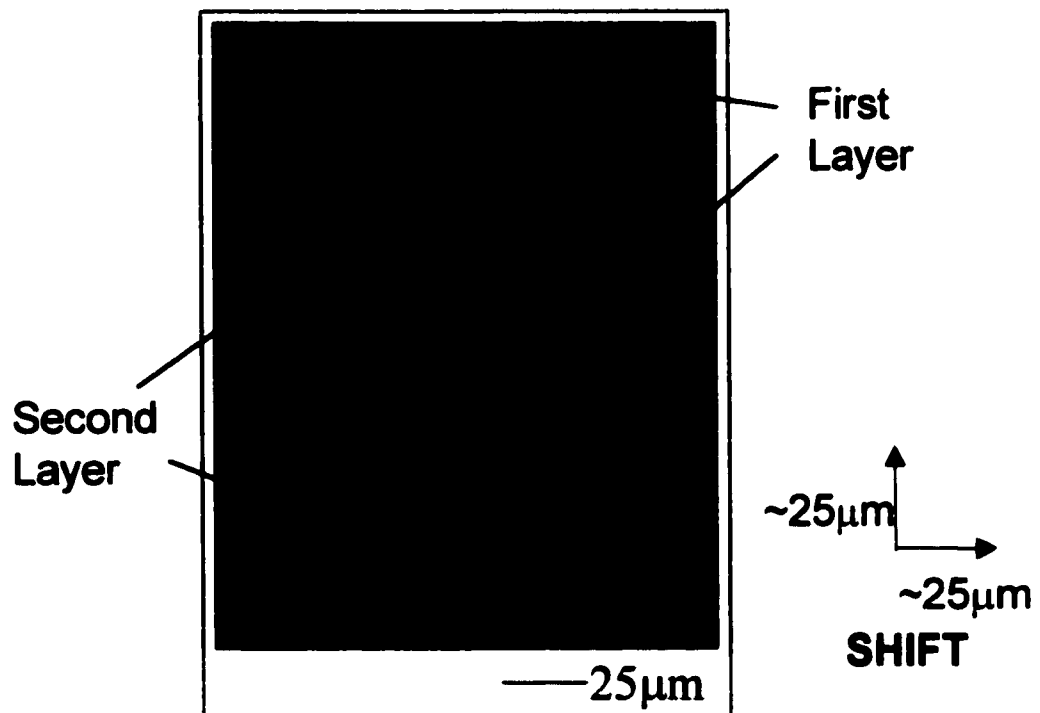
### **9-3. Modification using grooves and knife edges**

To further improve the accuracy of the registration between different layers grown by multiple step SAE, we adopted the idea of using grooves and knife edges to align the mask with the substrate. Since no clearance is needed for the knife edge to fit into the groove, this mechanism is expected to provide much more precise alignment as long as the grooves and knife edges are machined very accurately. This method has been used in other labs and excellent results have been obtained.<sup>[1]</sup>

In the real fabrication, the support ring was machined to have three knife-edge shaped wedges on the bottom. The wedges are 120° apart as with the three posts design introduced in the previous paragraph. The mask has openings of the same shape at the same position respective to the support ring so that it can adhere to the support ring. Fig. 9-4a shows the picture of the bottom side of the mask holder, revealing the mask and the knife-edge wedges of the support ring sticking out of the mask. Fig. 9-4b shows the substrate holder having three grooves drilled with 120° apart. They correspond to the knife-edge wedges in the support ring so that the two can fit well with each other. Fig. 9-5 shows two patterned ZnSe epilayers grown sequentially using this new mask fixture design. The poor feature is due to the use of the metal mask instead of silicon mask since the metal mask is much



**Fig. 9-4. New in situ mask fixture design using knife edges and grooves.**



**Fig. 9-5. Nomarski micrograph of two patterned ZnSe epilayers grown sequentially with the modified in situ mask fixture design using grooves and knife edges.**

easier to be machined to the desired shape. However, it is clear that the misalignment of the two patterned epilayers is significantly reduced to only 25 $\mu$ m in both directions. This slight misalignment may be due to the limited precision in the mechanical machining method used in our machine shop. Higher machining precision may be required.

#### **9-4. Summary**

In conventional device structure processing using photolithographic techniques, the accuracy of alignment can be in the range of tens of nanometer, which is much more precise than what our current *in situ* mask fixture can attain. A more rigorous mask registration mechanism and more precise machining are needed to improve the alignment of the multiple layers grown by the sequential shadow mask SAE.

Although the mask registration problem at present limits the applicability of the shadow mask SAE using the *in situ* mask fixture, there are still potential applications of this technique in some device structures that can use single step SAE or in which less strict registration of multiple layers is required. Due to the advantages the shadow mask SAE technique provides in a way of greatly simplifying the process, we would expect to see increasing applications of this technique in the device fabrication.

**Reference:**

[1] A.Y. Cho, private communication.

## CHAPTER 10

### Summary and Direction for Future Work

#### 10-1. Summary

It has been shown in the previous chapters that we have developed a shadow mask selective area molecular beam epitaxy technique using specially designed masks and mask fixtures. Excellent mesa pattern definition has been obtained by using a near normal incidence flux, a thin mask, and flat and intimate contact between the mask and the substrate. The quality of the patterned epilayers is comparable to that of flat epilayers, according to the defect density studies and the optical photoluminescence measurements.

The shadow mask SAE technique we developed has been applied to the growth of CdTe square arrays as a demonstration of its application in *in situ* patterning of the epilayers, especially in the *in situ* reticulation of HgCdTe detector arrays. Excellent array patterns in the dimensions similar as those used in the typical HgCdTe FPA have been obtained, the surfaces are flat, the edges are sharp and the separations are well defined. To further exploit the advantage of the shadow mask SAE with the *in situ* mask fixture and demonstrate the potential of shadow mask SAE for *in situ* device structure processing, we also performed *in situ* fabrication of Au/CdTe

detector-array-like structures. These structures were fabricated in two steps in the UHV environment without intermediate exposure and processing. Both the patterned CdTe and Au layers are well defined. The *in situ* prepared Au contact exhibits good adhesion properties and low interface contamination. One problem we identified is that the two layers are not completely aligned with each other due to the non-optimized registration of the two masks used in the *in situ* patterning and the *in situ* metallization. However, the *in situ* fabrication of the Au/CdTe detector-array-like structures demonstrates the potential of the shadow mask SAE technique for *in situ* device structure processing.

The shadow mask SAE technique using the *in situ* mask fixture has also been implemented in the fabrication and integration of semiconductor quantum well (QW) structures. It is a requirement that the active region of the laser and LED structures should be laterally restricted to define individual devices. By using shadow mask SAE, we can easily grow patterned QWs sandwiched in flat barrier layers to accomplish this. We can also integrate QWs of different thickness and/or composition on a single substrate to achieve device integration using multiple step SAE. These approaches were demonstrated by the growth and integration of three patterned ZnCdSe QWs of different thickness and Cd composition on a single GaAs substrate using

ZnSe barrier layers, and by the growth and integration of three different patterned ZnCdSe QWs on a single InP substrate using ZnCdMgSe barrier layers. The latter exhibited QW emission in the green, yellow and red spectrum from the individual patterned region, indicating its potential applications in integrated red-green-blue (R-G-B) LEDs based on the (Zn,Cd,Mg)Se material system.

We have also looked into the influence of the shadow mask SAE on the material defect density. The studies show that the defect density of patterned ZnSe epilayers grown on GaAs substrates is comparable to that of flat ZnSe layers grown under similar conditions, indicating no deleterious effect is caused by the use of the shadow mask. However, due to the small lattice mismatch between ZnSe and GaAs and the stacking faults interplay with the misfit dislocations, we were unable to identify if there is a similar defect reduction effect associated with the shadow mask SAE through limiting the growth area as with the oxide mask or patterned substrate SAE that have been previously observed in other material systems.

All these results indicate that the shadow mask SAE technique we developed is promising for *in situ* device structure processing and integration. The current mask fixture design is readily applicable for single step SAE or multiple step SAE that does not require very strict registration. However, a

more rigorous mask alignment mechanism should be pursued for multiple step SAE that requires stringent registration.

## **10-2. Directions for future work**

There are two directions for the future work of shadow mask SAE based on our accomplishments. One is the fabrication of integrated R-G-B LEDs based on the (Zn,Cd,Mg)Se material system and the other is the further investigation of defect reduction effect with shadow mask SAE.

### *10-2-1. Fabrication of integrated R-G-B LEDs based on the (Zn,Cd,Mg)Se material system*

We have demonstrated that shadow mask SAE is a feasible approach to integrate different ZnCdSe QWs on a single substrate. Further work would be to implement this technique to the integration of R-G-B LEDs on a single InP substrate based on the (Zn,Cd,Mg)Se material system. This can be done by integrating R-G-B ZnCdSe QWs on a single InP substrate using identical n-type and p-type ZnCdMgSe barrier layers and p<sup>+</sup> ZnSeTe contact layer.

### *10-2-2. Investigation of the defect density in the strained ZnCdSe/ZnCdMgSe quantum well*

The red (Zn,Cd,Mg)Se based LED is achieved by using strained ZnCdSe/ZnCdMgSe QW (~1.2% lattice mismatch to the InP substrate). The lattice mismatch may result in misfit dislocation defects that act as

**nonradiative recombination centers when the device is operated and therefore limit the device lifetime.**

**We were unable to identify if there is any defect reduction effect associated with the shadow mask SAE. The ZnSe/GaAs material system is not ideal for this study. We propose that the strained red ZnCdSe/ZnCdMgSe QW system eliminates the two problems associated with the ZnSe/GaAs system for the defect reduction study of shadow mask SAE. For one thing, the stacking fault density in the ZnCdSe/ZnCdMgSe QW is low, only those extending from the II-VI/III-V interface, and have already been reduced in our laboratory to the mid  $10^4$  cm<sup>-2</sup> range. Secondly, the lattice mismatch between ZnCdSe and ZnCdMgSe is relatively high (~1.2-1.5% mismatch) which results in a higher density of misfit dislocations above the critical thickness. Therefore it would be interesting to look into the defect density in the strained ZnCdSe/ZnCdMgSe QW grown with shadow mask SAE. Ideally we would compare the defect density in the patterned and non-patterned red ZnCdSe/ZnCdMgSe QWs using Cathodoluminescence, which is a more effective means of measuring defect density.<sup>[1]</sup>**

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