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**SCHOTTKY CELL MEMORY TECHNOLOGY
FOR NONVOLATILE MEMORY APPLICATIONS**

by

Zhongwei Pan

A research dissertation submitted to
the Graduate Faculty in Engineering
in partial fulfillment of the requirements
for the Degree of
DOCTOR OF PHILOSOPHY
The City University of New York

2001

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This manuscript has been read and accepted for the Graduate Faculty in School of Engineering in satisfaction of the dissertation requirement for the Degree of DOCTOR OF PHILOSOPHY.

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ABSTRACT

SCHOTTKY CELL MEMORY TECHNOLOGY FOR NONVOLATILE MEMORY APPLICATIONS

by

Zhongwei Pan

Dissertation Advisor: Professor Kai Shum

This Ph.D. dissertation demonstrates a novel concept for nonvolatile memory (NVM). The concept may become a new technology for NVM. We shall call this new technology as Schottky Cell Memory (SCM) technology. SCM is based on the alterable Schottky barrier height arising from the reversible electron movement from an electric-field-controlled charge source near a metal-semiconductor Schottky interface to an adjacent quantum well. Depending on the resultant charge state in the adjacent quantum well, this movement modulates the current flowing over the Schottky barrier, thereby differentiating at least two states which correspond to “1” and “0” of stored data. Once the device is on a particular

state, the device retains memory of the state it has been set on, even if it is held at zero bias for long periods of time. The device can be electrically addressed in a high-density device matrix. The state of the device can be repetitively switched by a positive or negative voltage pulse and can be read at a low sense voltage without destroying it. The device requires low power for switching and reading, is nonvolatile, is radiation tolerant, and is compatible with other conventional device processing for integration with microelectronic elements on a same substrate such as silicon (Si), gallium arsenide (GaAs), and indium phosphor (InP).

DEDICATION

To my parents, my wife, my younger sister and my loyal friends
for their newer ending support

ACKNOWLEDGMENTS

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CHAPTER 1

Introduction

Information stored in the existing semiconductor memories such as dynamic random access memories (DRAMs) and static random access memories (SRAMs) disappears when power is lost. As a result, critical information is usually stored on peripheral magnetic disks and tapes. Since the access speed at which a CPU can load and process data has greatly outpaced the ability of magnetic memory devices to store and retrieve the data, rotation-related storage devices become bottlenecks in data access and transfer. This is particularly true for the case of on-line transaction processing and large engineering programs.

In an attempt to reduce these bottlenecks, most systems now include caches. A cache is a relatively small amount of very fast solid-state memory devices that sit between the CPU and the data storage unit. The short access time and very fast high transfer rates of these devices supply data quickly and more closely match the performance of today's powerful CPUs. However, for any rotation-related storage unit, the access time and data transfer bandwidth are currently limited to a few 100 μ s and 20

Mbits/s, respectively. Moreover, the cost of cache is about 50 to 100 times more expensive than that of magnetic disks.

An ideal “alternative best” to completely overcome this speed bottleneck is to replace the rotation-related storage devices by nonvolatile memory (NVM). NVM can retain the stored data for extremely long periods of time without an external applied power. NVM not only can be accessed as fast as DRAMs and SRAMs, but also can be more reliable than rotation-related storage units. Commercial NVM products, such as ferroelectric random access memories (FRAMs) and Flash memories, have already been used for video and audio recording applications. More commercial products that use NVM technology to store data are being introduced each day in a wide variety of applications, ranging from cellular phones, pagers, palm PCs, hand PCs, digital clocks, VCRs, answering machines, sub-notebook computers to military and space missions.

Our solid-state device research group at CCNY has made a major breakthrough in developing a new technology for NVM. The novelty and ingenuity of this new technology, called Schottky Cell Memory (SCM) technology, uses a unique combination of the Schottky junction with electrically controllable barrier height and an adjacent quantum well separated by a semiconductor layer to store data. This technique has been

demonstrated in many devices based on the following two material systems: (1) II-VI Al/ZnCdSe/ZnCdMgSe/ZnCdSe/InP (buffer layer)/n⁺-InP (substrate), and (2) III-V Au/GaAs/AlGaAs/GaAs/AlAs/GaAs (buffer layer)/n⁺-GaAs (substrate). Those SCM devices were grown by molecular beam epitaxy (MBE).¹ Compared to conventional rotation-related storage technologies, the SCM technology should allow much high access speed to store information. Moreover, unlike conventional DRAMs and SRAMs, the SCM is nonvolatile, low cost, high density and long-term data storage reliability. It is expected to be less prone to write/erase degradation since the memory cell does not rely on hot electron injection compared to conventional floating-gate mechanism.

During the Ph.D. research period, the main objectives are (1) to further investigate its origin and mechanism of electric-field-controlled charge centers near the metal-semiconductor interface; (2) to demonstrate the concept in III-V semiconductor material systems such as Au / GaAs / AlGaAs / GaAs / AlAs / GaAs (buffer layer) / n⁺-GaAs (substrate); (3) to simulate SCM device's energy diagram and to test and measure the NVM's basic functional parameters to further design and optimize its structure; (4) to further study SCM device's nonvolatile memory

characteristics; and (5) to propose some more practical structures by analyzing above various mechanisms.

In Chapter 2, we will briefly report two main existing conventional NVM technologies (floating-gate and ferroelectric technologies), their design's principles, and the comparison of their technology criteria. In Chapter 3, a computer simulation program – one-dimensional self-consistent Poisson – Schrödinger solver will be described. This program will mainly be applied for device design. Its basic principle, algorithm, boundary conditions, and some practical examples will be discussed therein.

The concept of our NVM technology – Schottky cell memory (SCM), its basic principles, optimum plans, and its technological prospect will be introduced in Chapter 4. Chapter 5 will mainly discuss our SCM device growth and fabrication. MBE principle, MBE system, its growth procedure, and device fabrication will briefly be introduced.

In Chapter 6 and 7, we will mainly report two successful demonstrations. One is the II-VI Al/ZnCdSe/ZnCdMgSe/ n^+ -InP SCM device; the other is III-V Au/AlGaAs/GaAs/ n^+ -GaAs SCM device. The basic NVM functional characteristics for SCM will be discussed in detail during these two chapters. Moreover, we will also further investigate its

original and mechanism of the electric-field-controlled charge source. As a result, a novel type mode (electric-field-enhanced tunneling model) will be proposed to analyze our experimental results and further unveil its intrinsic mechanism of electric-field-controlled charge source in Chapter 6. In Chapter 7, we still will apply computer simulation to design and optimize our SCM structure in order to further improve its performance.

Finally, in Chapter 8, we will prospect the future of our SCM technology. This Ph.D. research work will be summarized in Chapter 9, after that, we will point out a kind of circuit architecture for NVM as our future work therein.

Reference

- ¹ Kai Shum, J. Zhou, W. Zhang, L. Zeng, and M. C. Tamargo, Appl. Phys. Lett. **71**, 2487 (1997).

CHAPTER 2

Background on NVM Technologies

2.1 Introduction

There are a wide variety of semiconductor structures that can act as NVM elements. Nowadays, there are two main existing technologies. One is the floating-gate technology that produces electrically erasable programmable read-only memories (EEPROMs) and Flash Memories. Another is the ferroelectric technology that yields ferroelectric random access memories (FRAMs).

2.2 Floating-gate technology

The general floating-gate transistor device structure is depicted schematically in Figure 2.1(a) and (b). A thin (~ 100 Å) dielectric layer between the floating gate and the drain enables the flow of electrons into and from the floating gate during WRITE/ERASE operations by means of Fowler-Nordheim tunneling.

In the WRITE operation the floating gate is charged negatively with electrons tunneling from the drain through the thin oxide layer (SiO_2) as shown in Figure 2.1(c). This is achieved by applying a positive voltage pulse to the top gate of the cell, while the source, drain, and substrate are grounded. The stored negative charge trapped on the floating gate shifts the transistor's threshold voltage (V_T), as measured on the top gate, toward a more positive value. In a subsequent READ operation the transistor will not conduct channel current.

The ERASE operation removes electrons from the floating gate by applying a positive high-voltage pulse at the drain, while the source is floating and both the top gate and the substrate are grounded. The threshold voltage is shifted in the negative direction, and channel current will flow during subsequent READ operation. Figure 2.1(d) shows the schematic I-V characteristics of the programmed and not-programmed floating-gate transistor.

During READ operation the voltage used is low enough so that tunneling current is negligible, and the floating gate is practically insulated. An erased cell will exhibit a channel current which is detected by a sense amplifier to identify a first logic level "0", while a programmed

cell will not draw any current which is associated with the other logic level “1”.

In memory circuits, a two-transistor cell is applied; the additional transistor is necessary in order to isolate the cell from adjacent cells during WRITE/ERASE operations.

The main drawbacks¹ of this floating-gate technology are: (1) poor write/erase endurance and (2) relatively high voltage operation.

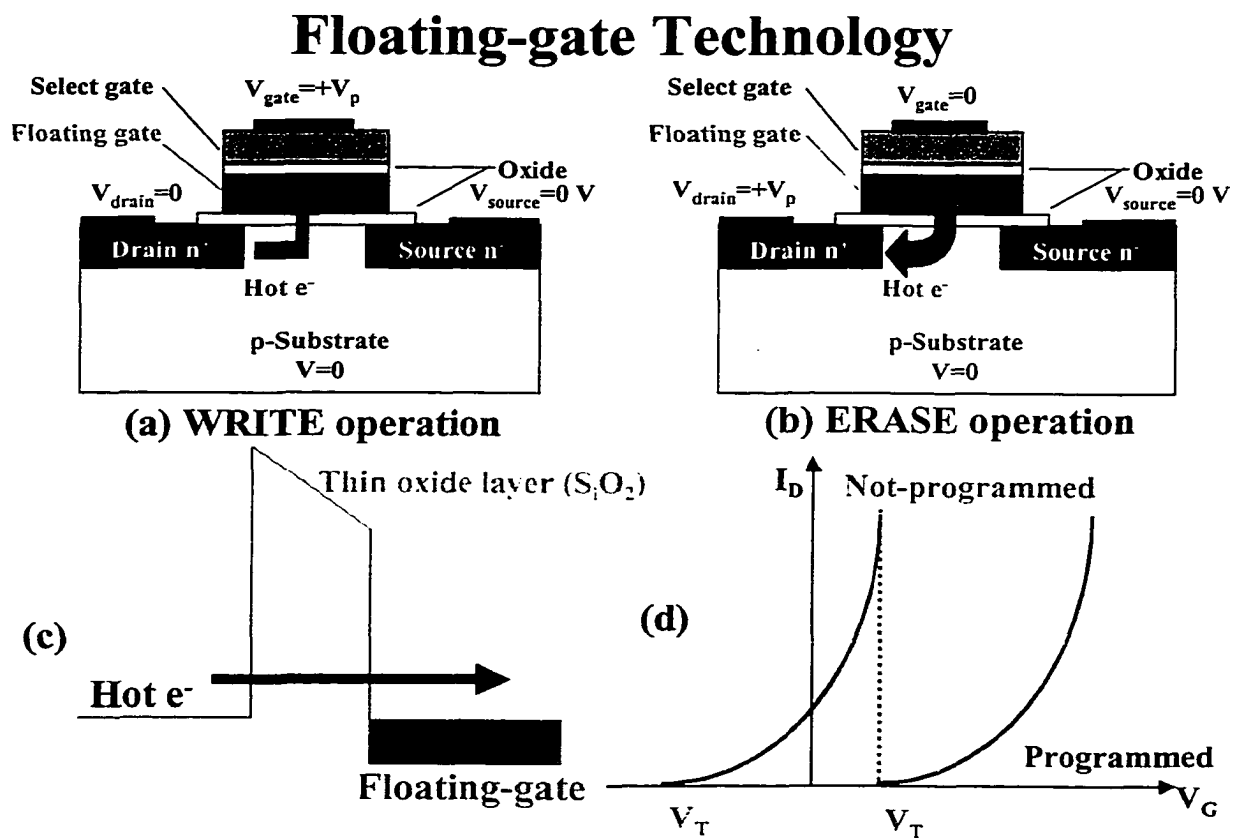


Figure 2.1 (a) (b) Schematic programming process (WRITE/ERASE operations) of the EEPROM (Intel cell), respectively. (c) Schematic hot e^- tunneling. (d) Schematic I - V curves for not-programmed and programmed floating-gate transistor.

2.3 Ferroelectrics technology

A ferroelectric thin-film memory capacitor exhibits a characteristic hysteresis behavior relating polarization (P) and applied field (E) as shown in Figure 2.2(a). There is a nominal threshold (or coercive field E_c), above which the polarization changes sign. The two zero-field values ($\pm P_r$) are equally stable. Thus, no applied voltage is required to maintain the memory of polarization states. A simplified unit cell model of a ferroelectric crystal is shown in Figure 2.2(b). An externally applied electric field moves the center atom into one of the two stable positions shown based upon the direction of the field. Once the external field is removed, the central atom remains in a stable position —preserving the state of the memory. External circuits sense this type of atom displacement and set the memory cell's digital state to a "0" or a "1". The state of the memory can be changed by simply reversing the direction of the electric field. The charge to be switched in a ferroelectric capacitor is about $20 \mu\text{C}/\text{cm}^2$, an order of magnitude higher than the value of $1.7 \mu\text{C}/\text{cm}^2$ typical of current DRAM capacitors.

Figure 2.2(c) depicts cross-section of the IMEC design for an integrated ferroelectric memory cell with a metal strap connection between top

electrode and transistor source/drain. IMEC is the largest Independent Micro-Electronics R&D Center in Europe. The FRAM technology appears to be about three generations behind Flash in terms of bit density, the key for producing high density FRAM is the technology of integrating ferroelectric capacitor to the Si integrated circuit. Current commercial products are available at 256 Kbit with 120 ns write/read access time, 10^{10} read/write cycle time, retention time of 10 years from Ramtron Corp., Colorado.

One major drawback² for the FRAM technology is the device's density. Up to now, the United States, Europe and Japan's FRAM products still stay on 256-Kbit versions. Till 1999, Samsung Electronics Company³ has recently developed the world's first 4-Mbit FRAM.

Ferroelectric Technology

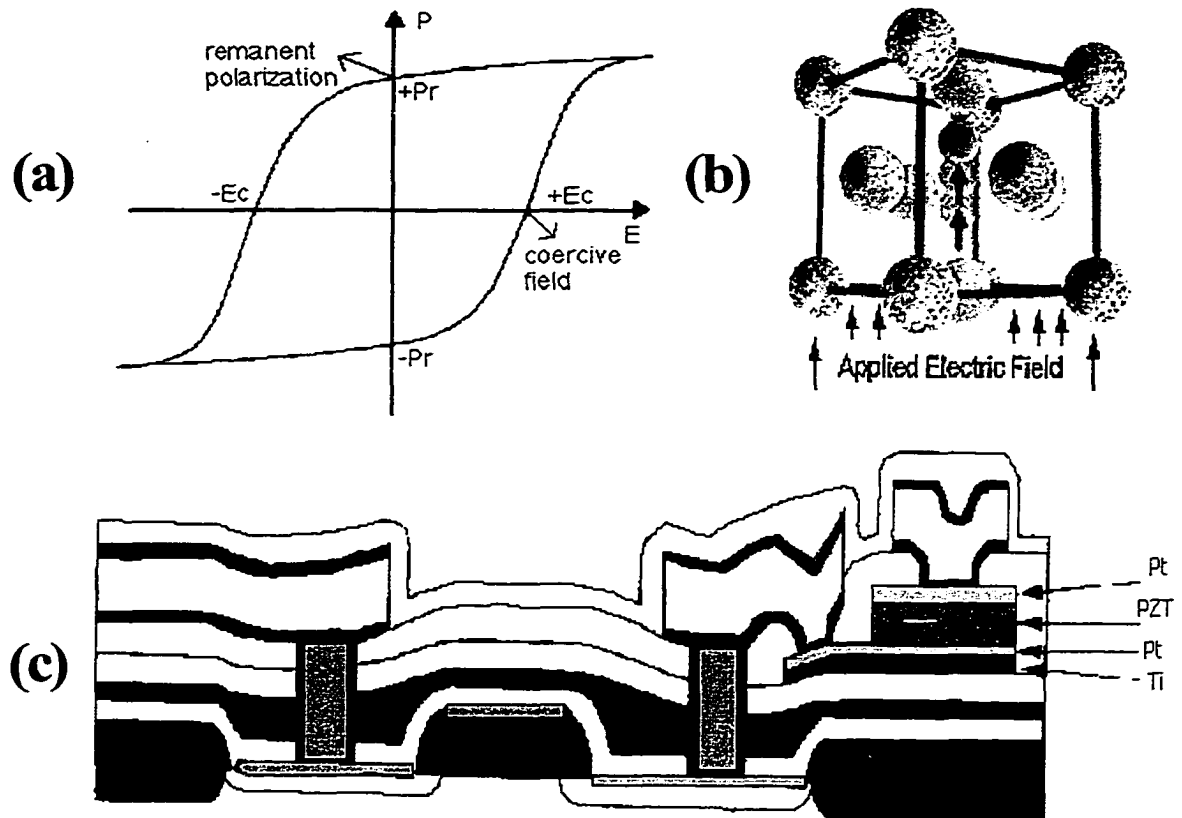


Figure 2.2 (a) Schematic of typical hysteresis behavior of ferroelectric capacitor. (b) A simplified unit model of a ferroelectric crystal. (c) Cross-section of the IMEC design for an integrated ferroelectric memory cell with a metal strap connection between top electrode and transistor source / drain. PZT stands for lead zirconate titanate material.

2.4 Comparison of floating-gate and ferroelectric technologies

In the following Table 2.1,³⁻⁸ technologies (FRAM, EEPROM, and Flash) are compared against a number of technology criteria. In Table 2.2,⁴⁻⁶ we list some main nonvolatile memory manufacturers and their websites. Note: All web addresses start with <http://> unless otherwise stated.

Table 2.1 Nonvolatile memory technology comparison

Technology	Ferroelectrics	Floating-gate	
Product	FRAM	EEPROM	FLASH
Highest density	4 Mbit ³	256 Kbit ⁸	32 Mbit ⁷
Write speed	150 to 200 (nsec)	10 (msec)	5 to 10 (μsec)
Read speed	150 to 200 (nsec)	60 to 150 (nsec)	70 to 150 (nsec)
Cycling endurance	10 ¹⁰ to 10 ¹² (both reads and writes)	10 ⁵ (writes only, reads infinite)	10 ⁶ (writes only, reads infinite)
Retention	> 10 years	> 20 years	> 20 years

Table 2.2 Some main nonvolatile memory manufacturers

Advanced Linear Devices www.aldinc.com	Analog Devices www.analog.com	AMD www.amd.com
Atmel Corp www.atmel.com	Catalyst Semiconductor www.catsemi.com	Cirrus Logic www.cirrus.com
Dallas semiconductor www.dalsemi.com	Datalight Corp www.datalight.com	Fairchild Semiconductor www.fairchildsemi.com
Fujitsu Microelectronics www.fujitsumicro.com	Hitachi America Ltd www.hitachi.com	Hyundai Electronics America www.hea.com
Information Storage Devices www.isd.com	Integrated Silicon Devices www.isd.com	Integrated Systems Inc www.isi.com
Integrated Silicon Solution www.issiusa.com	Intel Corp www.intel.com	Kingston Technology www.kingston.com
LG Semicon www.lg.co.kr	M-Systems Flash Disk Pioneers www.m-sys.com	Macronix America Inc www.macronix.com
Matsushita Electric Corp of America www.panasonic.com	Microchip Technology Inc www.microchip.com	Micron Technology Inc www.micron.com
Motorola Corp www.mot.com	Oki Semiconductor www.okisemi.com	Phoenix Technologies Ltd www.phoenix.com
National Semiconductor www.national.com	NEC Electronics Inc www.nec.com	Philips Semiconductors www.philips.com
Ramtron International Corp www.ramtron.com	Samsung semiconductor www.samsung.com	SGS-Thomson Microelectronics www.st.com
Silicon Storage Technology www.ssti.com	Simtek www.simtek.com	Toshiba America Electronic Components Inc www.toshiba.com
Summit Microelectronics www.summitmicro.com	Texas Instruments Inc www.ti.com	Xicor www.xicor.com

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CHAPTER 3

One-dimensional Self-consistent Poisson-Schrödinger Simulations

3.1 Introduction

To further understand nonvolatile memory devices, it is necessary to both qualitatively and quantitatively analyze the device. A qualitative analysis can often be made using the basic principles of quantum mechanics, along with some simplifying assumptions. However, a quantitative analysis is generally more difficult because the devices often do not lend themselves to closed solutions, and numerical solutions are needed. As part of this dissertation, a self-consistent one-dimensional Poisson-Schrödinger simulation program was applied to analyze nonvolatile memory structures where a closed form solution is not possible. The calculation of energy band diagrams and wave functions fosters a greater qualitative understanding of the operation of the simulated device. The main purpose of this chapter is to present the physics behind the simulations, along with an outline of the features of the program.

3.2 Basic equations

To find the potential energy profile and carrier concentration in a semiconductor device where quantum mechanics play an important role, it is necessary to solve both the Poisson and Schrödinger equations self-consistently. In general, a numerical solution is needed. The method of finite differences can be used.^{1,2} The first equation is the one-dimensional Poisson equation:

$$\frac{d}{dz}[\epsilon_s(z) \frac{d}{dz} \Phi(z)] = -q \{N_D^+(z) - n(z) - N_A^-(z) + p(z)\} \quad (3.1)$$

where Φ the electrostatic potential in volts, ϵ_s the semiconductor dielectric constant, N_D the ionized donor concentration, N_A the ionized acceptor concentration, p the hole concentration, n the electron concentration, and $q = 1.6 \times 10^{-19} \text{ C}$.

The other primary equation is the one-dimensional (1D), time independent, effective mass Schrödinger equation:³

$$-\frac{\hbar^2}{2} \frac{d}{dz} \left[\frac{1}{m^*(z)} \frac{d}{dz} \Psi(z) \right] + V(z) \Psi(z) = E \Psi(z) \quad (3.2)$$

where Ψ the electronic wave function, E the energy, V the potential energy, $\hbar$ Planck's constant divided by 2π , and m^* the effective mass of carriers (either electrons or holes). Electron-electron, hole-hole, electron-

hole, electron-phonon, and hole-phonon interactions are neglected. Equation 3.2 is valid if only one semiconductor energy band is considered. The eigen energy states can be found by solving Equation 3.2 separately for each carrier type, using the appropriate values of m^* and V for each carrier.

The objective is to find a conduction band profile and a carrier distribution which satisfy both Equations 3.1 and 3.2. First, it is necessary to define how these physical quantities are related to the variables in Equations 3.1 and 3.2. The energy of the conduction band edge is:

$$E_c(z) = V(z) = -q\Phi(z) + \Delta E_c(z) \quad (3.3)$$

where $\Delta E_c(z)$ the conduction band offset at the heterostructure interface, for example: $\Delta E_c(z)$ is 0.23 eV for $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ relative to GaAs. The energy of the valence band edge is $E_v(z) = V(z) = -q\Phi(z) + \Delta E_v(z)$. In these calculations thermal equilibrium is assumed. A given temperature is entered into the simulations explicitly in the calculation of carrier densities.

The energy eigenvalues of the Schrödinger equation give the quantized subband energies. These, in conjunction with the wave functions are used to calculate the electron concentration in the structure by the following equation:

$$n(z) = \sum_{k=1}^m \Psi_k^*(z) \Psi_k(z) n_k \quad (3.4)$$

where m is the number of bound states, and n_k is the electron concentration in each subband which includes the two-dimensional (2D) density of states, and the Fermi occupation probability of each subband:

$$n_k = \int_{E_k}^{\infty} \frac{m^*}{\pi \hbar^2} \frac{dE}{[1 + \exp(\frac{E - E_f}{kT})]} \quad (3.5)$$

where E_k is the eigen-energy.

An iteration procedure is applied to obtain self-consistent solutions for Equations 3.1 and 3.2. Starting with a trial potential $V(z)$, the wave functions, and their corresponding eigen-energies, E_k can be used to calculate the electron density distribution $n(z)$ using Equation 3.4 and 3.5. The computed $n(z)$ and a given donor concentration $N_D(z)$ is then used to calculate $\Phi(z)$ via Equation 3.1. The new potential energy $V(z)$ is again calculated by Equation 3.3. The subsequent iteration will yield the final self-consistent solutions for $V(z)$ and $n(z)$ which satisfy certain error criteria. These are several 1D self-consistent Poisson-Schrödinger solvers available through Internet. We have used the latest version of 1D Poisson-Schrödinger solver provided by Professor Gregory. L. Snider, who has published several papers using this solver.⁴⁻⁶

3.3 Simulation input file

The one-dimensional Poisson-Schrödinger solver is a very useful design tool where every user can easily evaluate the semiconductor devices. When a device is ready to simulate, an input file is required which contains the device structure information, the boundary conditions and the simulation parameters. The following file as shown in Figure 3.1 is a III-V SCM device's input file. The detailed results will be expressed in Chapter 7. The first part of this input file is to describe the device's parameters (Schottky barrier height, each layer's width, doping concentration, and calculated mesh's size). Our device's detailed structure is Au(3000 Å)/i-GaAs(50 Å)/n-Al_xGa_{1-x}As(5000 Å, x=0.30, Si: $5 \times 10^{16} \text{ cm}^{-3}$)/i-GaAs(56 Å)/i-AlAs(20 Å)/n⁺-GaAs(1500 Å buffer layer, Si: $2 \times 10^{18} \text{ cm}^{-3}$) on n⁺-GaAs substrate. The bias voltage, v_1 , is 0. The second part is used for calculating the quasi-bound wave function and its bound eigen-energy. Its starting point is 4800 Å and ending point is 5120 Å. The adjacent quantum well is just right in this region [4800 Å, 5120 Å]. Assume all of donors will be fully ionized. The device is simulated at room temperature (300 K) and the default value for calculated mesh size is 10 Å.

```

# test comment
surface schottky=0.6  v1
GaAs  t=50
AlGaAs t=5000  Nd=5e16  x=.3  dy=50
GaAs  t=56
AlAs  t=20
GaAs  t=1500  Nd=2e18  dy=50
substrate

fullyionized
v1 0.0
schrodingerstart=4800
schrodingerstop=5120
temp=300K
dy=10

```

Figure 3.1 Sample input file for 1D Poisson-Schrödinger program

3.4 Simulation examples

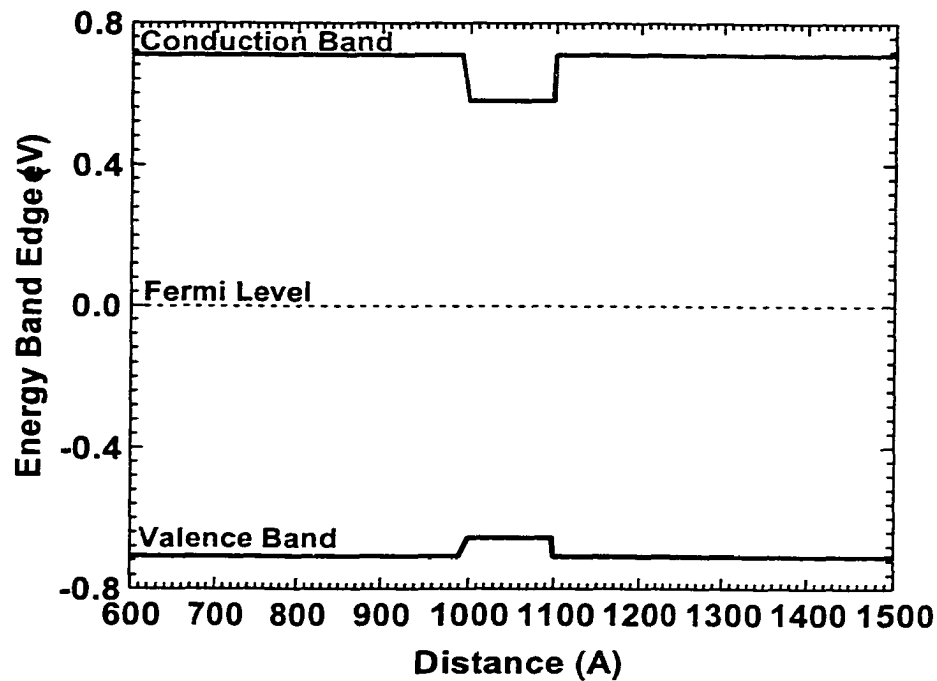
In this section, several simulation examples (intrinsic, n-type, p-type, and n-type/p-type δ -doped $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ semiconductor structures) are provided to demonstrate how the 1D Poisson-Schrödinger solver works.

Figure 3.2 shows the intrinsic heterostructure's energy band diagram. We selected an $\text{InGaAs}/\text{GaAs}$ semiconductor material system. The detailed structure is GaAs (1000 Å)/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x=0.20$, 100 Å)/ GaAs (1000 Å).

Both terminals of this device are ohm contacts. The region of quasi-wave function and its eigen energy is [890 Å, 1210 Å]. From Figure 3.2, we observed the structures of both conduction band and valence band. Since the device was not doped, the Fermi level was set in the middle position between conduction band and valence band, and no any quasi-wave function and its eigen energy was found.

Figure 3.3 – 3.6 show the simulated energy band diagrams for the devices which were doped to n-type, p-type, δ -doping n-type, and δ -doping p-type structure in InGaAs layer, respectively. Their structures are approximately same to the above except that the InGaAs layer was doped to n-type ($N_d=1\times 10^{18} \text{ cm}^{-3}$), p-type ($N_a=1\times 10^{18} \text{ cm}^{-3}$), n-type δ -doping (width=20 Å, $N_d=1\times 10^{19} \text{ cm}^{-3}$), and p-type δ -doping (width=20 Å, $N_a=1\times 10^{19} \text{ cm}^{-3}$) structure, respectively. When the device was δ -doped, the simulated region of quasi-wave function and its eigen energy is [850 Å, 1170 Å]. Both n-type and p-type doping densities in the GaAs layers were $1\times 10^{16} \text{ cm}^{-3}$. From Figure 3.3 – 3.6, we clearly observed the energy band diagrams (conduction band, valence band, and Fermi level) and their corresponding position relationship. Meanwhile, in InGaAs quantum well, the quasi-wave functions and their corresponding eigen energies were

obtained. Those simulation results are identical to the classical semiconductor energy band's theory.

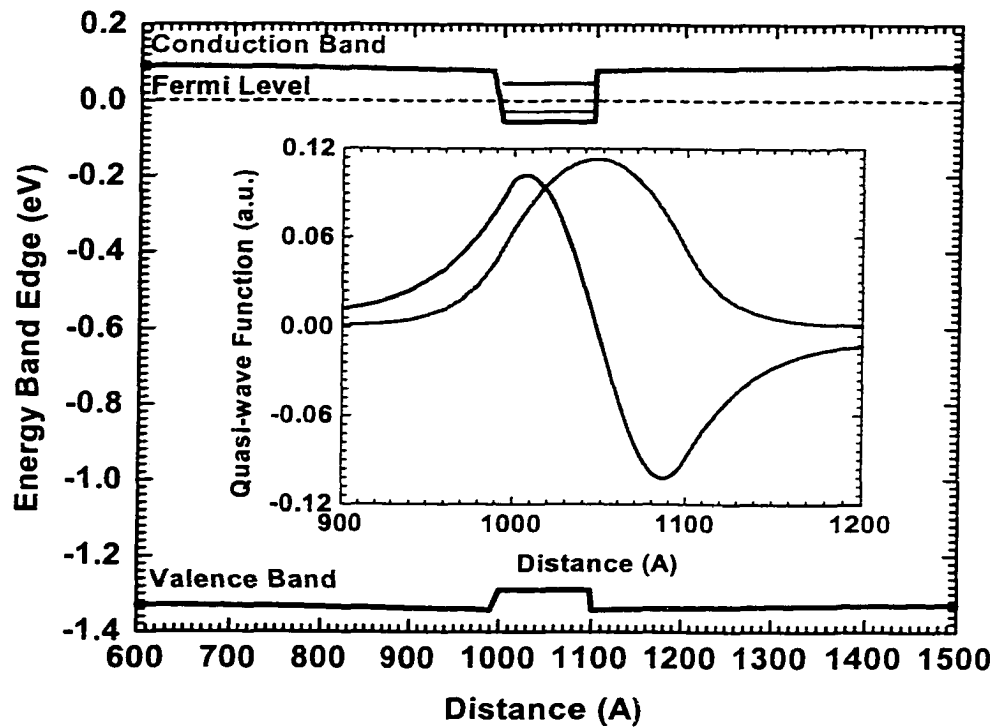


intrinsic structure simulation input file:

```
# test comment
surface ohmic v1
GaAs t=1000
InGaAs_GaAs x=0.2 t=100 dy=2
GaAs t=1000
substrate ohmic v2

fullyionized
v1 0.0
v2 0.0
schrodingerstart=890
schrodingerstop=1210
temp=300K
dy=10
```

Figure 3.2 shows the intrinsic GaAs/InGaAs/GaAs structure's energy band diagram simulation results. The below is 1D Poisson-Schrödinger solver's input file.

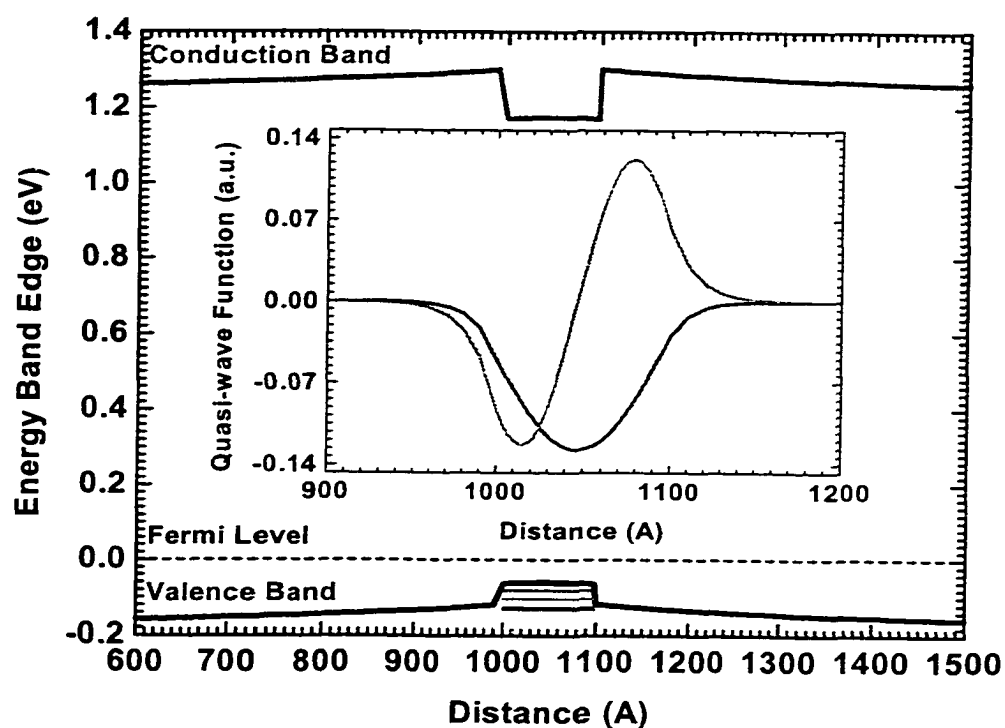


n-type structure simulation input file:

```
# test comment
surface ohmic v1
GaAs t=1000 Nd=1e16
InGaAs_GaAs x=0.2 t=100 Nd=1e18 dy=2
GaAs t=1000 Nd=1e16
substrate ohmic v2

fullyionized
v1 0.0
v2 0.0
schrodingerstart=890
schrodingerstop=1210
temp=300K
dy=10
```

Figure 3.3 shows the n-type GaAs/InGaAs/GaAs structure's energy band diagram simulation results. The inset is their quasi-wave functions of electrons bound in the heterostructure quantum well. The below is 1D Poisson-Schrödinger solver's input file.

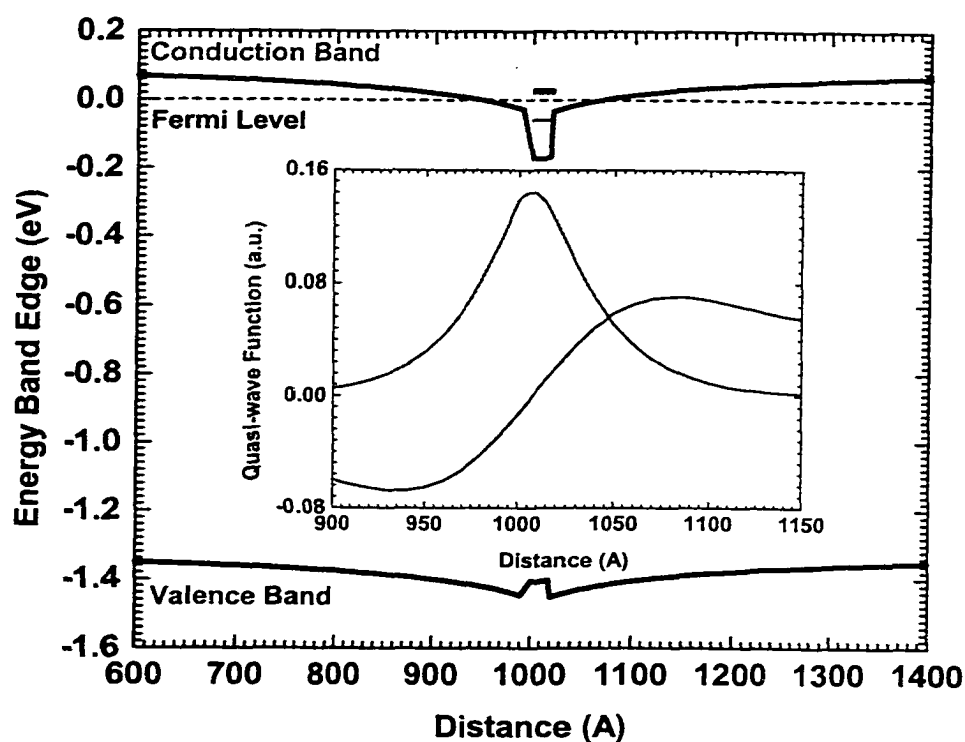


p-type structure simulation input file:

```
# test comment
surface ohmic v1
GaAs t=1000 Na=1e16
InGaAs_GaAs x=0.2 t=100 Na=1e18 dy=2
GaAs t=1000 Na=1e16
substrate ohmic v2

fullyionized
v1 0.0
v2 0.0
schrodingerstart=890
schrodingerstop=1210
temp=300K
dy=10
```

Figure 3.4 shows the p-type GaAs/InGaAs/GaAs structure's energy band diagram simulation results. The inset is their quasi-wave functions of holes bound in the heterostructure quantum well. The below is 1D Poisson-Schrödinger solver's input file.

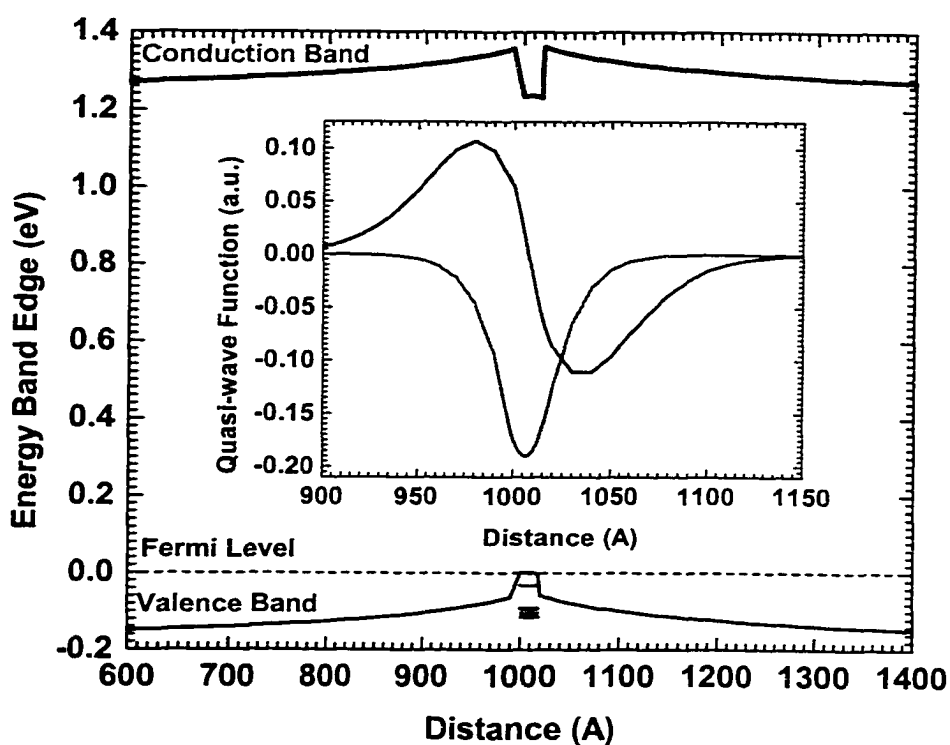


n-type δ -doped structure simulation input file:

```
# test comment
surface ohmic v1
GaAs t=1000 Nd=1e16
InGaAs_GaAs x=0.2 t=20 Nd=1e19 dy=2
GaAs t=1000 Nd=1e16
substrate ohmic v2

fullyionized
v1 0.0
v2 0.0
schrodingerstart=850
schrodingerstop=1170
temp=300K
dy=10
```

Figure 3.5 shows the n-type δ -doped GaAs/InGaAs/GaAs structure's energy band diagram simulation results. The inset is their quasi-wave functions of electrons bound in the heterostructure quantum well. The below is 1D Poisson-schrödinger solver's input file.



p-type δ -doped structure simulation input file:

```
# test comment
surface ohmic v1
GaAs t=1000 Na=1e16
InGaAs_GaAs x=0.2 t=20 Na=1e19 dy=2
GaAs t=1000 Na=1e16
substrate ohmic v2

fullyionized
v1 0.0
v2 0.0
schrodingerstart=850
schrodingerstop=1170
temp=300K
dy=10
```

Figure 3.6 shows the p-type δ -doped GaAs/InGaAs/GaAs structure's energy band diagram simulation results. The inset is their quasi-wave functions of holes bound in the heterostructure quantum well. The below is 1D Poisson-schrödinger solver's input file.

References

- ¹ G. L. Snider, Ph.D. dissertation *‘Design, Fabrication, and Analysis of Split-gate Ballistic Constrictions’*, University of California, Santa Barbara, 1991.
- ² F. S. Acton, *Numerical Methods that Work*, New York: Harper and Row, 1970.
- ³ G. Bastard, Phys. Rev. B **25**, 7584 (1981).
- ⁴ G. L. Snider, I. H. Tan, and E. L. Hu, J. Appl. Phys. **68**, 5922, 1990.
- ⁵ I. H. Tan, G. L. Snider, and E. L. Hu, J. Appl. Phys. **68**, 4071, 1990.
- ⁶ G. L. Snider, I. H. Tan, and E. L. Hu, J. Appl. Phys. **68**, 2849, 1990.

CHAPTER 4

Concept of Schottky Cell Memory

4.1 Introduction

Conventional nonvolatile memory technologies, although they are mature and rather robust, do have their own drawbacks. Scientists still continue to find better alternatives. Our solid-state device research group is involved in an extensive research focused on devising and developing an entirely new class of NVM technology. The approach the research group came up with – Schottky cell memory (SCM) – is able to save data in the event of a power failure by making electrons of electric-field-controlled charge source drift into an adjacent potential quantum well. The key of our SCM technology is two elements. One is that SCM consists of electric-field-controlled charge source near the metal-semiconductor Schottky interface and an adjacent quantum well. The other is reversible electron movement between charge source and an adjacent quantum well modulates the current flowing over the Schottky barrier, therefore differentiating at least two states which correspond to “1” and “0” of stored data. The total

SCM device roughly is divided into six regions: metal contact, Schottky barrier, electric-field-controlled charge source, carrier (electron/hole) transport, potential quantum well for storing carrier (electron/hole), and n^+/p^+ -semiconductor substrate. Besides, possessing all characteristics of nonvolatile memory, this new SCM device still has very low write/erase voltage and simple memory structure. Therefore, it is expected to become a new member of the entire existing NVM family.

In this Chapter, we are concerned with SCM's basic physical principles, device model and device structures. Since Schottky junction is an important and essential component of the SCM device, its Schottky effect and alterable Schottky barrier height play a crucial role in modulating the magnitude of device's currents which corresponds on-state and off-state, respectively. So, we will start to discuss SCM's principle from Schottky junction's characteristics.

4.2 Schottky junction – a simple model

The ideal energy band diagram for a particular metal and n-type semiconductor before contact is shown in Figure 4.1 (a). The vacuum level is used as a reference level. The parameter, Φ_m , the metal work function, is

defined as the minimum energy required for an electron to escape from the metal surface (i.e., Fermi level) into free space at $T = 0$ K. Φ is the semiconductor work function, and χ is known as the electron affinity. Table 4.1 (a) and (b) give the work functions of various metals and the electron affinities of several semiconductors, respectively. In Figure 4.1 (a), we have assumed that $\phi_m > \phi_s$. For this situation, the metal-n-semiconductor energy band diagram is shown in Figure 4.1 (b). The Schottky barrier height, seen by electrons in the metal trying to move into the semiconductor, is given, ideally, by

$$\Phi_B = \Phi_m - \chi \quad (4.1)$$

If an external electric field is applied to the metal surface, then so-called Schottky effect or image lowering effect appears. To understand the Schottky effect, let us consider the energy band diagram shown in Figure 4.2 (b) and (c). Figure 4.2 (b) is a plot of the potential energy assuming that no other electric fields exist. When an electric field is applied to metal surface, electrons that escape from the metal surface will experience two external forces: the image force which arises from the Coulomb attractive force due to the positive image charges induced inside the metal by the escaping electrons, and the Lorentz force due to the applied electric field. The positive image charges create a Coulombic attractive force which

tends to pull the escaping electrons back into the metal. The image force can be expressed by

$$F_i = -\frac{e^2}{16\pi\epsilon_s x^2} \quad (4.2)$$

This image effect is shown in Figure 4.2 (a). The potential energy associated with this image force is given by

$$V_i(x) = -\int_{\infty}^x F_i dx \quad (4.3)$$

The potential energy due to the applied electric field can be written as

$$V_a(x) = -eEx \quad (4.4)$$

Finally, the total potential energy of the electron is equal to the sum of above two equations, namely,

$$V(x) = V_i(x) + V_a(x) = -\frac{e^2}{16\pi\epsilon_s x} - eEx \quad (4.5)$$

The distance at which the maximum potential energy occurs is obtained by differentiating Equation 4.5 with respect to x and then setting the result equal to zero. This yields

$$x_m = \sqrt{\frac{e}{16\pi\epsilon_s E}} \quad (4.6)$$

Meanwhile, we also obtain the maximum potential energy for the electrons,

$$V_m(x_m) = -\frac{e^2}{16\pi\epsilon_s x_m} - eEx_m = -2eEx_m = -e\Delta\phi \quad (4.7)$$

It is shown in Figure 4.2 (c) that the effect of the image force and the applied electric field is lower the Schottky barrier height of a metal-semiconductor Schottky junction. Therefore, the effective metal-semiconductor Schottky barrier height under the applied electric field can be obtained from Figure 4.2 (c), and the result is

$$e\phi_{effective} = e\phi_{B0} + V_m = e\phi_{B0} - e\Delta\phi = e\phi_{B0} - e\sqrt{\frac{eE}{4\pi\epsilon_s}} \quad (4.8)$$

where $e\Delta\phi = -V_m$ is the image lowering potential energy.

To directly see the effect of the image lowering effect, we consider a usual example, a gallium arsenide case, $\epsilon_s = \epsilon_r \epsilon_0 = 13.1 \times 8.85 \times 10^{-14} = 1.16 \times 10^{-12}$ (F/cm). If the first applied electric field, E_1 , is assumed to be 10^5 V/cm, then $x_m = 17$ Å and $e\Delta\phi = 0.03$ eV. On the other hand, if the second applied electric field, E_2 , is 10^7 V/cm, then $x_m = 2$ Å and $e\Delta\phi = 0.3$ eV. Thus, it is obvious that the image lowering effect is greatly reduced at higher electric fields.

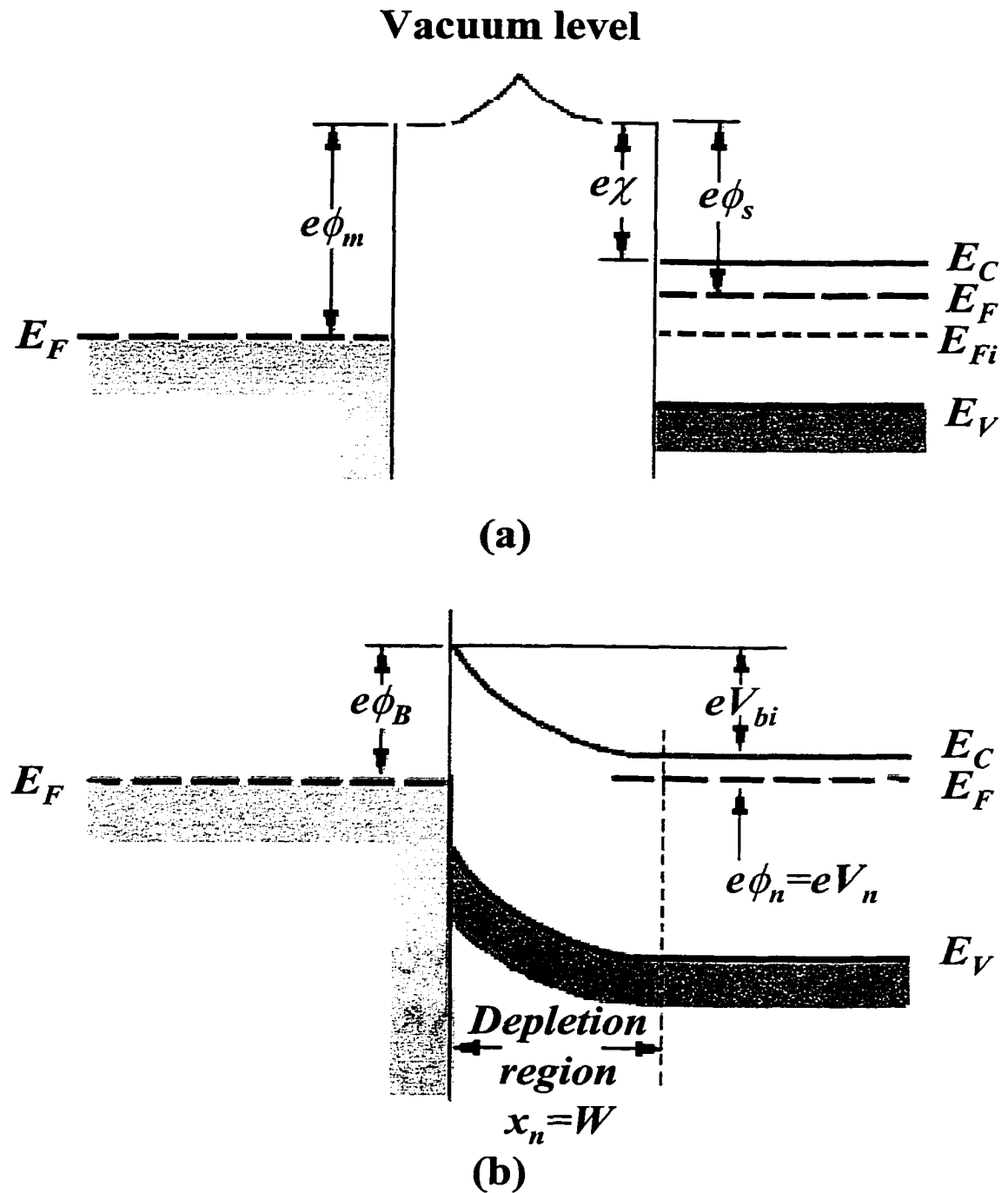


Figure 4.1 (a) Energy band diagram for a metal and n-type semiconductor before contact; (b) Schematic energy band diagram of a metal and n-type metal-semiconductor Schottky junction for $\phi_m > \phi_s$.

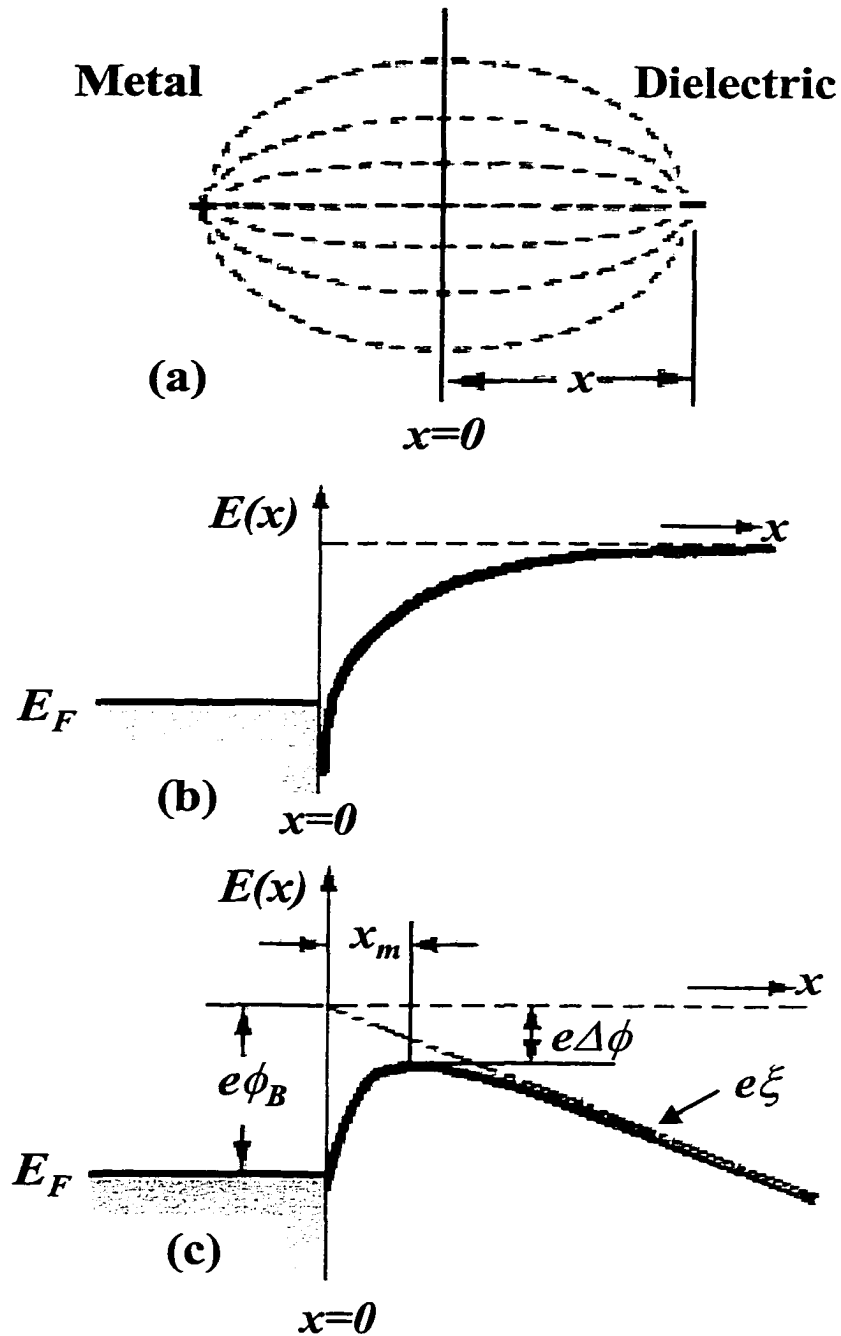


Figure 4.2 (a) image charge and applied electric field lines at a metal-semiconductor Schottky interface; (b) a plot of the potential energy assuming that no other applied electric fields exist; and (c) Schottky effect at the metal-semiconductor Schottky interface in the presence of an applied electric field.

(a) Work functions of some elements

Element		Work Function (Φ_m volts)
Symbol	Name	
Ag	Silver	4.26
Al	Aluminum	4.28
Au	Gold	5.10
Cr	Chromium	4.50
Mo	Molybdenum	4.60
Ni	Nickel	5.15
Pd	Palladium	5.12
Pt	Platinum	5.65
Ti	Titanium	4.33
W	Tungsten	4.55

(b) Electron affinity of some semiconductors

Element		Electron Affinity (χ volts)
Symbol	Name	
Ge	Germanium	4.13
Si	Silicon	4.01
GaAs	Gallium Arsenide	4.07
AlAs	Aluminum Arsenide	3.50

Table 4.1 (a) gives work functions of some elements; and (b) gives electron affinity of some semiconductors.

4.3 Schottky junction – alterable Schottky barrier height

According to above Schottky junction model, the barrier height for an ideal metal-semiconductor Schottky contact is equal to the difference between the work function of a metal, ϕ_m , and the electron affinity, χ_s of a semiconductor. This simple relationship holds only when both the interface states and the image lowering effect are negligible.

The potential and electric field distributions in the space-charge region, and the depletion layer width of a Schottky junction can be derived by solving Poisson's equation using proper boundary conditions. The 1D Poisson's equation in the space-charge region of a Schottky junction is given by

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \quad (4.9)$$

where ϵ_s is the dielectric constant of the semiconductor and $\rho(x)$ is charge density. By integrating above equation, we can obtain the spatial distribution of the electric field. This approach leads to

$$E(x) = -\frac{dV(x)}{dx} = \int \frac{\rho(x)}{\epsilon_s} dx + C_1 \quad (4.10)$$

where C_1 is a constant determined by the boundary conditions. The potential distribution can be obtained by integrating $E(x)$ to yield

$$V(x) = -\int E(x)dx + C_2 = -\iint \frac{\rho(x)}{\epsilon_s} d^2x - C_1x + C_2 \quad (4.11)$$

where C_2 is another constant of integration determined by the boundary conditions.

We will take an example of one-sided abrupt junction approximation to discuss how to alter Schottky barrier height. According to one-sided abrupt junction approximation, the charge density may be expressed as

$$\rho(x) = \begin{cases} eN_D(0 < x < x_n) \\ 0(\text{otherwise}) \end{cases} \quad (4.12)$$

where N_D is doping concentration and x_n is depletion layer width, respectively. The boundary conditions are

$$\begin{cases} V(0) = -\phi_B(x=0) \\ E(x) = -\frac{dV(x)}{dx} = 0(x=x_n) \end{cases} \quad (4.13)$$

where ϕ_B is Schottky barrier height. So the constants C_1 and C_2 are equal to $-\frac{eN_Dx_n}{\epsilon_s}, -\phi_B$, respectively. Finally, we obtain the spatial distributions of electric field and potential inside the depletion region. These are, respectively,

$$E(x) = \left(\frac{eN_D}{\epsilon_s}\right)(x - x_n) \quad (4.14)$$

$$V(x) = -\left(\frac{eN_D}{\epsilon_s}\right)\left(\frac{x^2}{2} - x_nx\right) - \phi_B \quad (4.15)$$

When $x=x_n$, we can obtain depletion layer width as

$$x_n = \sqrt{\frac{2\epsilon_s(V_{bi} - V_a)}{eN_D}} \quad (4.16)$$

where V_{bi} , built-in voltage, is $\phi_m - \phi_s = \phi_B - V_n$, V_a is applied voltage, and V_n , Fermi potential, is $\frac{(E_C - E_F)}{e} = (\frac{k_B T}{e}) \ln(\frac{N_C}{N_D})$. It is seen from above expression that the depletion layer width is directly proportional to the square root of the applied voltage, and is inversely proportional to the square root of the doping density of the semiconductor. Furthermore, the depletion layer width decreases with the square root of the forward bias voltage (i.e., $V_a > 0$), and increase with the square root of the reverse bias voltage (i.e., $V_a < 0$).

Combining the above results and Schottky effect, we can obtain total energy band diagram's expression as follows. The schematic energy band diagram is shown in Figure 4.1 (b).

$$\begin{aligned} E_C(x) &= -eV_n - eV(x) + eV_i(x) = -eV_n + (\frac{e^2 N_D}{\epsilon_s})(\frac{x^2}{2} - x_n x) + \phi_B - \frac{e^2}{16\pi\epsilon_s x} \\ &= \phi_B - eV_n + (\frac{e^2 N_D}{\epsilon_s})(\frac{x^2}{2} - x_n x) - \frac{e^2}{16\pi\epsilon_s x} \end{aligned} \quad (4.17)$$

$$\text{where } x_n = \sqrt{\frac{2\epsilon_s(V_{bi} - V_a)}{eN_D}} \text{ and } V_n = \frac{(E_C - E_F)}{e} = (\frac{k_B T}{e}) \ln(\frac{N_C}{N_D}).$$

Since Schottky effect mainly occurs $x \rightarrow 0 \ll x_n$, then rapidly increase to 0. In order to qualitatively discuss the results of Equation 4.17, we omit the term of $\frac{e^2}{16\pi\epsilon_s x}$ and fix $x=x_n$. Finally, Equation 4.17 can be written as follows.

$$E_C = e\phi_B - eV_n - \left(\frac{e^2 N_D}{2\epsilon_s}\right)x_n^2 = e\phi_B - eV_n - \left(\frac{e^2 N_D}{2\epsilon_s}\right)\left(\frac{2\epsilon_s(V_{bi} - V_a)}{eN_D}\right) = e\phi_B - eV_n - e(V_{bi} - V_a) \quad (4.18)$$

From Equation 4.18, we can obviously see that the Schottky barrier height is altered by applied electric field. In the following sections, we still will continue to detailed discuss this effect.

4.4 Schottky junction – current flow

The basic process of current transport in a metal-semiconductor Schottky junction is by transport of electrons over the potential barrier, which can be described by the thermionic emission theory.

The thermionic emission characteristics are derived using the assumptions that the barrier height is much large than kT , so that the Maxwell-Boltzmann approximation can be applied and thermal equilibrium is not affected by this process. The current $J_{s \rightarrow m}$ is the electron

current density due to the flow of electrons from the semiconductor into the metal, and the current $J_{m \rightarrow s}$ is the electron current density due to the flow of electrons from the metal into the semiconductor. The subscripts of current indicate the direction of electron flow.

The current density $J_{s \rightarrow m}$ is a function of the concentration of electrons which have x-directed velocities sufficient to overcome the barrier. The expression is

$$J_{s \rightarrow m} = e \int_{E_c}^{\infty} v_x dn \quad (4.19)$$

where E_c is the minimum energy required for thermionic emission into the metal, v_x is the carrier velocity in the direction of transport, and e is the magnitude of the electronic charge. The incremental electron concentration is given by

$$dn = g_c(E) f_F(E) dE \quad (4.20)$$

where $g_c(E)$ is the density of states in the conduction band and $f_F(E)$ is the Fermi-Dirac probability function. Assuming that the Maxwell-Boltzmann approximation can be expressed as

$$dn = \frac{4\pi(2m_n^*)^{3/2}}{h^3} \sqrt{E - E_c} \exp\left[-\frac{(E - E_F)}{kT}\right] dE \quad (4.21)$$

If all of the electron energy above E_c is assumed to be kinetic energy, then we can receive

$$\frac{1}{2}m_n^*v^2 = E - E_c \quad (4.22)$$

The net current density in the metal-semiconductor junction can be written as

$$J = J_{s \rightarrow m} - J_{m \rightarrow s} \quad (4.23)$$

which is defined to be positive in the direction from the metal to the semiconductor. We can find the following very important formula.

$$J = [A^* T^2 \exp(\frac{-e\Phi_B}{kT})][\exp(\frac{eVa}{kT}) - 1] \quad (4.24)$$

$$A^* \equiv \frac{4\pi e m_n^* k^2}{h^3}$$

The parameter A^* is called the effective Richardson constant for thermionic emission. V_a is applied voltage. Till now, we receive the current-voltage relationship of a metal-semiconductor Schottky junction. When the alterable Schottky barrier height of the device is changed, we can obtain a set of different current-voltage relationship. This is a simple memory prototype which consists of alterable Schottky junction.

To see the simple model, we consider an example, a silicon case. Assume the Schottky barrier height of Au-Silicon is initially 0.9 eV which corresponds to off-state. When an external voltage (-0.5 V to 0.5 V) applies this device, the Schottky barrier will be modulated to 0.6 eV which corresponds to on-state. The cross-sectional area of the device is 2.5×10^{-3}

(μm^2). The computer calculated results for current-voltage relationship are shown in Figure 4.3. In Figure 4.3, we clearly see the difference between on-state's current and off-state's current is approximately 6 times. The MatLab program is shown in Appendix A.3.

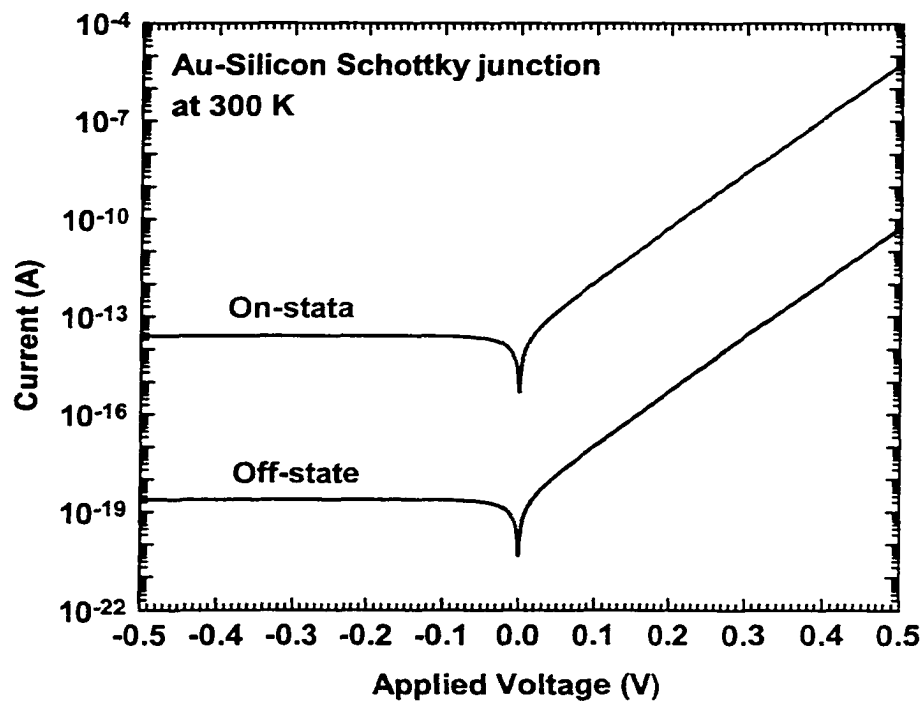


Figure 4.3 shows the on-state/off-state's current-voltage relationship for Au-Silicon Schottky junction.

4.5 Schottky memory cell

As stated above, Schottky memory cell roughly consists of six regions: metal contact, Schottky barrier, electric-field-controlled charge source, carrier (electron/hole) transport, potential quantum well for storing carrier (electron/hole), and n^+ or p^+ -semiconductor substrate.

The Schottky memory cell's key is the reversible carrier (electron/hole) transport between electric-field-controlled charge source and an adjacent potential well (carriers are referred to hereinafter electrons for electron-based semiconductor devices and holes for hole-based semiconductor devices) in a metal-semiconductor Schottky junction. The electric-field-controlled charge source is located near the metal-semiconductor Schottky interface in the junction depletion region. The adjacent quantum well is situated at the end of the depletion region. An electric field is applied reversibly across the depletion region to change the spatial position of the carriers either in the electric-field-controlled charge source or in the adjacent quantum well. The effective Schottky barrier height, which modulates the current flowing, depends on whether the carriers are resided in the electric-field-controlled charge source or in the adjacent quantum well, which corresponds two states of "1" or "0", respectively. Hence, a

two-terminal device contains such a metal-semiconductor Schottky junction can be used to form a memory element. The position of the carriers remains the same and endures unless intentionally moved by the application of a reversed electric field across the depletion region.

The electric-field-controlled charge source can be provided by the following three methods: DX^- centers, a deep heterostructure quantum well, and δ -doping centers.

4.5.1 Electric field distributions in Schottky memory cell

According to above model, charge density of Schottky memory cell will be simplified as shown in Figure 4.4. In order to conveniently discuss its characteristics, assume Schottky memory cell only consists of one semiconductor material. Its dielectric constant is ϵ_s . N_{d1} is the intrinsic doping concentration for the device without external applied field, N_{d2} is the carrier density excited from the electric-field-controlled charge source when an external field applies the device. During each switch, $\alpha\%$ carriers are drifted from electric-field-controlled charge source to adjacent quantum well or from adjacent quantum well to electric-field-controlled charge source, respectively. The alterable Schottky barrier height mainly

occurs in the depletion region $[0, x_n]$. The widths of the electric-field-controlled charge source and the adjacent quantum well are $[a, a_1]$ and $[b, b_1]$, respectively. Although those assumptions do not provide an accurate charge distribution, they at least do provide very reasonable approximate expressions for the electric field distributions and alterable Schottky barrier height.

The charge distribution is as follows.

$$\rho_1(x) = \begin{cases} eN_{d1}(0 < x < x_n) \\ 0(\text{otherwise}) \end{cases}$$

$$\rho_2(x) = \begin{cases} 0(0 < x < a) \\ eN_{d2} \times \alpha\%(a < x < a_1) \\ 0(a_1 < x < b) \\ -eN_{d2} \times \alpha\%(b < x < b_1) \\ 0(\text{otherwise}) \end{cases}$$

$$\rho(x) = \rho_1(x) + \rho_2(x)$$

$$< 0 < a < a_1 < x_n < b < b_1 < +\infty >$$

(4.25)

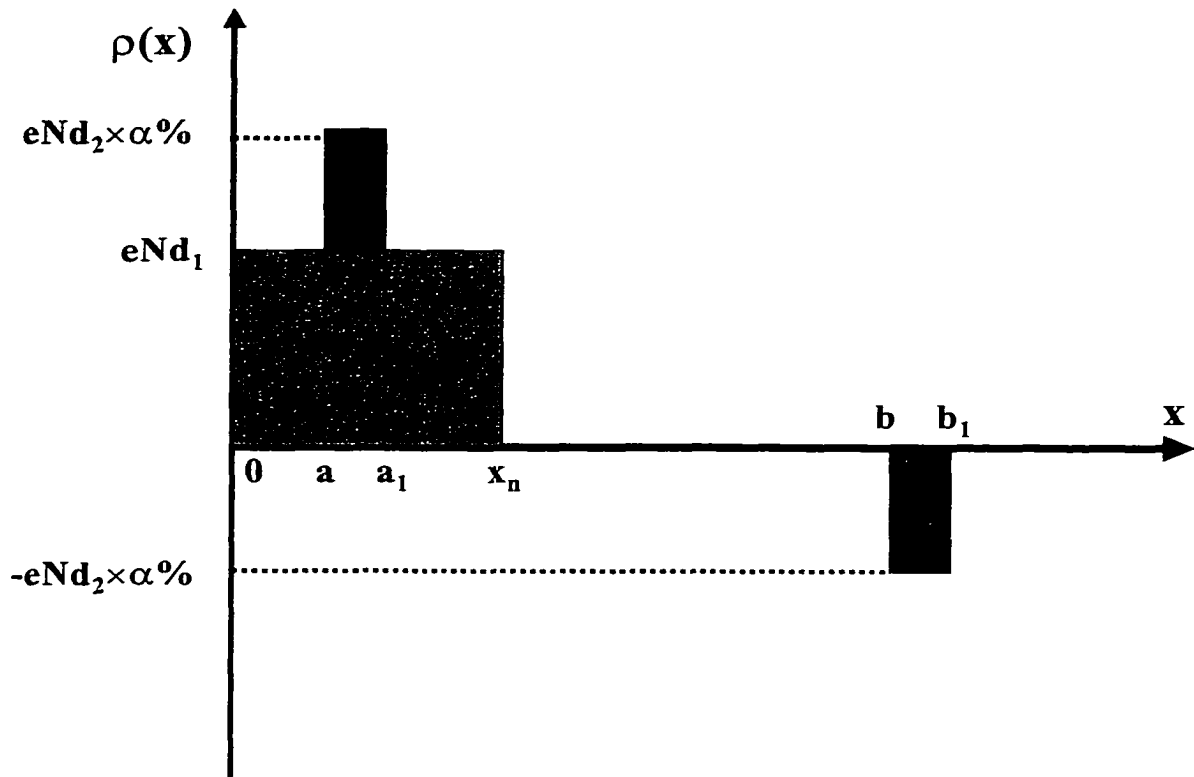


Figure 4.4 shows a simplified mathematics' model which reflects the relationship between space charge distribution ($\rho(x)$) and device's length (x).

The electric field distribution can be received from the Poisson equation

$$\left(\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_s} \Rightarrow E(x) = \int \frac{\rho(x)}{\epsilon_s} dx + C \right).$$

It consists of two parts. The first part is

$$E_1(x) = \begin{cases} \frac{eN_{d1}}{\epsilon_s} (x - x_n) & 0 < x < x_n \\ 0 & \text{otherwise} \end{cases} \quad (4.26)$$

and the second part is

$$E_2(x) = \begin{cases} \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) - \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (a_1 - a) < 0 < x < a > \\ \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (x - a_1) + \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) < a < x < a_1 > \\ \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) < a_1 < x < b > \\ \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - x) < b < x < b_1 > \\ 0 < otherwise > \end{cases} \quad (4.27)$$

Finally, we can receive the total electric field distribution as follows.

$$E(x) = E_1(x) + E_2(x) = \begin{cases} \frac{eN_{d1}}{\epsilon_s} (x - x_n) + \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) - \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (a_1 - a) < 0 < x < a > \\ \frac{eN_{d1}}{\epsilon_s} (x - x_n) + \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (x - a_1) + \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) < a < x < a_1 > \\ \frac{eN_{d1}}{\epsilon_s} (x - x_n) + \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) < a_1 < x < x_n > \\ \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - b) < x_n < x < b > \\ \frac{eN_{d2} \times \alpha\%}{\epsilon_s} (b_1 - x) < b < x < b_1 > \\ 0 < otherwise > \end{cases}$$

< footnote: $0 < a < a_1 < x_n < b < b_1 < +\infty$ >

(4.28)

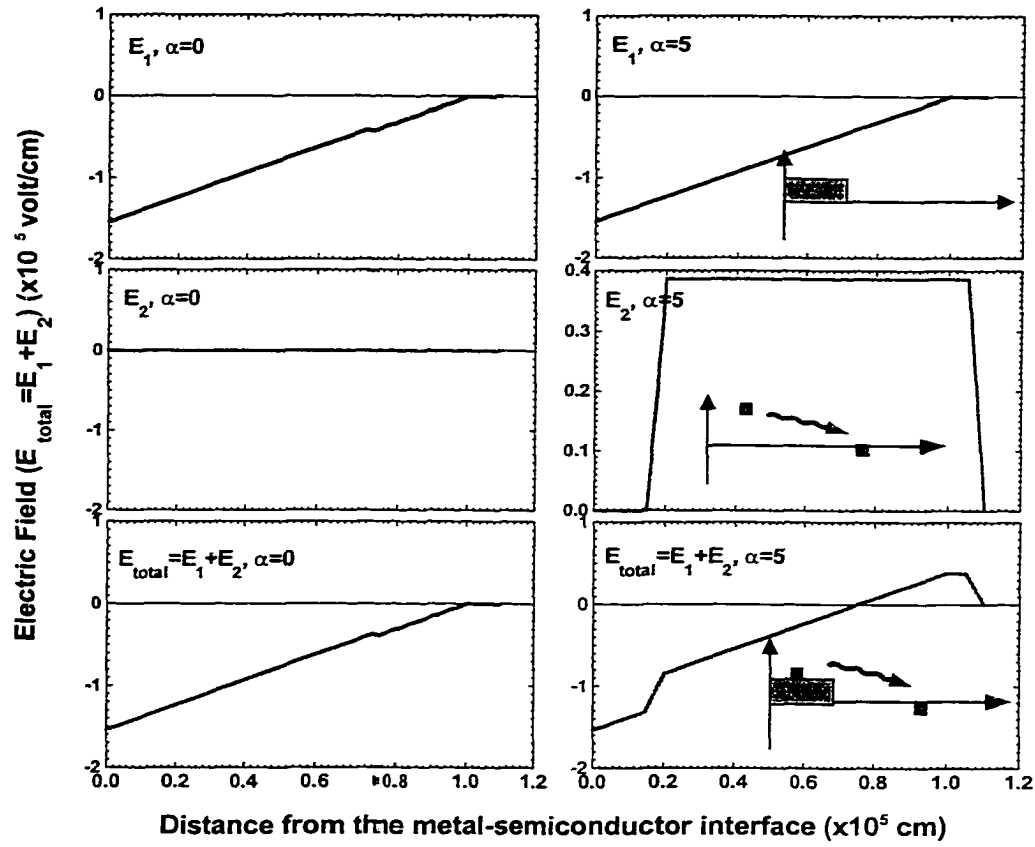


Figure 4.5 shows the electrical field distributions for $\alpha=0$ and $\alpha=5$, respectively.

The above Figure 4.5 shows the electric field distributions for $\alpha=0$ and $\alpha=5$, respectively. The dielectric constant, ϵ_s , is $11.7\epsilon_0$ (Silicon). The value of α determines how many carriers (electrons/holes) are drifted during each switch under the effect of electric field distributions. The detailed MatLab program for electric field distributions is shown in Appendix A.1.

4.5.2 Alterable Schottky barrier height in Schottky memory cell

Alterable Schottky barrier height consists of two parts. One is contributed from charge distributions and the other is from image charges. The charge distributions are shown in Equation 4.25. The energy band diagram can be expressed as

$$E_C(x) = V_n + \Phi_{\rho(x)}(x) - \frac{e}{16\pi\epsilon_s x} \quad (\text{eV})$$

(4.29)

The potential energy, $\Phi_{\rho(x)}(x)$, can be again found by integrating the electric field distributions as $\Phi_{\rho(x)}(x) = -\int E(x)dx + C$ (eV). The electric field distribution, $E(x)$, is shown in Equation 4.28. So we can receive the potential energy as follows.

$$\Phi_{\rho(x)}(x) = \begin{cases} (I): -\frac{eN_{d1}}{2\epsilon_s}(x-x_n)^2 - \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(b_1-b)x + \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(a_1-a)x + C_1 < 0 < x < a > \\ (II): -\frac{eN_{d1}}{2\epsilon_s}(x-x_n)^2 - \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(x-a_1)^2 - \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(b_1-b)x + C_2 < a < x < a_1 > \\ (III): -\frac{eN_{d1}}{2\epsilon_s}(x-x_n)^2 - \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(b_1-b)x + C_3 < a_1 < x < x_n > \\ (IV): -\frac{eN_{d2} \times \alpha\%}{\epsilon_s}(b_1-b)x + C_4 < x_n < x < b > \\ (V): \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(x-b_1)^2 + C_5 < b < x < b_1 > \end{cases} \quad (4.30)$$

The following problem is how to determine the constants $[C_1, C_2, C_3, C_4, C_5]$. Because the charge distribution, $\rho(x)$, are not uniform, it is totally divided into five regions according to our model. When carriers (electrons/holes) are drifted between electric-field-controlled charge source and adjacent quantum well due to electric field's effect, the potential energy diagram will appear bent. If the minimum point, $x_{\min}$, lies in the different regions, respectively, we can receive five sets of different constants $[C_1, C_2, C_3, C_4, C_5]$ as shown in Equations 4.31 – 4.35. The value of $x_{\min}$ can be determined by assuming total electric field $E(x_{\min})=0$ as shown in Equation 4.28.

Region I: $x_{\min} \in [0, a]$

$$\left\{ \begin{array}{l} C_1 = \frac{eN_{d1}}{2\epsilon_s}(x_{\min} - x_n)^2 + \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(b_1 - b)x_{\min} - \frac{eN_{d2} \times \alpha\%}{\epsilon_s}(a_1 - a)x_{\min} \\ C_2 = C_1 + \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(a_1^2 - a^2) \\ C_3 = C_1 + \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(a_1^2 - a^2) \\ C_4 = C_1 + \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(a_1^2 - a^2) \\ C_5 = C_1 + \frac{eN_{d2} \times \alpha\%}{2\epsilon_s}(a_1^2 - a^2 + b^2 - b_1^2) \end{array} \right. \quad (4.31)$$

Region II: $x_{\min} \in [a, a_1]$

$$\left\{ \begin{array}{l} C_1 = C_2 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (a^2 - a_1^2) \\ C_2 = \frac{eN_{d1}}{2\varepsilon_s} (x_{\min} - x_n)^2 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (x_{\min} - a_1)^2 + \frac{eN_{d2} \times \alpha\%}{\varepsilon_s} (b_1 - b)x_{\min} \\ C_3 = C_2 \\ C_4 = C_2 \\ C_5 = C_2 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b^2 - b_1^2) \end{array} \right. \quad (4.32)$$

Region III: $x_{\min} \in [a_1, x_n]$

$$\left\{ \begin{array}{l} C_1 = C_3 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (a^2 - a_1^2) \\ C_2 = C_3 \\ C_3 = \frac{eN_{d1}}{2\varepsilon_s} (x_{\min} - x_n)^2 + \frac{eN_{d2} \times \alpha\%}{\varepsilon_s} (b_1 - b)x_{\min} \\ C_4 = C_3 \\ C_5 = C_3 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b^2 - b_1^2) \end{array} \right. \quad (4.33)$$

Region IV: $x_{\min} \in [x_n, b]$

$$\left\{ \begin{array}{l} C_1 = C_4 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (a^2 - a_1^2) \\ C_2 = C_4 \\ C_3 = C_4 \\ C_4 = \frac{eN_{d2} \times \alpha\%}{\varepsilon_s} (b_1 - b)x_{\min} \\ C_5 = C_4 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b^2 - b_1^2) \end{array} \right. \quad (4.34)$$

Region V: $x_{\min} \in [b, b_1]$

$$\left\{ \begin{array}{l} C_1 = C_5 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b_1^2 - b^2 + a^2 - a_1^2) \\ C_2 = C_5 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b_1^2 - b^2) \\ C_3 = C_5 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b_1^2 - b^2) \\ C_4 = C_5 + \frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (b_1^2 - b^2) \\ C_5 = -\frac{eN_{d2} \times \alpha\%}{2\varepsilon_s} (x_{\min} - b_1)^2 \end{array} \right. \quad (4.35)$$

When $x=0$, from Equation 4.30, we can receive alterable Schottky barrier height, Φ_B' , as shown in Equation 4.36.

$$\begin{aligned} \Phi_B' &= V_n + abs\left(-\frac{eN_{d1}}{2\varepsilon_s} x_n^2 + C_1\right) \\ V_n &= V_t \ln\left(\frac{N_c}{N_{d1}}\right) \end{aligned} \quad (4.36)$$

Figure 4.6 shows computer calculated results. when $\alpha=0$ (off-state) and 5 (on-state), we receive the alterable Schottky barrier heights, Φ_B' , for the off-state and on-state, are equal to 0.92 eV and 0.65 eV, respectively. The dielectric constant, ε_s , is $11.7\varepsilon_0$ (Silicon). In the region ($x \rightarrow 0$), an obvious Schottky barrier lowering's effect is observed. The detailed MatLab program for alterable Schottky barrier height is shown in Appendix A.2.

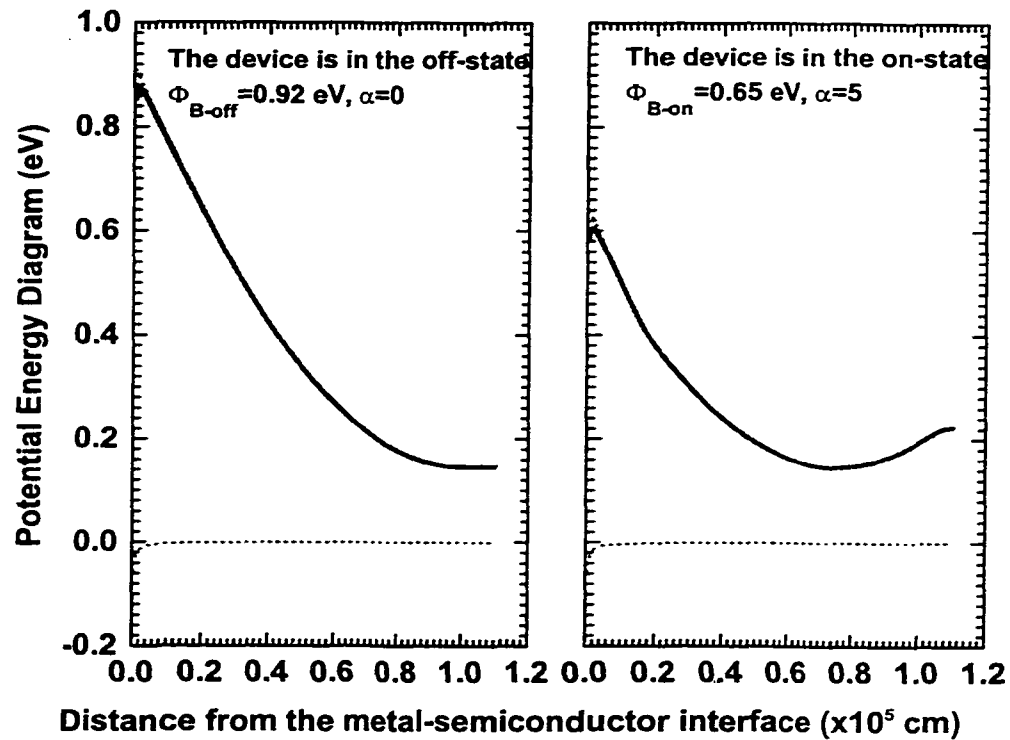


Figure 4.6 shows the computer calculated results. An obvious 'Schottky barrier lowering' effect is discovered.

4.5.3 Current flow in Schottky memory cell

Since the basic process in SCM model is by transport of carriers (electrons/holes) over the alterable Schottky barrier, the alterable Schottky barrier is a key component of SCM device, we think that the thermionic emission model, which usually predicts the carrier transport in a metal-semiconductor Schottky barrier diode, fully can illustrate the current flow

in SCM device. Hence, we can apply Equation 4.24 to reflect the current-voltage (I-V) relationship of our SCM device. The case of hole flow is opposite to electron flow.

When the device is in the on-/off-state, the alterable Schottky barrier height, Φ_{B-on}/Φ_{B-off} , can be obtained from above Section 4.5.2. The computer calculated results and discussions are shown in Figure 4.12 and Section 4.7, respectively, and MatLab program is shown in Appendix A.3.

4.6 DX⁻-centers used as electric-field-controlled charge source

Here, the DX⁻ charge centers will be taken an example of the electric-field-controlled charge source to explain SCM operation's principle in this Section. Their experimental results, 1D Poisson-Schrödinger simulation results, and further investigations will be detailed explained in the following chapters.

The schematic energy band diagram of the SCM is shown in Figure 4.7. The total SCM device consists of six regions: metal contact, Schottky barrier, electron transport, electron potential quantum well, hetero-interface barrier, and n⁺-semiconductor substrate. The reverse current (negative bias with respect to the substrate) is small since the image

lowering effect on the Schottky barrier height is negligible for ionized donor densities on the order of 10^{14} to 10^{15} cm^{-3} (unintentionally doped II-VI or III-V semiconductors). The forward current can be designed to be small by introducing a hetero-interface barrier near the interface of region 4 and 5. Therefore, both reverse and forward currents in off-state are small for a given probing voltage region (e.g., within ± 1 volt). The SCM device is in a non-conductive state as shown in Figure 4.7(a).

To electrically turn a SCM device on from the off-state, we first discuss how one can electrically control the Schottky barrier height that is an energy barrier for injecting electrons from a metal contact to an adjacent semiconductor. A simplified expression for the image lowering potential energy is given as follows¹

$$q\Delta\Phi = C[N_d^+ (\text{in } 10^{14} \text{ cm}^{-3}) (V_b - V_a) (\text{in volts})]^{1/n} (\text{meV}) \quad (4.37)$$

where C is the constant related with semiconductor materials, N_d^+ is the ionized donor density, V_b is the built-in potential, V_a is the applied bias (negative under reverse bias), and the value of n depends on the assumption used for the space charge distribution (4 for an one-sided abrupt junction approximation). It is known that the reverse current of a Schottky diode at a given temperature is exponentially dependent on the effective barrier height, $q\Phi_{\text{eff}} = q\Phi_b - q\Delta\Phi$. The ingenuity of the proposed

SCM device is to make use of the tunable nature of a Schottky barrier height through the image lowering effect. As shown in the Equation 4.37, the value of $q\Delta\Phi$ can be turned on when $N_d^+ \neq 0$ and be turned off when $N_d^+ \approx 0$. The electric-field-controlled charge centers (for example, DX centers²) are useful for this application. They provide an electric-field-controlled source of ionized donors. When a critical reverse bias (e.g., V_r) is applied, two electrons for each DX center ($DX^- \Leftrightarrow D^0 + e^- \Leftrightarrow D^+ + 2e^-$) near the metal-semiconductor interface will be emitted to the conduction band and will drift away from this interface leaving behind a large number of normal ionized donors. The condition of $N_d^+ \gg 0$ holds. This results in a large image lowering effect on the barrier height of the Schottky contact as shown in Figure 4.7(b).

To turn the device on from the off-state, we can apply a negative bias slightly large than $|V_n|$ (dc or pulse) so that electrons located near the metal-semiconductor interface will be emitted to the conduction band and drift towards an adjacent quantum well through the electron transport region and be confined there. As a result of this charge transport, both reverse and forward current will be increased. The increase of the reverse current is due to a smaller effective Schottky barrier height, $q\Phi_{\text{eff}}$, caused by the image lowering effect when a large equivalent ionized donor density

exists near the metal-semiconductor Schottky interface. The forward current increase is due to a resonant tunneling current enhancement arising from the confined electrons in the adjacent quantum well. It should be emphasized that the novelty of the proposed SCM device manifests itself from the fact that the electric-field-controlled electron emission from the DX centers causes an increase of not only the reverse current but also the forward current.

To turn the device off from the on-state, a critical positive bias V_p is required to release the electrons confined in the adjacent quantum well. These electrons will be swept back to the metal-semiconductor interface and be captured by the ionized DX centers when the electron energy exceeds the capture energy barrier, E_{ca} , as shown in Figure 4.7.

Either on-state or off-state is sustainable even when the external power is removed. For the on-state, the electrons left from the metal-semiconductor interface are confined in the adjacent quantum well. The device will stay in the on-state as long as electrons remain confined. For the off-state, the electrons are released from the potential well and be captured by the charge centers near the metal-semiconductor interface. The device will stay in the off-state as long as the probing voltage is less than $|V_n|$, i.e., $|eV_n| < E_{em}$ (emission barrier height) as shown in Figure 4.7.

The detailed experimental results, 1D Poisson-Schrödinger simulation results, and further investigations will be explained in the following chapters.

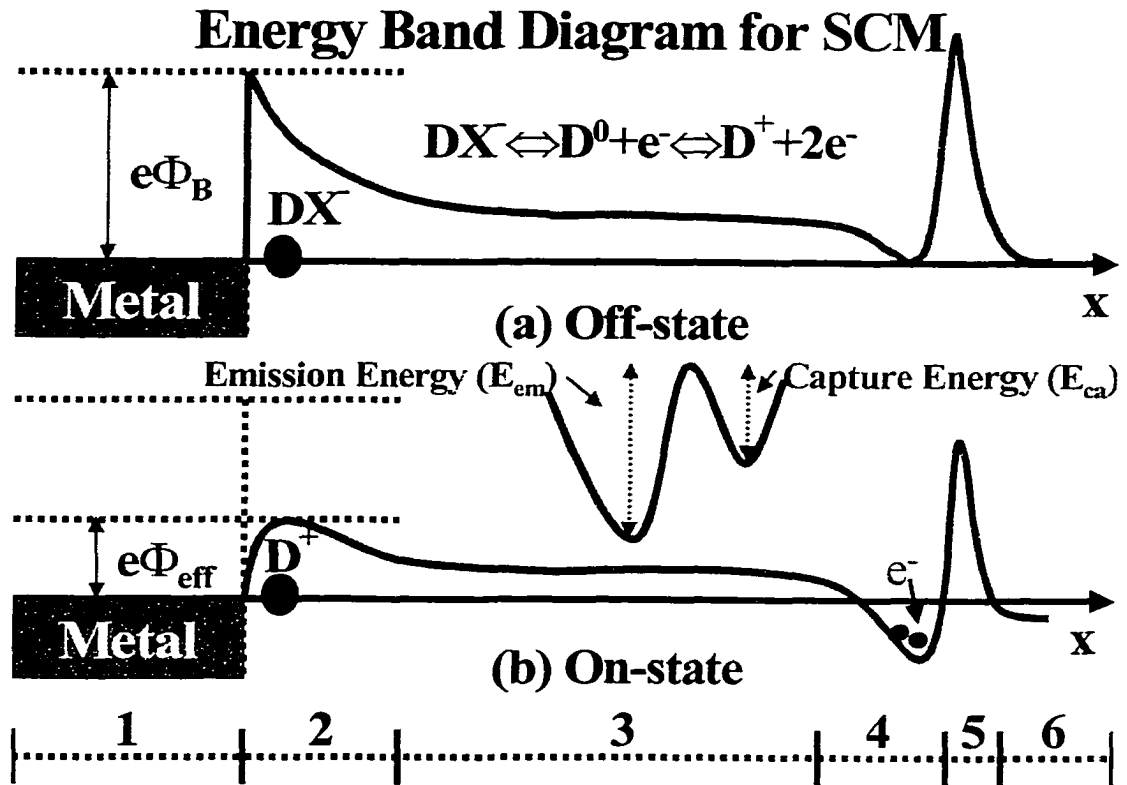


Figure 4.7 Schematic energy band diagrams for the SCM. The SCM device consists of six regions: 1. metal contact; 2. Schottky barrier; 3. electron transport region; 4. an adjacent quantum well; 5. hetero-interface barrier; and 6. n^+ -semiconductor substrate. Both (a) off-state and (b) on-state for the SCM device correspond to “1” and “0” of stored data, respectively. The inset in (a) shows a reversible process for a DX^- center. The inset in (b) shows an energy diagram of a DX^- center.

4.7 Heterostructure quantum well used as electric-field-controlled charge source

In the Section, we will mainly discuss the other case, which the electric-field-controlled charge source is provided by a p-type or n-type heterostructure quantum well, respectively. Their device structures roughly are the same as DX-center case. The difference is that a heterostructure quantum well will be used to act as DX centers disclosed before.

The following one preferred structure is a memory element comprising two deep p-type SiGe quantum well on a p-type Si substrate. The structure is compatible with conventional silicon processing for integration with other microelectronic elements on the same silicon substrate. The further detailed descriptions with reference to the accompanying drawings are as follows.

Figure 4.8 —Figure 4.12 enable us to clearly understand the mechanism of our NVM model. Figure 4.8 is a cross-sectional illustration of a p-type SiGe memory device with two electrodes A and B. The gate electrode A is a metal layer that contains an adjacent semiconductor structure forming an Schottky junction and the other electrode B is attached to the bottom of the p^+ -Si substrate. Between the electrodes A and

B is the layered semiconductor structure, Si (20 nm, $N_a=1\times10^{17} \text{ cm}^{-3}$) / $\text{Si}_{1-x}\text{Ge}_x$ ($x=0.6$, 5 nm, $N_a=4.5\times10^{18} \text{ cm}^{-3}$) / Si (115 nm, $N_a=1\times10^{17} \text{ cm}^{-3}$) / $\text{Si}_{1-x}\text{Ge}_x$ (5 nm, $N_a=1\times10^{17} \text{ cm}^{-3}$) / Si (10 nm, intrinsic layer) / Si (10 nm, $N_a=1\times10^{17} \text{ cm}^{-3}$) / Si (100 nm, $N_a=1\times10^{18} \text{ cm}^{-3}$) / p^+ -Si substrate, that consists of the SiGe quantum well A and the SiGe quantum well B. Between the two quantum wells is a field region (Si <115 nm, $N_a=1\times10^{17} \text{ cm}^{-3}$) with the electric field strength depending on the charge densities in the two SiGe quantum wells A and B.

Figure 4.9A displays the calculated electric field (E_i) in the Schottky junction depletion region when the quantum well A and B are not charged. When a positive electric pulse is applied to the gate electrode A, the holes confined in the SiGe quantum well A are electrically excited. Part of holes will be drifted into SiGe the quantum well B during the pulse period and remain there until they are being excited by another pulse. The SiGe quantum well A is now negatively charged because of the deficiency of holes while the SiGe quantum well B is positively charged due to the excess of holes. The density changes for holes in the SiGe quantum well A and B are shown in Figure 4.10. The electric field component (E_{ind}) induced by the holes transfer from the SiGe quantum well A to B is shown in Figure 4.9B. This electric field has an opposite sign in comparison with

the field E_1 displayed in Figure 4.9A. The addition of the normal electric field E_1 and the induced electric field E_{ind} due to the external excitation results in a new electric field distribution (E_2) in the Schottky depletion region, which is shown in Figure 4.9C. It can be also stated mathematically that $E_2 = E_1 + E_{ind}$. Depending on the value of $E_{ind} = 0$ or $\neq 0$, there exists a binary electric field distribution either E_1 or E_2 in the Schottky depletion region. Since the band bending in the depletion region is directly related to the electric field distribution, the band diagram of the memory device should also reflect this binary characteristics. Figure 4.11A and 4.11B display the valence band diagrams of the memory device by applying 1D Poisson-Schrödinger solver. The valence band diagrams correspond to the electric field distribution of E_1 and E_2 , respectively. The two SiGe quantum wells A and B are also shown with eigen energy levels for heavy holes. The dash line indicates the Fermi level of the device at equilibrium. The most important parameter shown in the diagrams is the value of valence band edge at the metal-semiconductor interface, Schottky barrier height (Φ_B), since it dictates the current flow over the metal-semiconductor junction. For $E_{ind} = 0$, $\Phi_B = 0.6$ eV and for $E_{ind} \neq 0$, $\Phi_B = 0.4$ eV. The room temperature current-voltage (I-V) characteristics of the memory device in Figure 4.8 described above are shown in Figure 4.12. The I-V curve bb'

corresponds to the off-state when $E_{ind}=0$ while the curve CC' is for the on-state when $E_{ind}\neq 0$. It clearly shows four orders of magnitude in current between on-state and off-state when the memory device is probed in a voltage range of -0.5 V to $+0.5$ V. The on-/off-state remains unchanged until E_{ind} is changed by an external voltage pulse. The switching time between on-state and off-state is expected to be on an order of picosecond since only mobile carriers are involved.

InGaAs/GaAs is considered as another semiconductor material system to form n-type deep quantum wells on an n-type GaAs substrate. Figure 4.13 shows the second memory structure. The two deep quantum well A and B are formed due to large conduction band offset between InGaAs and GaAs. Figure 4.14A and 4.14B display the on-/off-state conduction band diagrams, respectively. This structure uses InGaAs/GaAs based material system which is compatible with GaAs electronic devices such as GaAs junction field-effect transistors and bipolar transistors.

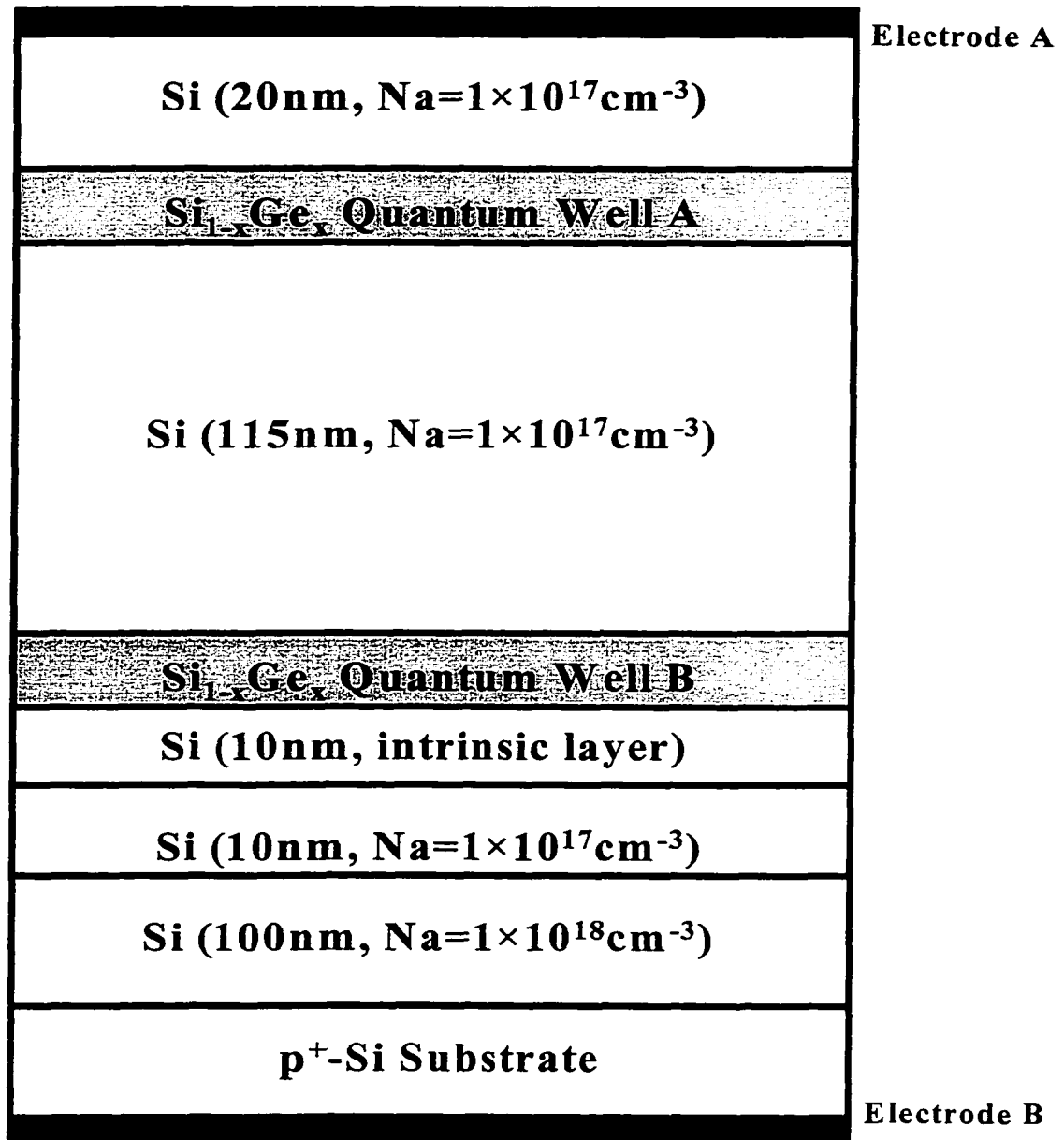


Figure 4.8: Schematic cross-sectional representation of p-type SiGe structure.

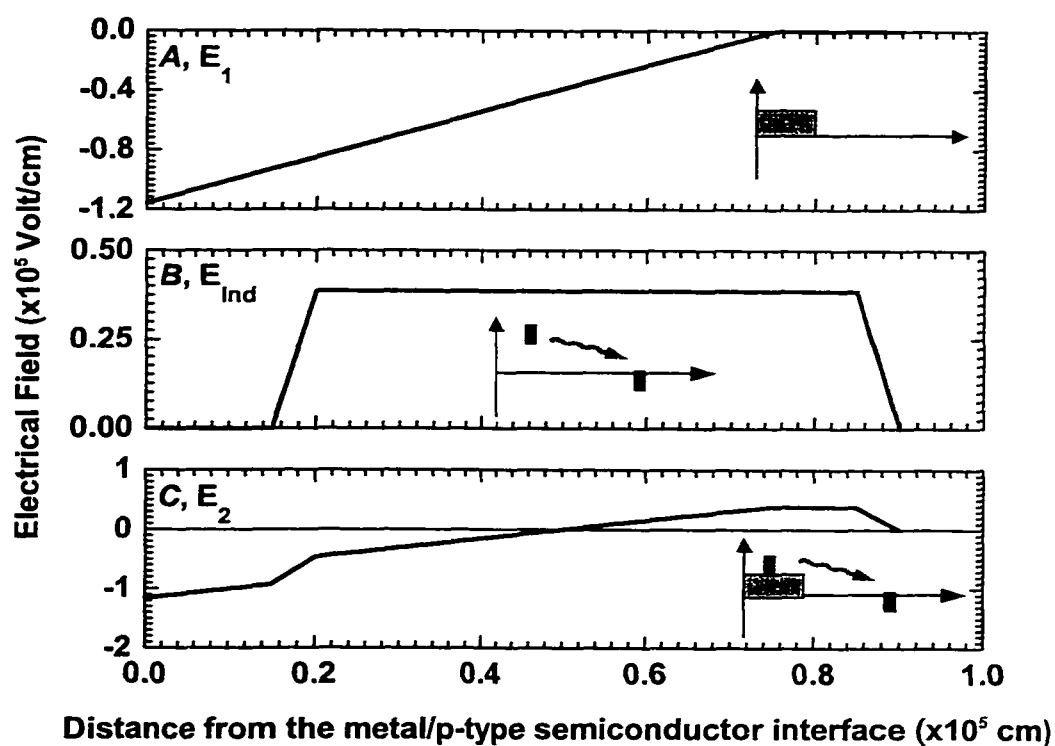


Figure 4.9A displays the calculated electric fields in the Schottky junction depletion region when no electrical excitation voltage pulse is applied; the memory device is in the off-state, Figure 4.9B shows the electric field induced by hole transport from the quantum well A to the quantum well B, and Figure 4.9C gives the electric field in the depletion region when the device is electrically excited (written) by a suitable voltage pulse; the memory device is in the on-state.

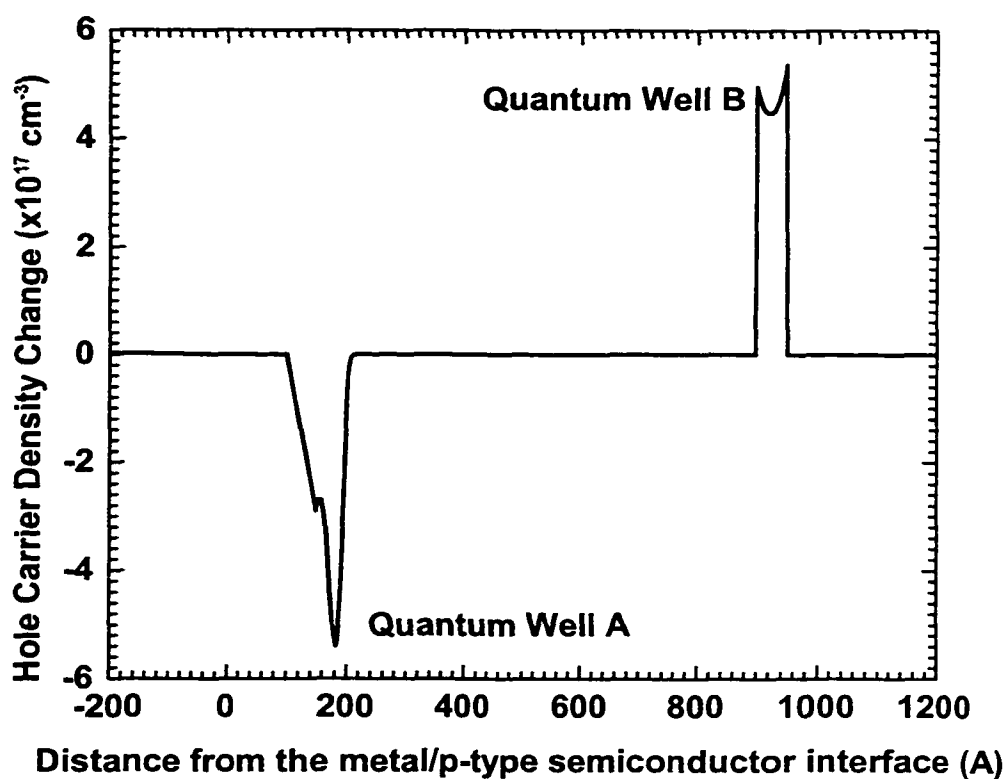


Figure 4.10 shows carrier density change after the device is electrically excited by an applied voltage pulse that force the carriers in the first well A to be drifted to the second well B. It can be seen that the deficit of carriers in the well A and the access carriers in the well B.

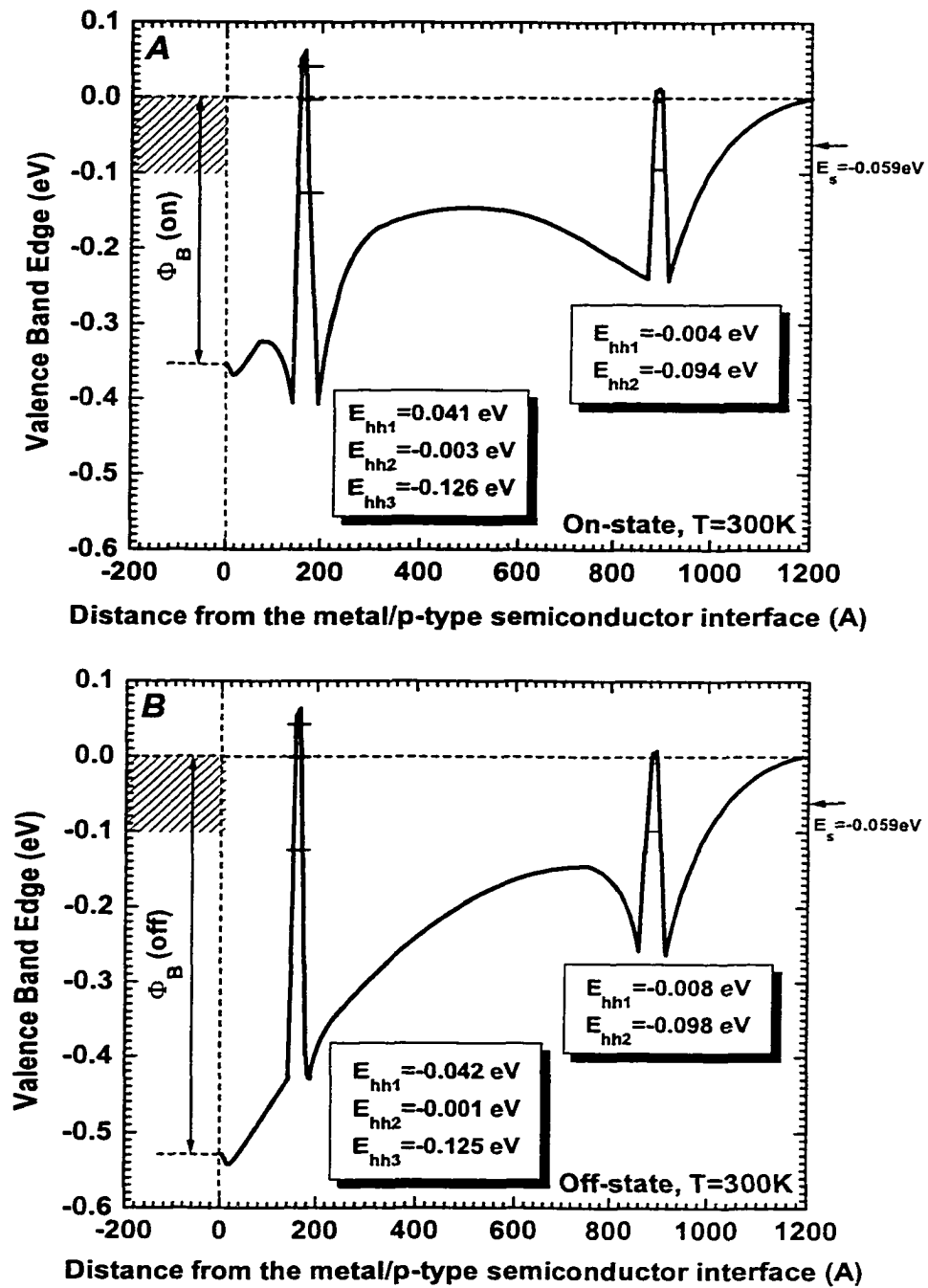


Figure 4.11A displays schematically the valence band edge (potential energy for holes), E_v , of the p-type SiGe at the on-state, and Figure 4.11B is the E_v at the off-state.

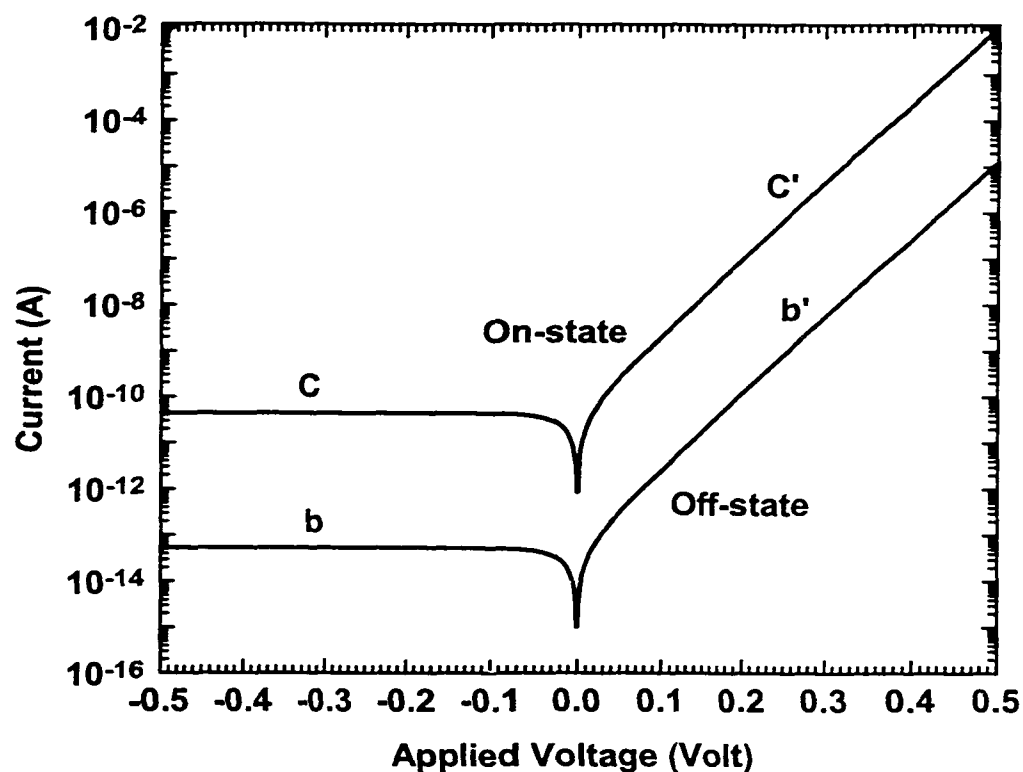


Figure 4.12 shows the room temperature current-voltage characteristics of the p-type SiGe memory device at both on-state and off-state. There are four orders of magnitude difference in current between the on-state and off-state.

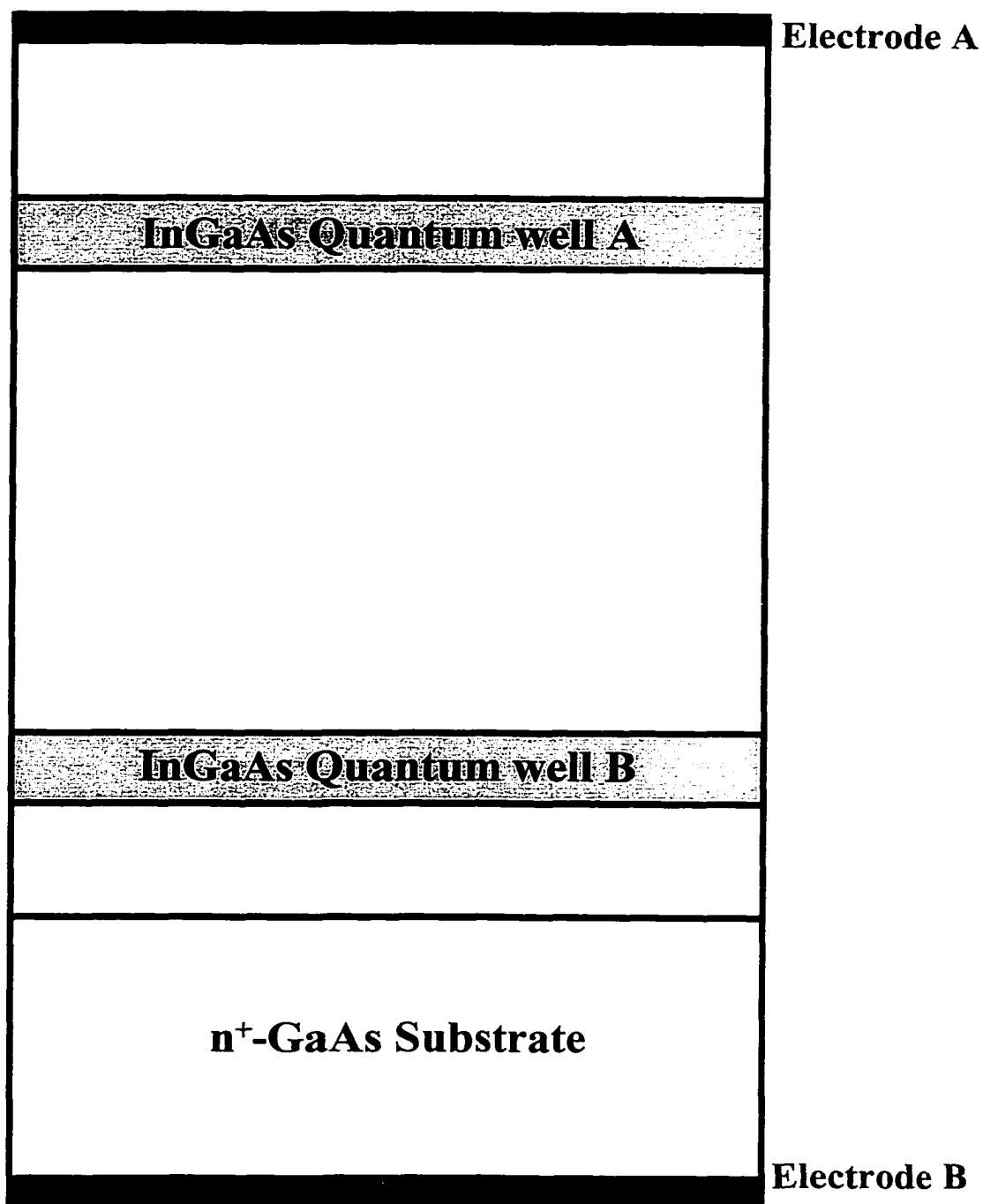


Figure 4.13: Schematic cross-sectional representation of the third structure using InGaAs quantum wells on the n^+ -GaAs substrate.

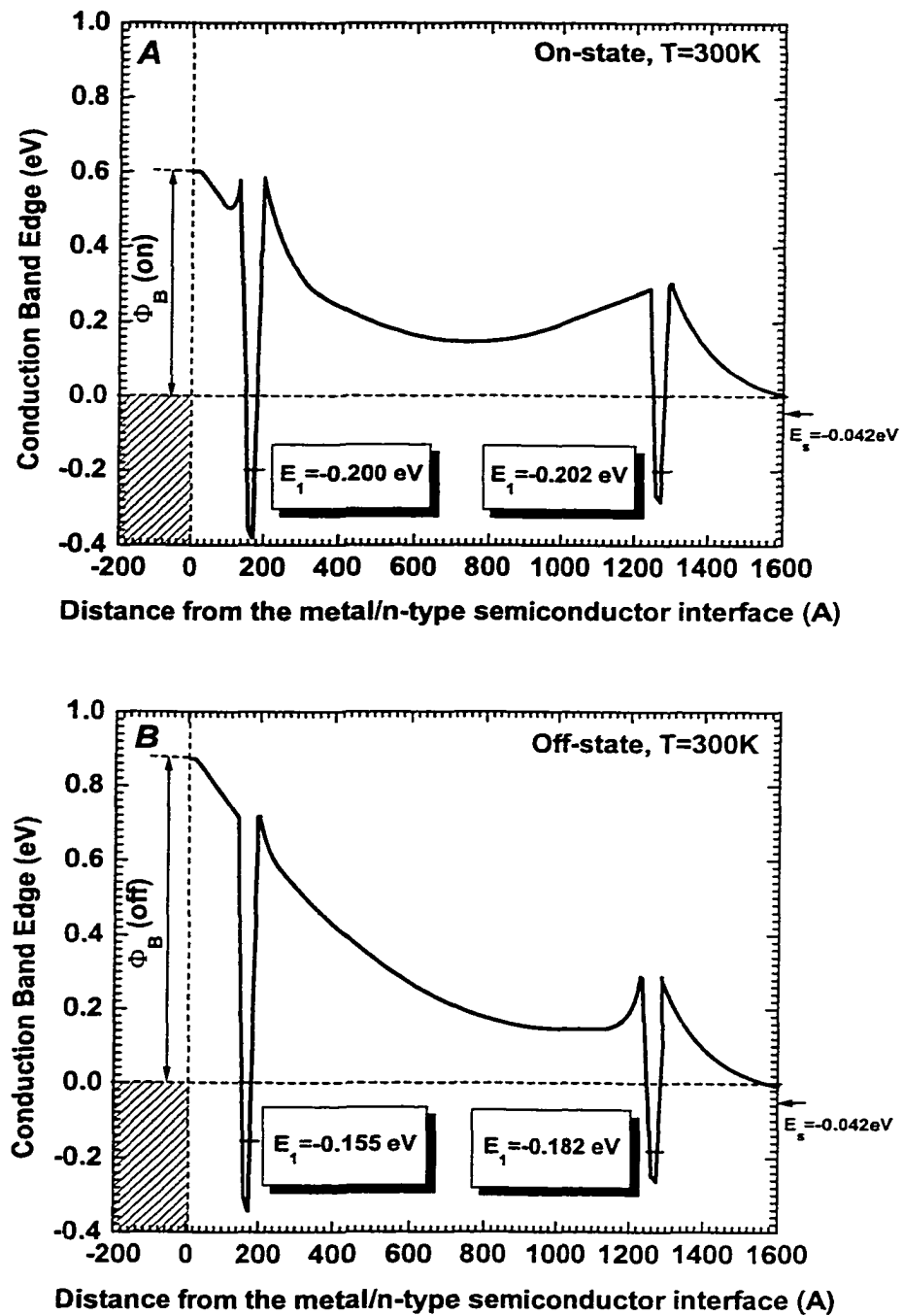


Figure 4.14A is the conduction band edge, E_c , for the structure in Figure 4.11 at the on-state, Figure 4.14B is the E_c for the structure in Figure 4.11 at the off-state.

4.8 δ -doping quantum well used as electric-field-controlled charge source

The Schottky memory cell model is not limited to the above SiGe and InGaAs structures. δ -doping as another means to form deep quantum wells in the Schottky depletion region. Figure 4.15 shows the third memory structure. The structure differs from the former in that the quantum well A and B are formed by n-type δ -doping instead of using SiGe and InGaAs alloys. The n^+ -Si substrate is used for this structure which is fully compatible with silicon electronic devices. The conduction band diagrams for on-/off-state are shown in Figure 4.16A and 4.16B, respectively.

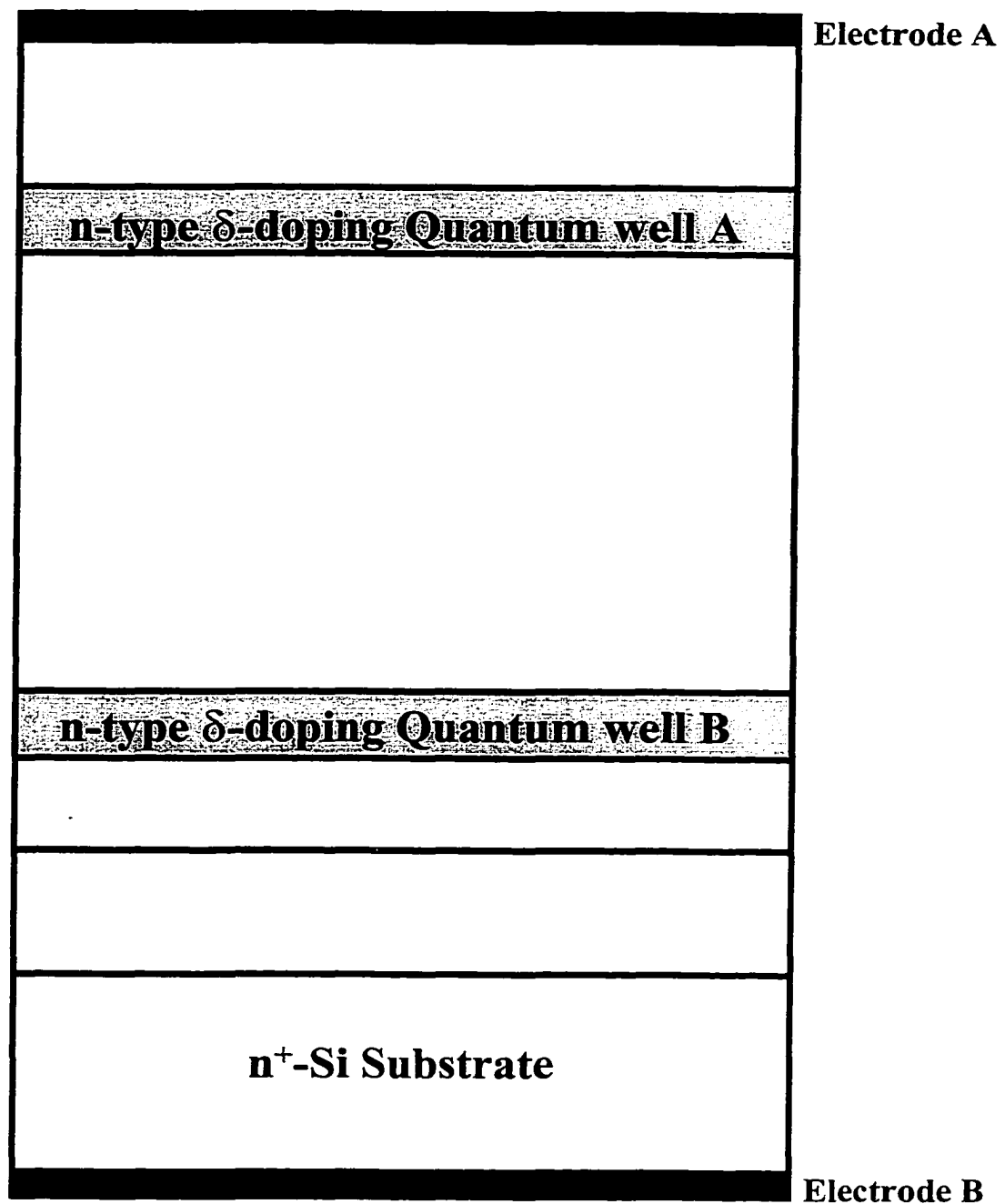


Figure 4.15: Schematic cross-sectional representation of n-type δ -doped quantum wells on the n^+ -Si substrate.

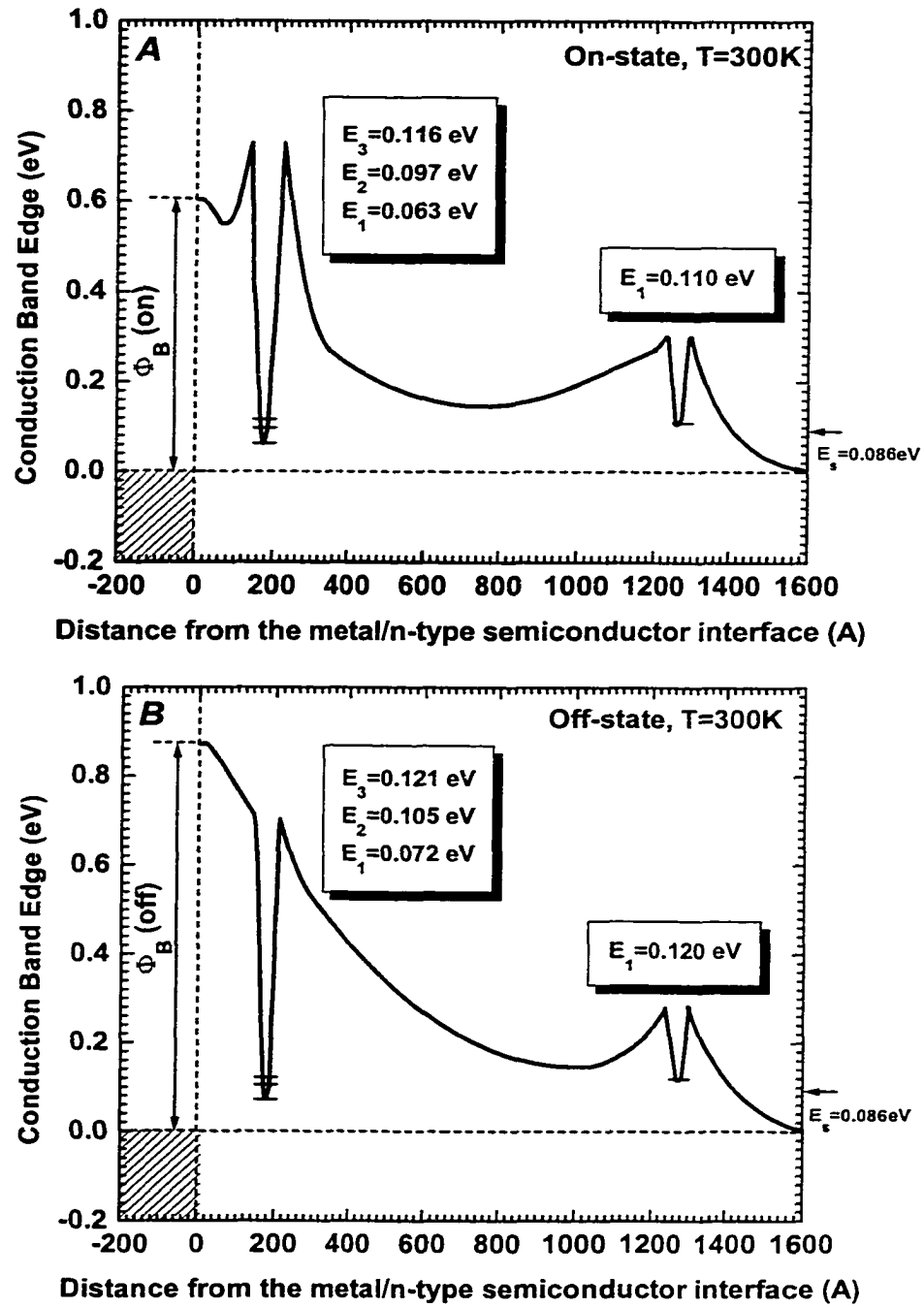


Figure 4.16A is the conduction band edge, E_c , for the structure in Figure 4.11 at the on-state, Figure 4.13B is the E_c for the structure in Figure 4.11 at the off-state.

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CHAPTER 5

Material Growth and Device Fabrication

Our II/VI and III/V SCM devices were grown by molecular beam epitaxy (MBE) technology. In this Section, we will take an example of our II-VI Al/ZnCdSe/ZnCdMgSe/ZnCdSe/InP (buffer layer)/n⁺-InP (substrate) SCM device to briefly introduce the device growth process by applying MBE technology.¹

5.1 MBE principle

The MBE process² achieves epitaxial growth in an ultra-high vacuum (UHV) environment through the chemical reaction of one or more thermal molecular beams with a crystalline surface of the substrate. This process is illustrated schematically in Figure 5.1 which shows the essential components necessary for MBE growth of II/VI Al/ZnCdSe SCM device. All these components are in a UHV environment. Molecular beams are provided by thermal Knudsen effusion cells. Each cell contains a crucible which in turn contains one of the constituent chemical elements or

compounds of the desired epilayer. The temperature of each cell is chosen so that the vapor pressures of the materials are sufficiently high for generation of thermal energy molecular beams by free evaporation. The cells are arranged so that the central portion of the beam flux distribution from each cell intersects the substrate. Each cell has a shutter between the cell and the substrate. Operation of these shutters permits abrupt cessation or initiation of any given beam flux to the substrate. By choosing the appropriate cell through the opening of its shutter and the appropriate substrate temperature, epitaxial films of the desired chemical components can be obtained. The extremely high precision in beam flux control allows the growth of very thin layers, even mono-layers. This distinguishing characteristics has enabled MBE to become one of the main growth technologies for heterostructures including quantum wells and superlattices. While the UHV environment allows the growth of very pure materials, it is also ideal for in-situ analytical instrumentation. In Figure 5.1, the in-situ reflection high energy electron diffraction (RHEED) technique is shown, which is a powerful technique to monitor the growth process.

Molecular Beam Epitaxy (MBE)

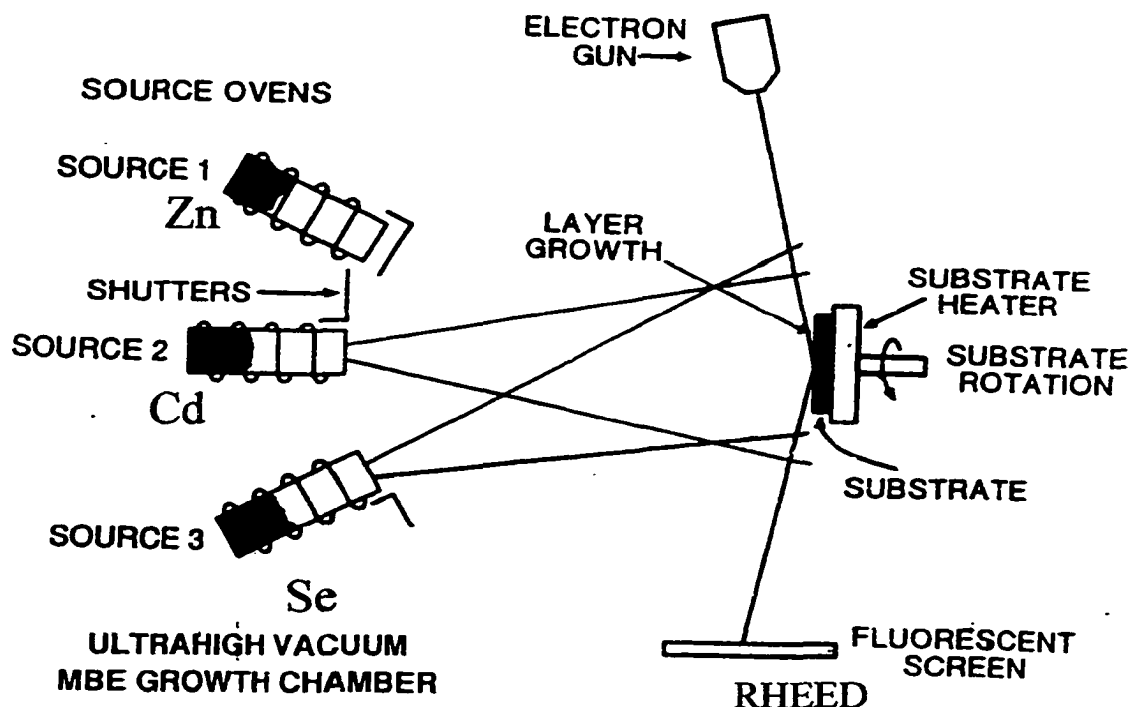


Figure 5.1 shows the illustration of MBE process

5.2 MBE system

Our II-VI SCM devices in this dissertation were done in a Riber 2300P MBE system in Professor Tamargo's laboratory, Chemistry Department, CCNY/CUNY. Figure 5.2 shows the schematic of the top-view of the system. The system includes 6 chambers: loading chamber, transfer channel, substrate treatment chamber, metallization chamber, and two growth chambers. Chamber 1 is for III-V materials and chamber 2 for II-

VI materials. There are several gate valves to separate all the chambers to insure that unintentional cross contamination between them does not occur. In order to avoid contamination and achieve ultra-high vacuum, all the chambers are pumped by an ion-pump and a Ti sublimation pump except the loading chamber which is pumped by a turbo-molecular pump with a mechanical pump as the first stage and the substrate treatment chamber which is pumped by a cryo-pump. Besides the ion pump, the II-VI chamber and the metallization chamber are each pumped by an additional cryo-pump. The loading chamber is used for loading substrates. There is a gate valve between the loading chamber and the other chambers which allows us to vent the loading chamber by using ultra pure nitrogen gas to load substrates and not affect the vacuum in other chambers. This allows the vacuum in the other chambers to remain in the range of 10^{-10} Torr. The substrates or samples can be transferred within the system through the transfer channel. The substrate treatment chamber is used to out-gas the substrates before transferring them to the growth chamber. The metallization chamber is equipped with an e-beam evaporator, which can deposit metal layers in situ on the sample to fabricate a device.

The chambers for the growth of III-V and II-VI semiconductor materials are similar. Each is equipped with a substrate manipulator

(holder, rotator, heater and temperature sensor of the substrates), RHEED, quadrupole mass spectrometer, and cryo-shrouds around the manipulator and the cells. These cryo-shrouds will have a flow of liquid nitrogen (LN) through them during growth to prevent the thermal interference between the sources and also trap the residual molecules inside the chamber to obtain UHV vacuum. There are 8 cells in the III-V chamber equipped for Ga, In, Al, Mn, As, InP (for P flux), Si (for n-type doping) and Be (for p-type doping), and 8 cells in the II-VI chamber for Zn, Cd, Mg, Se, Te, CdTe, ZnCl_2 (for Cl flux used for n-type doping) and a radio frequency (RF) nitrogen cell for p-type doping. Very high purity materials from 6N to 8N have been used as the source materials to ensure high purity films are grown. Each time new sources were charged, the temperatures of all the sources were elevated to at least 100°C (except Se and ZnCl_2 , whose temperature is 80°C and 60°C , respectively) without introducing LN in the cryo-shrouds for ~ 6 hours to roughly outgas the source materials. Then the sources were elevated to a temperature 20°C higher than the temperature required during the growth, with the LN cooling of the chamber, for ~ 6 hours to insure the source materials were thoroughly out-gassed before the actual growth took place. All the pyrolytic boron nitride (PBN) crucibles used in the chambers were out-gassed in the transferring

channel or substrate treatment chamber by heating to $\sim 1200^{\circ}\text{C}$ for ~ 24 hours before they were used.

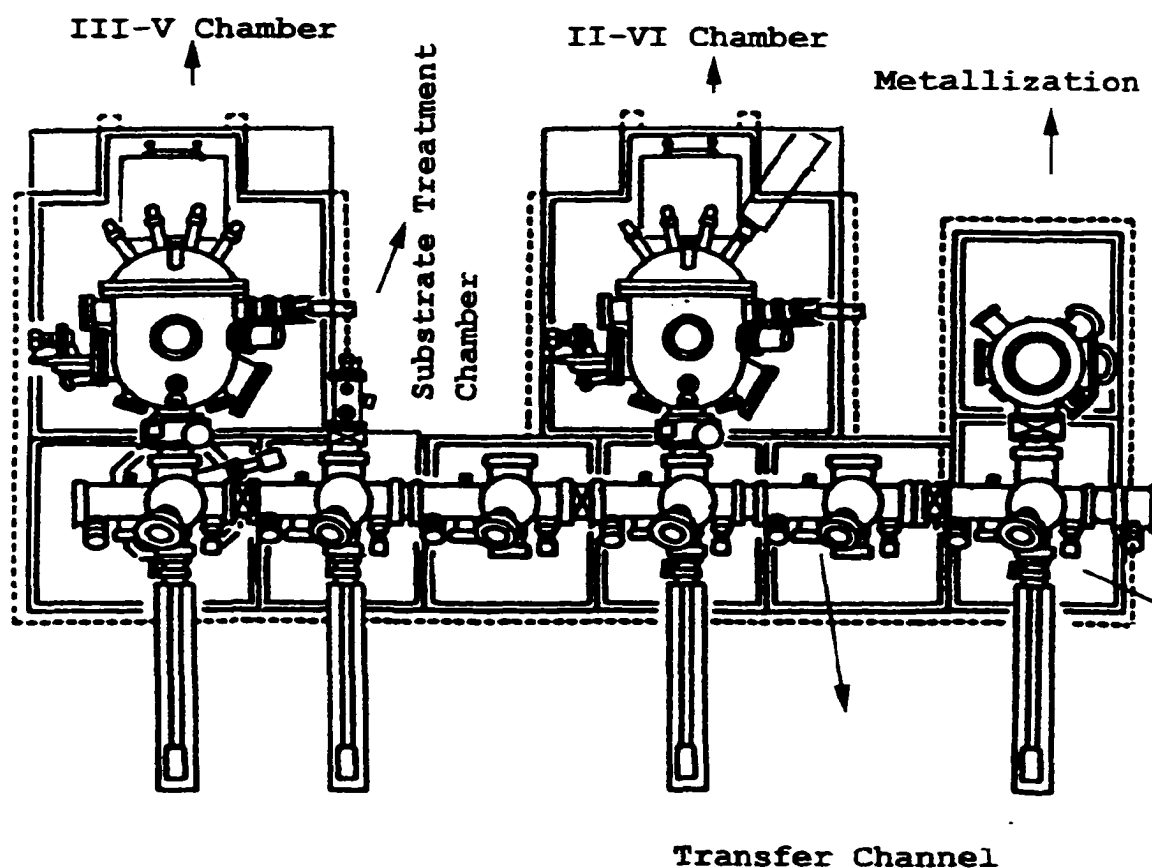


Figure 5.2 shows the top view of the MBE system

5.3 Growth procedure of MBE

InP (100) substrates from Sumitomo Electric, having defect density of $\sim 10^3 \text{ cm}^{-2}$, were used in our II-VI SCM devices. Prior to use, the substrates were degreased by using trichloroethylene (TCE), acetone and methanol

and etched in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (4:1:1) for 1 minute to remove the residual polishing damage. Then an oxide layer was formed on the surface by flushing the wafers with deionized water to protect the fresh InP surface from contamination of carbon. The wafers were then In-bonded onto a Mo block to load into the loading chamber in the MBE system. The loading chamber was first pumped by an oil-free mechanical pump, then it was pumped by two sorption pumps to $\sim 10^{-3}$ Torr. After that, the turbo-pump system was opened and the loading chamber was pumped down very quickly to 10^{-8} Torr. The substrates were transferred to the substrate treatment chamber to out-gas at 150°C for 20 min. The oxide desorption of the substrate was performed in the III-V chamber by heating the substrate with an As flux impinging on the InP surface. After the growth of the III-V buffer layer, the substrate was transferred very quickly to the II-VI chamber to start the growth of II-VI layer. The contamination or damage during the transfer is expected not to be severe.³

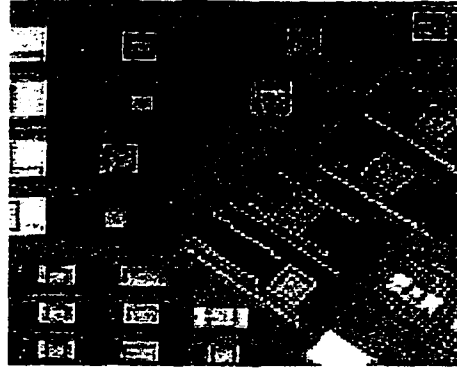
5.4 Device fabrication

Since SCM devices are fabricated on a whole semiconductor wafer by MBE, each one must be divided and packaged individually. After each

device is separated, it is attached to a package by using sliver glue. Connections are made between the SCM device and package using a tool called a wire bonder. There are a number of ways to perform wire bonding. Our facilities are capable of using ultrasonic bonding technology using very thin thread made of gold to make the electrical connections as shown in Figure 5.3 (a). Other ways include thermo-compression bonding and thermo-sonic bonding. Schottky junctions were fabricated by depositing round-shaped Al or Au with a thickness of about 3000 Å and a diameter of approximately 2 mm using a high vacuum e-beam evaporator through a mask onto the device's epilayer. We selected a very popular and inexpensive side brazed package, also known as Dual-In-Line-Package (DIP) as shown in Figure 5.3 (b), as device holder. There is an even number of pins on each side of the package, with leads extending passed the package to plug into a socket. Other packages still include cladded Pin-Grid Arrays (PGAs), Leadless Chip Carriers (LCCs), and Surface Mounted packages.



(a)



(b)

Figure 5.3 (a) the cross-sectional illustration of bonding SCM device; (b) a series of productions for side brazed packages also known as Dual-In-Line -Packages (DIPs)

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CHAPTER 6

II-VI Semiconductor Based on Schottky Cell Memory

6.1 II-VI semiconductor materials

– **Al/ZnCdSe/ZnCdMgSe/ZnCdSe/InP/n⁺-InP**

To demonstrate the our SCM concept, we has grown more than 100 hetero-structure devices fabricated using 15 different wafers with different $\text{Zn}_{1-x-y}\text{Cd}_x\text{Mg}_y\text{Se}(t)/\text{InP}(t_b)$ epilayer structures grown on n^+ -InP substrates by molecular beam epitaxy (MBE). Detailed structure is shown in Figure 6.1. Both ZnCdMgSe and InP layers were intentionally undoped. The layer thickness of ZnCdMgSe(t) was measured by grooving the sample with a Philtec sectioner and the thickness of InP(t_b) is estimated by the growth rate. The values for x and y were determined from the single crystal x-ray diffraction.¹ Schottky diodes were fabricated by depositing round-shaped Al contacts with a thickness of 300 nm and a diameter ranging from 0.5-2 mm using a high vacuum evaporator through a mask onto the ZnCdMgSe

epilayers. Individual diodes were then cleaved from the wafers and bonded to device holders for current-voltage (I-V) measurements. The I-V data were taken in the dark by a computerized HP4142B source/monitor unit.

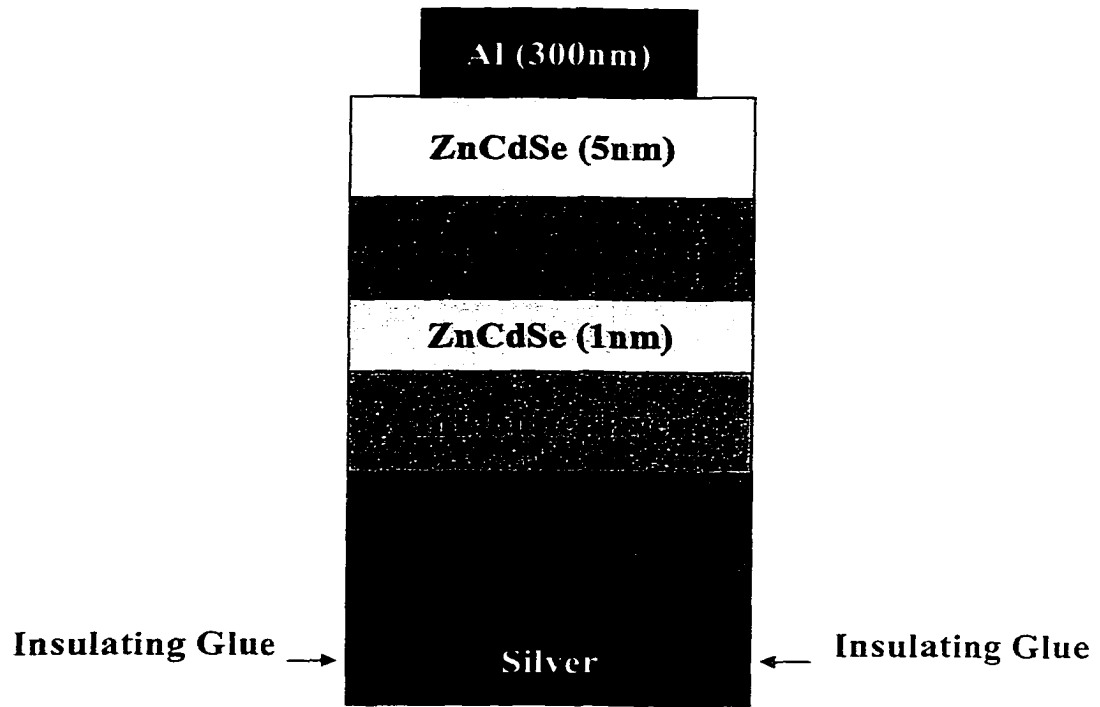


Figure 6.1 Cross-section of Al/ $\text{Zn}_{1-x-y}\text{Cd}_x\text{Mg}_y\text{Se}$ /InP/ $\text{n}^+\text{-InP}$.

6.2 I-V characteristics

The room temperature I-V data taken from a device fabricated from one wafer (A575) are displayed in Figure 6.1.² The device layer structure is Al(300 nm)/ZnCdSe (5 nm)/ZnCdMgSe(0.75 μm)/ZnCdSe(1 nm)/InP(200

nm buffer layer)/n⁺-InP (substrate). The applied bias starts at -1.5 V and increases towards 1.5 V. The device is initially in the on-state (low resistance state). When the applied bias reaches slightly over 1 V, the current sharply jumps to a current value less than 1 nA. The device has made a transition from on-state to off-state (high resistance state). Moving continuously from ~1-1.5 V, the device stays at the off-state. The device remains at the off-state when the applied bias changes its moving direction from 1.5 toward -1.5 V. At about -1.5 V, the device switches back to the on-state. In the on-state, a strong negative differential resistance (NDR) under forward bias was observed and in the reverse bias region the device behaves as a leaky Schottky diode in Figure 6.2. The on-state current is three orders greater than the off-state current.

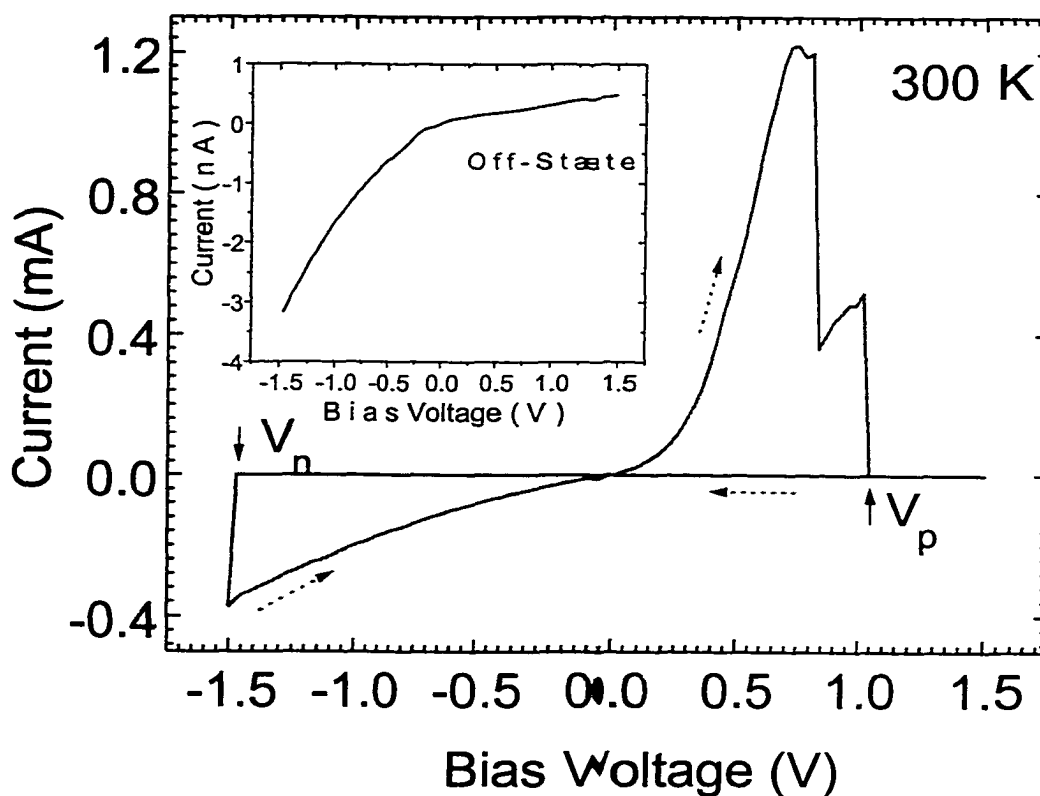


Figure 6.2 I-V curve of the Al(300 nm)/ZnCdSe(5 nm)/ZnCdMgSe(0.75 μm)/ZnCdSe(1 nm)/InP(200 nm)/ n^+ -InP device in the dark at room temperature.

This I-V hysteresis can be repeated many times. The device can stay either in the on- or off-state even when the applied bias is removed. The value of the current at 0.75 V is 1.218 mA for the on-state and 0.242 nA for the off-state. This remarkable current difference between the on- and off-state with a ratio of 5 million at a given applied bias gives us a real demonstration that our proposed SCM principle is possible to be developed

a new NVM technology. The value of V_n at which the device makes a transition from the off-state to the on-state is in a range of -1.2–2.5 V and the value of V_p at which the device makes a transition from the on-state to the off-state is in a range of 0.45-2 V. Both V_p and V_n depend on the detailed structure parameters and device temperature. It should be pointed out that the Al atoms may diffuse into ZnCdMgSe and form DX centers there.

6.3 Transient switching characteristics

Transient switching experiments have been carried out to measure the speed of on-to-off and off-to-on switching. A narrow electrical pulse with a width of ~100 ns was applied to the II-VI SCM device that is in series with a normal resistor. The device voltage $[V_d(t)]$ was measured as a function of time using a LeCroy digital oscilloscope. Figure 6.3 shows transient switching profiles for on-to-off (solid-curve) and off-to-on (dot-curve) switching in the dark at room temperature.² The value for V_n and V_p indicated in the figure is consistent with that measured in the dc case. A resolution limited short switching time of less than 100 ns was measured for the off-to-on transition. For the on-to-off transition, the switching time

is about 100 ns. The longer transition time for the on-to-off state transition might be limited by the large device size.

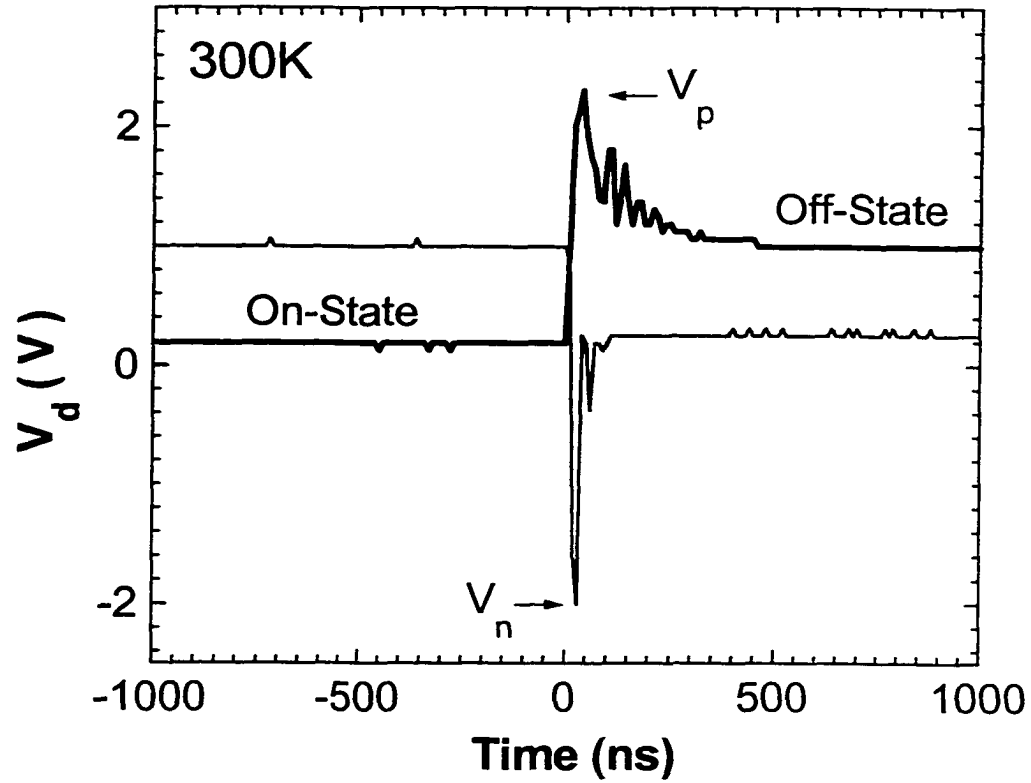


Figure 6.3 Transient switching profiles measured in the dark at room temperature for Al(300 nm)/ZnCdSe(5 nm)/ZnCdMgSe(0.75 μ m)/ZnCdSe (1 nm)/InP(200 nm buffer layer)/n⁺-InP(substrate). The black curve is for the on-to-off switching while the red curve is for the off-to-on switching.

Although the number of on-to-off and off-to-on repetitions can be theoretically infinite for our SCM device, the endurance for the current

devices has not yet been fully characterized. For the limited data, we have found it is much easier to continuously repeat the I-V hysteresis for devices having smaller V_n and V_p values. Figure 6.4 displays the continuously recorded I-V hysteresis (± 1 V, current limit 5 mA) in a sequence of 1 to 6 at room temperature from another SCM device (D5) fabricated from the A326 wafer with the device layer structure of Al(300 nm)/ZnCdSe(1100 μm)/InP (100 μm buffer layer)/ n^+ -InP (substrate). The variation of V_p is from 0.30 to 0.34 V while the variation of V_n is from -0.25 to -0.44 V for up to the 5th repetition. At the 6th repetition, the value of V_p exceeds the prefixed measurement limit of -1 V resulting in the termination of hysteresis.

In conclusion, we have proposed the SCM concept for NVM and presented a proof-of-concept demonstration using II-VI $\text{Zn}_x\text{Cd}_y\text{Mg}_{(1-x-y)}\text{Se}$ semiconductor materials grown on n^+ -InP substrates. This study shows that it is feasible to fabricate a new class of NVM cells based on our SCM principle.

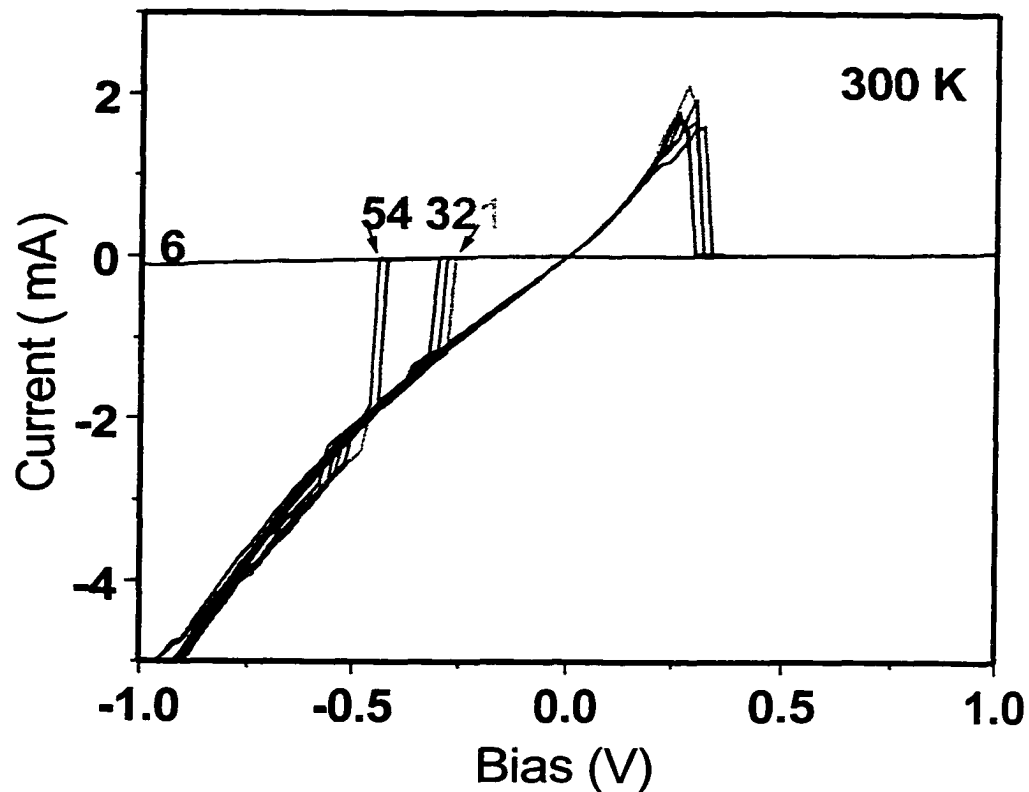


Figure 6.4 Continuously recorded I-V curves in a sequence of 1-6 for the Al(300 nm)/ZnCdSe(1100 μm)/InP(100 μm buffer layer)/ n^+ -InP (substrate).

6.4 Tunneling effect through a parabolic barrier¹¹

Electrons can penetrate potential barriers if these barriers are thin and low enough, as pointed out by Oppenheimer, Fowler and Nordheim. This quantum-mechanical phenomenon can easily be understood by recognizing that the wave function of an electron cannot immediately stop at a barrier,

but rather decreases exponentially into the barrier with a slope determined by the barrier height. If the barrier is thin, there is a non-zero amplitude of the wave function remaining at the end of the barrier. This phenomenon is called electron tunneling.

A parabolic barrier is better suited as an approximation for barriers in which two fields overlap. The parabolic barrier type is shown in Figure 6.5. The transmission probability T_e for a wide class of barriers is given in the WKB approximation by

$$T_e \cong \exp \left\{ - \int_0^a |k(x)| dx \right\}$$

(6.1)

The corresponding wave vector is given by

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}} \sqrt{\frac{(\Delta E)^2 - (eFx)^2}{\Delta E}} \quad (6.2)$$

[* General parabolic equation is $E(x) = -Ax^2 + B$ as shown in Figure 6.5. when $x=0$, there is no external electric field, so $E(0) = \Delta E$. So we can receive the parabolic equation $E(x) = -Ax^2 + \Delta E$. According to the same reason, when $x=a$, since the total $E(a) = 0$, that is to say, $\Delta E = eFx|_{x=a}$, we can get $a = \frac{\Delta E}{eF}$. And, $E(a) = 0 = -A\left(\frac{\Delta E}{eF}\right)^2 + \Delta E \Rightarrow A = \frac{(eF)^2}{\Delta E}$. Finally, we obtain

its parabolic equation and corresponding wave vector are

$$E(x) = -\frac{(eF)^2}{\Delta E} x^2 + \Delta E, k(x) = \sqrt{\frac{2m^* E(x)}{\hbar^2}} = \sqrt{\frac{2m^*}{\hbar^2} \frac{(\Delta E)^2 - (eFx)^2}{\Delta E}}, \text{ respectively.}]$$

After integration, we can receive

$$\int_0^a |k(x)| dx = \frac{\pi}{2} \sqrt{\frac{2m^*}{\hbar^2}} \frac{(\Delta E)^{3/2}}{eF} \quad (6.3)$$

Therefore, the transmission probability for a parabolic barrier is given by

$$T_e = \exp \left\{ -\frac{\pi}{2} \sqrt{\frac{2m^*}{\hbar^2}} \frac{(\Delta E)^{3/2}}{eF} \right\} \quad (6.4)$$

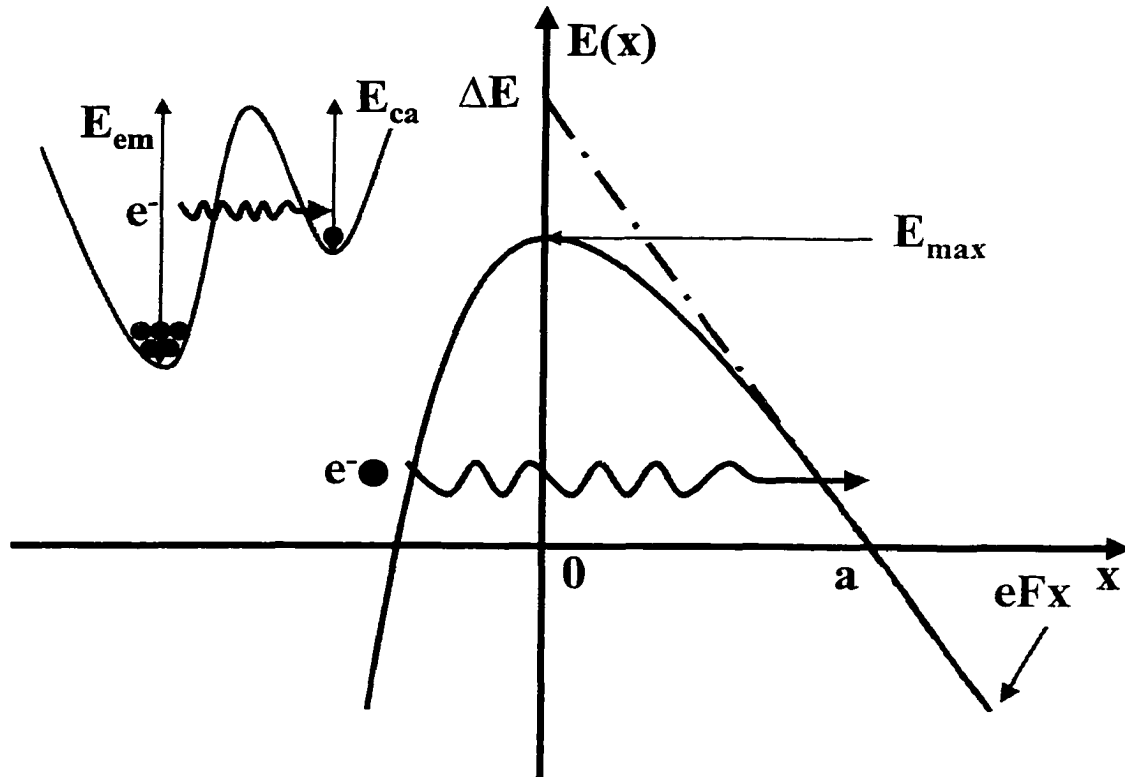


Figure 6.5: Schematic parabolic barrier in which an energy diagram of a deep-level charge center and an external field are overlapped.

6.5 C-V study of deep centers (DX centers) in II-VI

Al/Zn_xCd_{1-x}Se Schottky diodes

Since Goodman³ presented the first comprehensive descriptions of the metal semiconductor properties in terms of the capacitance-voltage (C-V) relationship, the characteristics of a metal-semiconductor Schottky barrier diode has been of interest.⁴⁻⁹ According to ideal Schottky theory ($\frac{1}{C^2} = \frac{2(V_{bi} + V)}{e\epsilon_s N_d}$), The projection to where $\frac{1}{C^2} = 0$ yields built-in voltage V_{bi} and the slop is inversely proportional to N_d . However, our experimental $\frac{1}{C^2} - V$ relationships of new type II-VI Al/Zn_xCd_{1-x}Se Schottky diodes are nonlinear as shown in Figure 6.6 and are not in good agreement with this theory, they appeared bent after -0.4 V reserve bias. In this section, we propose an “electric-field-enhanced tunneling” model to analyze our experimental results and further unveil its intrinsic origin and mechanism of electric-field-controlled charge centers.

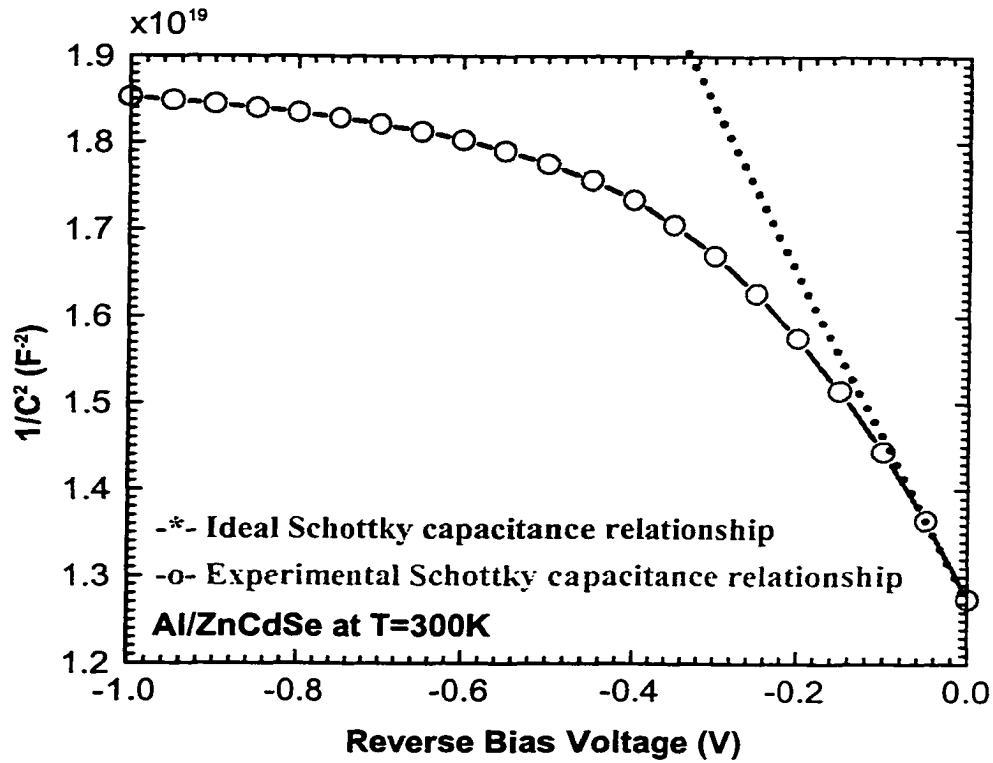


Figure 6.6 shows a nonlinear C^{-2} - V experimental result of II-VI Al/ZnCdSe Schottky diodes.

Many conventional C-V measurements for studying deep-level charge centers in semiconductors are based on the thermal emission of carriers by the traps within the depletion region of a diode. It is commonly assumed that the internal electric field has almost no influence on the results. In fact, depending on the doping level and the bias voltage, this electric field can be very large: typically 10^8 V/m for $N_D - N_A = 10^{18} \text{ cm}^{-3}$ and $V_a = -3 \text{ V}$ ¹⁰. So under reverse bias voltage, deep traps can be further ionized and their ionized electrons can be penetrated their barrier into conductive band, their

$\frac{1}{C^2}-V$ curves are not straight lines as required by ideal Schottky theory.

Therefore, it is critical to precisely understand its transport mechanisms. In our proposed model, two kinds of electric field effects are considered: (1) Frenkel-Poole ionization effect which is achieved by tilting the bands and thus lowering the thermal ionization energy of such a deep center and (2) the tunneling effect. So our model can be called as “electric-field-enhanced tunneling model”.

In Frenkel-Poole effect, owing to two fields i.e., the Coulomb-attractive field of deep center and the external field, overlap, the parabolic barrier is better suited as an approximation for metal-semiconductor Schottky diodes. Its electric-field-enhanced thermal ionization probability of a deep charge center is as follows.¹¹

$$I_{tc} = I_{tc}^{(0)} \exp\left(\frac{\beta \sqrt{F}}{kT}\right) \quad (6.5)$$

$$\beta = \sqrt{\frac{e^3}{\pi \epsilon_s \epsilon_0}} \quad (6.6)$$

where $I_{tc}^{(0)}$ is the non-field thermal ionization probability, F is the applied electric field, e and ϵ_0 are the electric charge and permittivity of free space and ϵ_s is the relative high-frequency dielectric constant, respectively.

Oppenheimer,¹² Fowler and Nordheim¹³ pointed out that it is most possibility that electrons can penetrate potential barrier through tunneling when these barriers are thin and low in the semiconductor. In the tunneling effect, space charge density is no longer nearly a constant and consists of two parts. One is provided by the donor impurity atoms according to ideal Schottky theory, another is electric-field-enhanced tunneling electron density provided by deep traps.

$$N = N_d + N_e \quad (6.7)$$

where N_d is the Schottky donor concentration, whereas N_e is a "excess space charge concentration" which has a field dependence given by.

$$\begin{aligned} N_e &= N_{t0} \times T_{en} = N_{t0} \times \exp\left(-\int_0^{a_0} |k(x)| dx\right) = N_{t0} \times \exp\left(-\frac{\pi}{2} \sqrt{\frac{2m}{(h/2\pi)^2}} \frac{(E_b)^{3/2}}{eF}\right) \\ &= N_{t0} \times \exp\left(-\pi^2 \frac{V_b}{V}\right) \end{aligned} \quad (6.8)$$

where N_{t0} is the concentration of deep centers, T_{en} is the field enhanced tunneling transmission probability.¹¹ Here, E_b is the parabolic energy barrier height, m is the electron effective mass, e is electronic charge, $h/2\pi$ is Planck's constant, F is electric field, V_b is E_b/e and V is $\lambda_0 F$

$$\left(\frac{2\pi}{\lambda_0} = k_0 = \sqrt{\frac{2mE_b}{(h/2\pi)^2}}\right), \text{ respectively.}$$

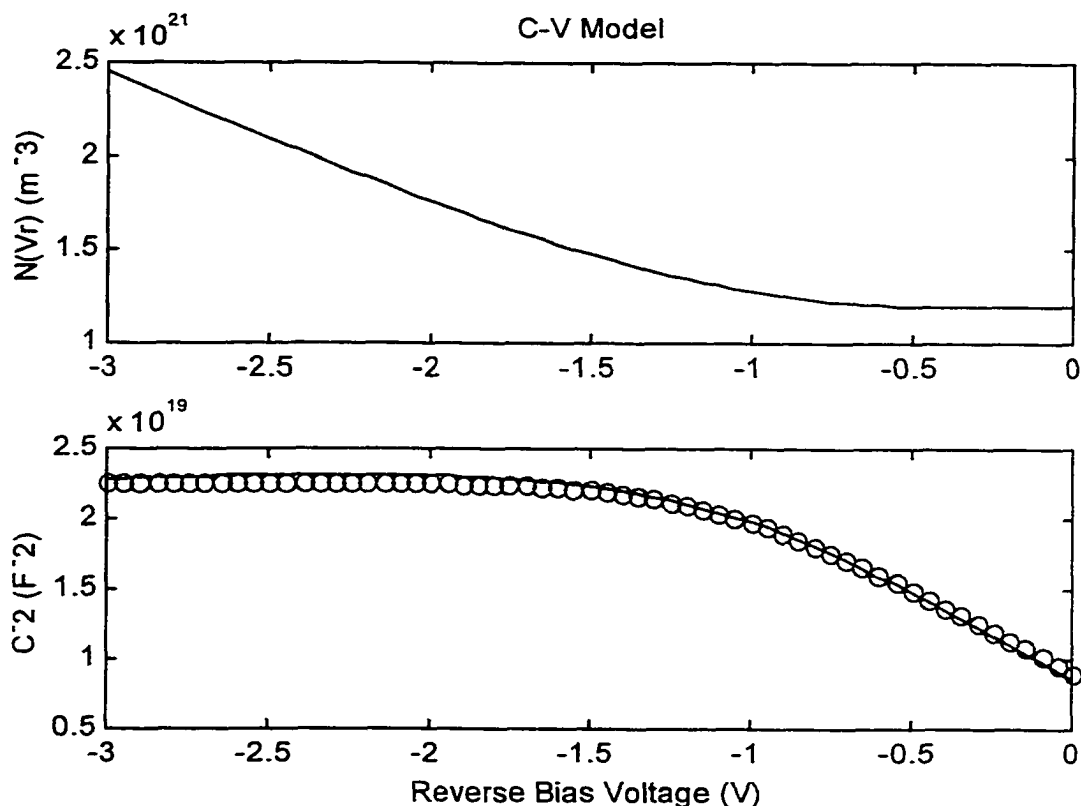


Figure 6.7 N vs V and C^2 vs V plots, Circle dots are experimental observation, solid line is theoretical simulation result.

The above Figure 6.7 shows the $\frac{1}{C^2} - V$ curve obtained from one of our best devices measured at 1-MHz frequency in the dark. Circle dots are experimental observation and line is theoretical simulation result. Both of them present much more promising context. As shown in Figure 6.7, a significant phenomenon is observed that $\frac{1}{C^2} - V$ plot appears bent from about -0.4 V. According to our theoretical simulation result, the height of its parabolic barrier is about 0.32 eV, the Schottky barrier of $\text{Zn}_{0.61}\text{Cd}_{0.39}\text{Se}$

is about 0.85 V, Schottky donor concentration is found to be $1.2 \times 10^{15} \text{ cm}^{-3}$, trap concentration is $\sim 3.3 \times 10^{14} \text{ cm}^{-3}$, i.e., one order of magnitude below the free-carrier concentration. This is a very promising result. Many authors¹⁴⁻¹⁶ reported a close relationship to the well-known electron trap in ZnSe with a thermal activation energy of 0.30-0.34 eV. Vardya and Mahajan¹⁷ pointed out that a Se vacancy or a V_{Se} -impurity complex is responsible for the about 0.32 eV trap, Hu¹⁵ also described the trap to a Zn vacancy defect. Vardya and Mahajan explained this deep center as a sum of at least four different centers with different trap parameters, related to different V_{Se} -impurity configurations. Further studies require additional information that can be obtained from deep-level transient spectroscopy (DLTS) and electron spin resonance measurement.

In summary, our “electric-field-enhanced tunneling” model can be used as an effective tool to analyze the deep-level charge centers’ characteristics of II-VI $\text{Al/Zn}_x\text{Cd}_{1-x}\text{Se}$ Schottky diodes. The theoretical simulation results from our novel model indicate there exist deep centers with concentration ($3\text{-}4.5 \times 10^{14} \text{ cm}^{-3}$) and parabolic-barrier height (0.32V). The results give implication that the predominant trap in $\text{Zn}_x\text{Cd}_{1-x}\text{Se}$ has the same origin as the well-known $\sim 0.32 \text{ eV}$ trap in ZnSe.

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CHAPTER 7

III-V Semiconductor Based on Schottky Cell Memory

7.1 III-V semiconductor materials

– Au/GaAs/AlGaAs/GaAs/AlAs/GaAs/ n^+ -GaAs

For the initial demonstration of the SCM principle, Al/Zn_{1-x-y}Cd_xMg_ySe/InP(buffer layer)/ n^+ -InP (substrate) metal/semiconductor (MS) structures were successfully applied.¹ To further validate the SCM concept and extend its range, we will report on the design and demonstration of SCM devices using III-V GaAs/AlGaAs semiconductor quantum structures.² There are two types of structures A and B. The structure A consists of the layers of Au(300 nm)/i-GaAs(5 nm)/n-Al_xGa_{1-x}As(500 nm, x=0.30, Si: $5 \times 10^{16} \text{ cm}^{-3}$)/i-GaAs(5.6 nm)/i-AlAs(2 nm)/ n^+ -GaAs(150 nm buffer layer, Si: $2 \times 10^{18} \text{ cm}^{-3}$) on n^+ -GaAs substrate. The structure B is identical to the A except the 5.6 nm i-GaAs layer is omitted as shown in Figure 7.1. All of the III-V SCM devices were grown by a Varian Gen-II solid source molecular beam epitaxy (MBE) on n^+ -GaAs (100) substrates. The gold

contacts with a thickness of 300 nm and a diameter of 2 mm were deposited through a mask on the epilayers using a high vacuum evaporator. Individual devices were then cleaved from the wafers and bonded to standard device holders. The current-voltage (I-V) measurements were taken with a computerized HP4142B source/monitor unit in the dark at room temperature.

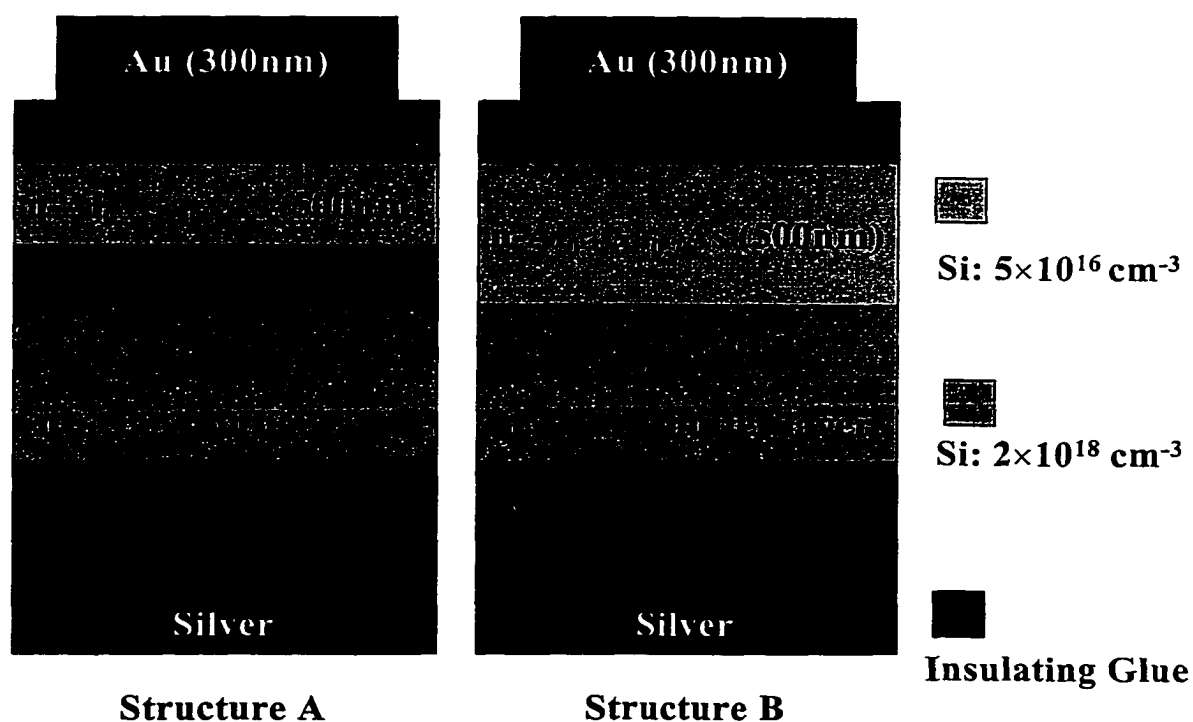


Figure 7.1 Cross-section of Structure A (Au/GaAs/AlGaAs/GaAs/AlAs/ n^+ -GaAs) and Structure B (Au/GaAs/AlGaAs/AlAs/ n^+ -GaAs).

7.2 Computer simulation results

By self-consistently solving Poisson and Schrödinger equations,³ we have calculated conduction band edge, E_C , electron density, and electric field as function of distance from the MS interface. The results of calculated E_C for the structures A and B are displayed in Figure 7.2 (a) and (b), respectively. The dashed line indicates the Fermi energy level. On the Schottky contact side, the Schottky barrier height ($e\Phi_b$) and built-in potential energy (eV_b) are 0.8 and 0.7 eV, respectively, for both structures A and B. On the ohm contact side, there is a quantum well formed by the AlGaAs and AlAs barriers for the structure A while there is no quantum well in the structure B. The electron density in the quantum well at equilibrium is on the order of 10^{18} cm^{-3} as shown in Figure 7.3. The free electron density is below 10^{15} cm^{-3} in the depletion region from 0 to 100 nm. The sub-band energies are calculated to be 6.4 meV below and 117.5 meV above the Fermi level for the ground and the first excited state, respectively, as shown in Figure 7.4. However, according to earlier research,⁴ negatively charged DX⁻ centers in the AlGaAs layer are known to exist and have a density level similar to the Si doping level (10^{16} cm^{-3}). The energy diagram for a DX center is schematically shown in Figure 7.2

(a). For AlAs mole fraction ($x=0.30$) and Si donors, the capture energy E_{ca} is 0.21 eV and the emission energy E_{em} is 0.43 eV. Without external bias, these negatively charge DX^- centers are stable even they are near the metal-semiconductor interface where the maximum electric field ($\sim 10^5$ V/cm) occurs. When a critical reverse bias (V_n) is applied, each DX^- center near the metal-semiconductor interface will emit two electrons to the conduction band ($DX^- \leftrightarrow D^0 + e^- \leftrightarrow D^+ + 2e^-$). They will be drifted away from the metal-semiconductor interface leaving behind additional ionized donors. It is these additional ionized donors near the metal-semiconductor interface that result in a large image lowering effect⁵ on the Schottky barrier height. To maintain the lowered Schottky barrier height even after removing external bias, a suitable quantum well is placed 500 nm away from the metal-semiconductor interface. This quantum well is essential and is used to capture and store the electrons emitted from DX^- centers near the metal-semiconductor interface. The Schottky barrier height will be recovered once these electrons stored in the quantum well are drifted back and captured by the D^+ donors restoring DX^- centers near the metal-semiconductor interface. For the comparison purpose, the structure B is designed not to contain a quantum well. Therefore, the lowered Schottky

barrier height cannot be sustained after removing the external bias. No memory effect is expected from this structure.

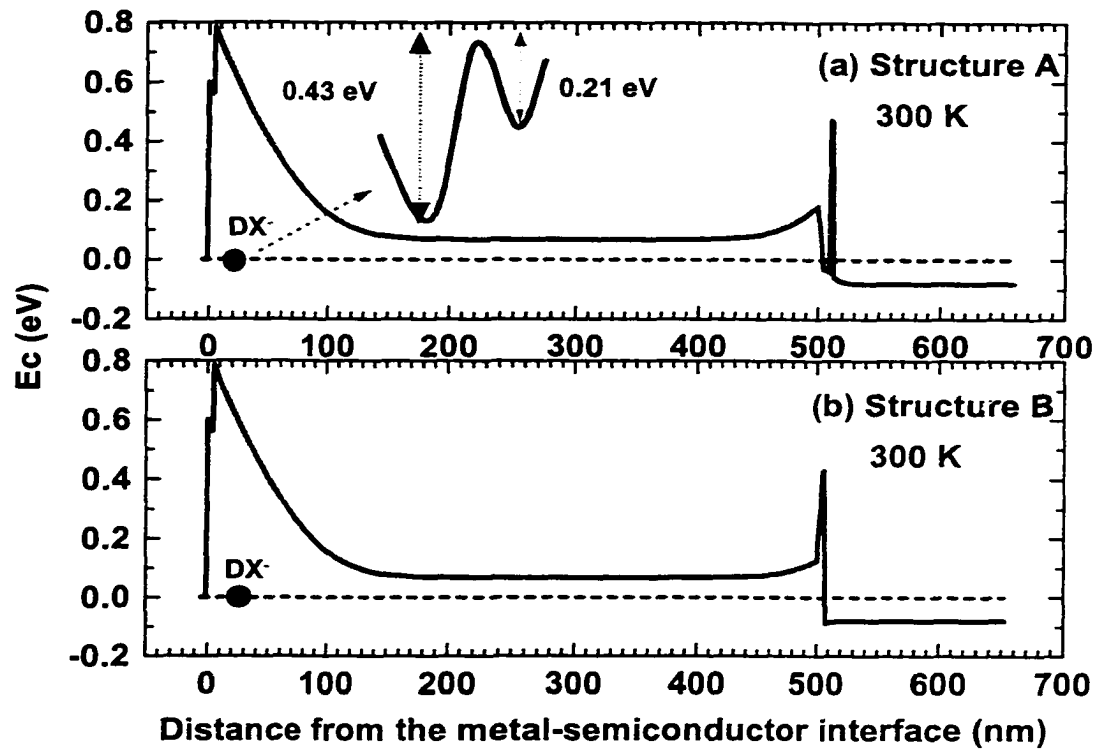


Figure 7.2 Calculated conduction band edge E_C for the structure A and B. The filled circles indicate the negatively charged DX^- centers near the M-S interface. The insert in (a) shows an energy diagram of a DX^- center.

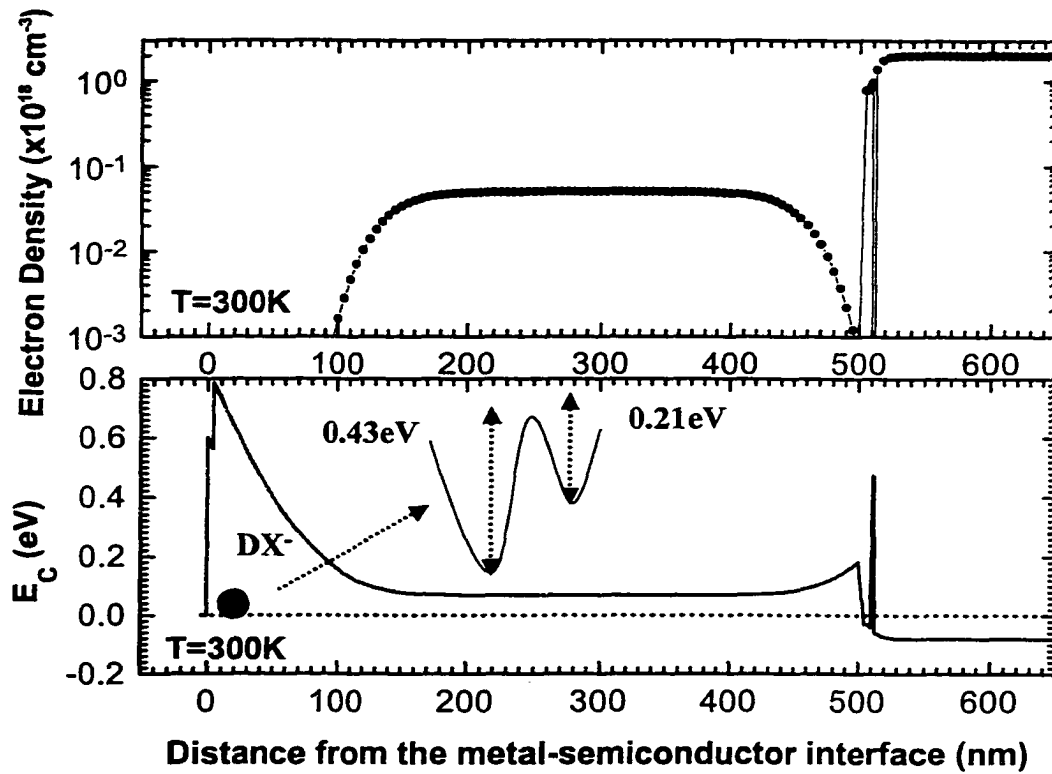


Figure 7.3 Calculated conduction band edge E_C and calculated electron density for the Structure A (Au/GaAs/AlGaAs/GaAs/AlAs/ n^+ -GaAs). The filled circle indicates the negatively charged DX^- centers near the M-S interface. The insert shows an energy diagram of a DX^- center.

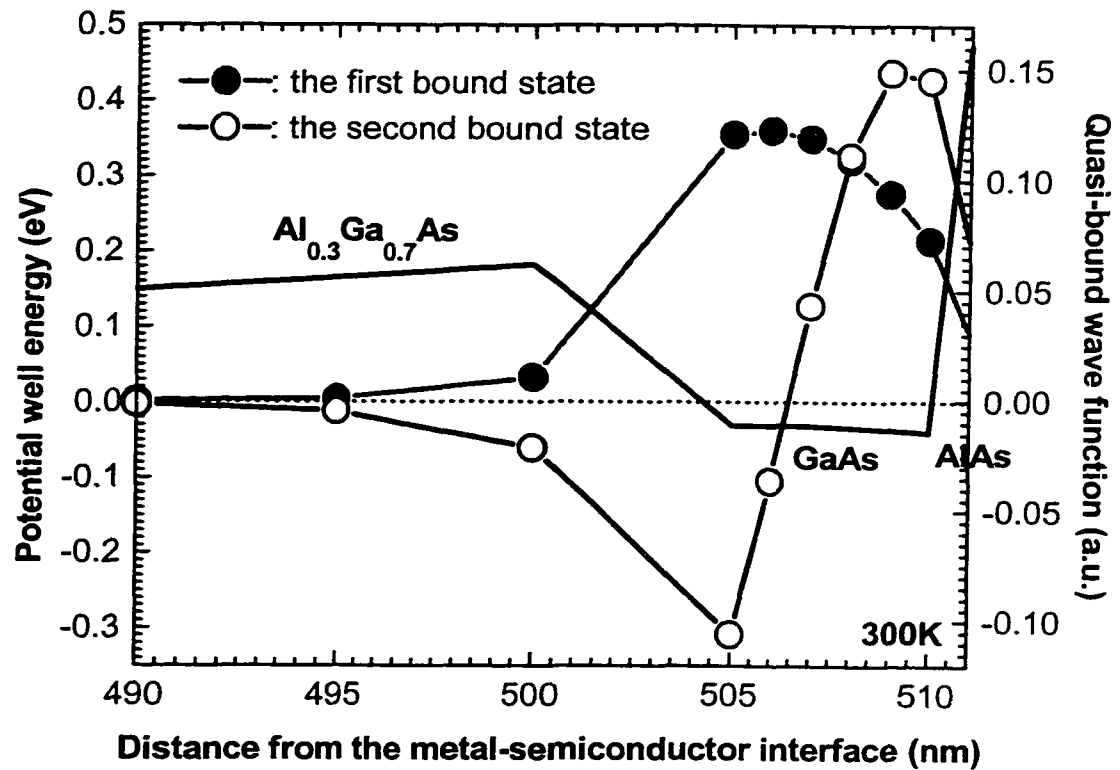


Figure 7.4 Calculated two quasi-bound states in the AlGaAs/GaAs quantum well.

7.3 Basic III-V SCM characteristics

Besides conventional device characteristics, the SCM also has some important functional memory characteristics, which are used to evaluate the memory performance of the SCM. These characteristics can be divided into four main classes.

1. The I-V characteristics describe its bi-resistance characteristics of the SCM.
2. The threshold voltage characteristics demonstrate its relationship between turn-on voltage and applied pulse during programming.
3. The endurance characteristics give the SCM threshold window, which is the difference between the threshold voltages in the written and the erased states, as a function of the number of programming cycles. They are characteristic for the intrinsic number of write/erase cycles that can be endured before both programmed states are no longer distinguishable.
4. Finally, the retention characteristics give the threshold voltage in either programmed state as a function of the time after programming, and indicate the intrinsic ability of the SCM to retain its content over long periods of time.

In order to demonstrate the above characteristics of our III-V SCM, we arrange to set up a computer controlled experimental system and to write a program using Window version of HP basic to control a multiple source/monitor system (HP 4042B). Using this set-up, we measured and recorded the following experimental results: (1) the I-V curves (on-state

and off-state) of III-V Structure A and B in a given sense voltage range under a trig voltage pulses (V_p - and V_n -pulses), respectively; (2) the turn-on voltage of Au/GaAs/AlGaAs/GaAs/AlAs/ n^+ -GaAs SCM device in order to further unveil DX-center origin. Since this threshold voltage is related to the capture and emission energy of the DX centers, the fact that $\frac{V_{th}(off-to-on)}{V_{th}(on-to-off)} \equiv \frac{E_{em}}{E_{ca}}$ provides a self-consistent evidence that the DX centers near the metal-semiconductor interface act as a source of the electric-field-controllable donors; (3) the endurance of Au/GaAs/AlGaAs/GaAs/AlAs/ n^+ -GaAs SCM device, cycling was planned to perform by measuring the on-state and off-state current at a constant bias under a train of alternately positive and negative excitation pulses (V_p -/ V_n -pulses); (4) the endurance of the Au/GaAs/AlGaAs/GaAs/AlAs/ n^+ -GaAs SCM device, we measured its on-state and off-state currents at a constant bias in a same time interval. Its on-state and off-state were prepared by the electrical pulse excitations of V_n and V_p , respectively.

These experimental results and discussions are described in detail as follows.

The I-V data for the structure A and B are displayed in Figure 7.5 (a) and (b), respectively. The dashed curves were measured without any additional electrical excitation other than bias voltage source. The turn-on

voltage for both devices A and B is about 0.7 V as it is consistent with the built-in voltage. The open-circle and filled-circle curves were measured after each device was electrically excited by a positive pulse and a negative pulse, respectively. The pulse height/width of 10 V/50 ms was used. For the device A, it is apparent that the I-V curve after the positive (negative) pulse excitation is shifted towards higher (lower) turn-on voltage. Consider the turn-on voltage is approximately equal to the built-in potential V_b , and then the I-V data show that the barrier height can be effectively altered by electrical excitations. The device maintains its higher barrier height (off) or lower barrier height (on) state until another excitation arrives to alter the state. For the device B, no I-V curve shifts were observed under the same electrical excitations as expected. This experimental observation clearly demonstrates the SCM concept.

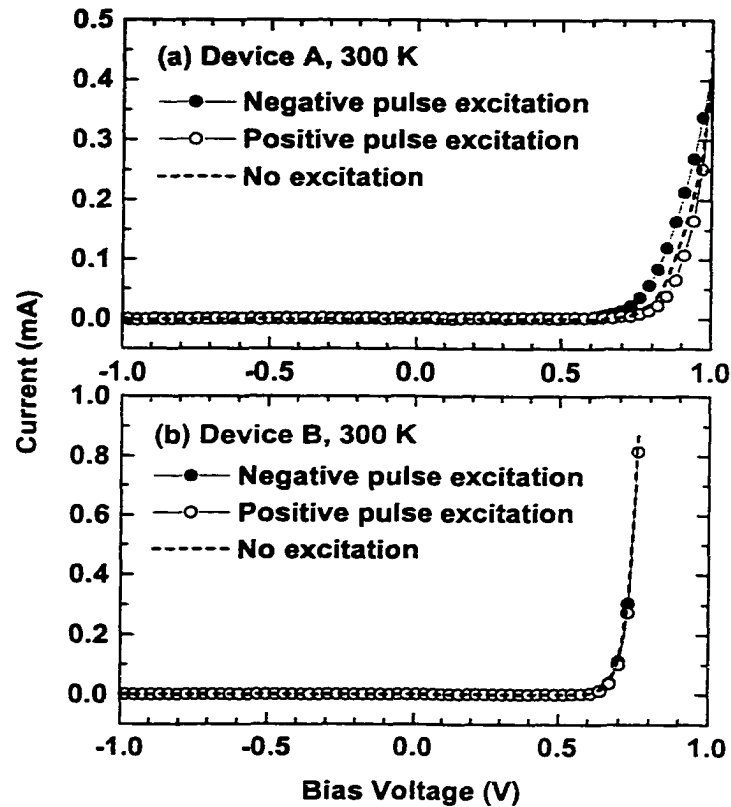


Figure 7.5 Measured I-V data for the device A (a) and B (b).

Figure 7.6 shows the excitation pulse height dependence of the turn-on voltage for device A. The turn-on voltage increases as the (positive) pulse height increases from 3 to 10 V [Figure 7.6 (a)] while it decreases as the (negative) pulse height increases from -3 to -13 V [Figure 7.6 (b)]. It appears in this figure that a threshold pulse height (V_{th}) can be defined to turn the device from either off to on or from on to off state transition. This threshold voltage is about -9 V for off to on and 4.5 V for on to off as indicated in the figure. Since this threshold voltage is related to the capture

and emission energy of the DX centers, the fact that

$$\frac{V_{th}(off-to-on)}{V_{th}(on-to-off)} = \frac{9}{4.5} \cong \frac{E_{em}}{E_{ca}} = \frac{0.43}{0.21}$$

provides a self-consistent evidence that

the DX centers near the metal-semiconductor interface act as a source of the electric-field-controllable donors.

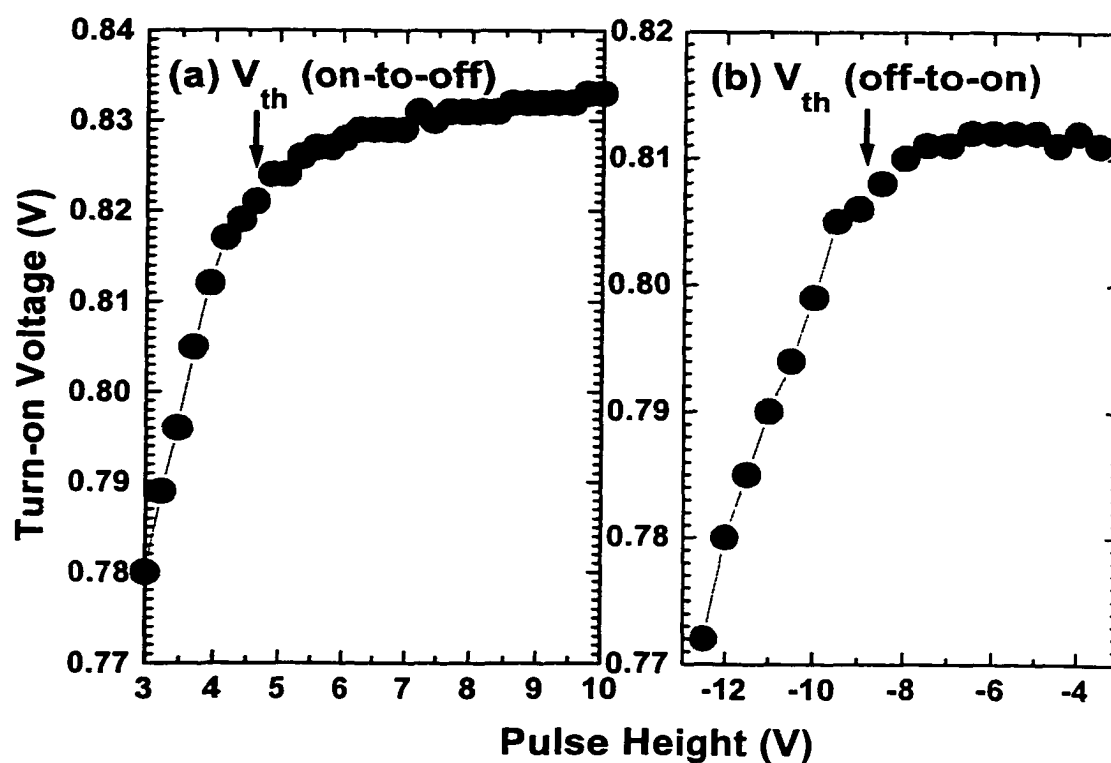


Figure 7.6 Turn-on voltage as a function of the electrical excitation pulse height (pulse width=500 ms) for the device A, (a) from on state to off state by applying positive pulses, and (b) from off state to on state by applying negative pulse.

To evaluate the endurance of the device A, cycling was performed by measuring the on-state and off-state current at the bias of 0.85 V under a

train of alternately positive and negative excitation pulses ($V_p=10$ V, $V_n=-10$ V, and width of 500 ms). The measured current at the on and off state is displayed in Figure 7.7 (a). It appears that the on-state current can hold on the level of 30 μ A and the off-state current tends to increase from 21.5 to 23.5 μ A during a period of 50 write/erase cycles. Based on the slope of the off-state current change, 2 μ A/50 cycles, the endurance of the device A is estimated to be 200. Although this number is too far away from the required number to meet the practical needs, it clearly demonstrates the SCM concept and warrants more research to validate this emerging technology.

The retention characteristics of the device A are shown in Figure 7.7 (b). On-state and off-state were prepared by the electrical pulse excitation of -10 and 10 V, respectively. The pulse duration of 500 ms was used. The on-state and off-state currents were measured at 0.85 V in a 20 s time step. The current difference between on and off state is about 8 μ A and is still detectable up to 10^4 s.

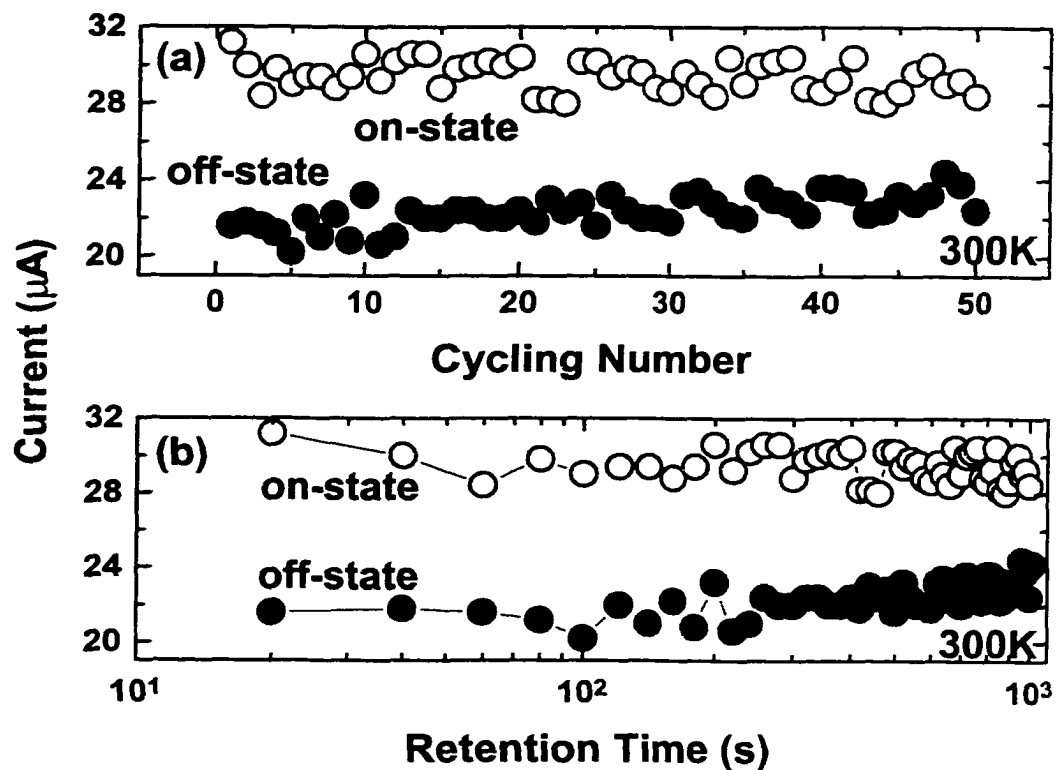


Figure 7.7 (a) On-state and off-state current for the memory device A at 0.85 V as a function of cycling number. (b) Retention characteristics of the memory device A.

In conclusion, we have designed and demonstrated a promising nonvolatile memory device based on the GaAs/AlGaAs material system. The device performance can be further improved along the line of the Schottky cell memory concept. For example, the depth of quantum well can be adjusted by using InGaAs instead of GaAs to effectively store electrons.

Finally, if possible, we will explore the possibility of fabricating the new memories using SiGe/Si substrates that is quasi-lattice-matched to Si substrates. Their detailed structures were described in Chapter Four. Since this material has been extensively studied by IBM Thomas J. Watson Research Center⁶⁻⁸ for bipolar junction transistor (BJT) and heterojunction bipolar transistor (HBT) applications. High quality $\text{Si}_{1-x}\text{Ge}_x$ ($x=0.3-1$) films were grown on Si substrates by ultrahigh-vacuum chemical-vapor deposition (UHV/CVD) using Si as buffer layer. This $\text{Si}_{1-x}\text{Ge}_x$ material is interesting since it can be grown on quasi-lattice-matched Si substrates where the mainstream Si transistors can be integrated on.

References

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- ⁷ D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y. Sun, B. S. Meyerson, and T. Tice, IEEE Trans. on Electron Devices **42**, 455 (1995).
- ⁸ D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y. Sun, B. S. Meyerson, and T. Tice, IEEE Trans. on Electron Devices **42**, 469 (1995).

CHAPTER 8

Technological Prospect of SCM

Since the NVMs have many advantages over the rotation-related storage devices, it is clear that the NVM market is growing rapidly and will continue to do so into the foreseeable future. NVM is competing in an industry where rotating storage media dominates. Up to now, the Flash memory and the FRAM are replacing hard disks in some applications. Since there are some intrinsic drawbacks (for example, relatively low density 4 Mbits/inch² of FRAM memory and limited write/erase cycles of Flash memory) in those two technologies, any new NVM technology, which has potential to overcome those drawbacks, will have a real impact to this field. Figure 8.1 shows the NVM technology roadmap surging as device densities increase and its importance to the industry. At the 256-Kbit level, NVM chips just replace EEPROM and battery backed, SRAM for the storage of configuration and parameter data. The 1-Mbit and 4-Mbit NVM devices will begin to replace DRAM and SRAM as a solution for working memory. The world's first 4-Mbit FRAM has been developed in Samsung Electronics Company in 1999.¹ At densities of 16 Mbits and

above, NVM technology will become the optimum solution for systems that can use an all-in-one memory to handle work memory and data/parameter storage. We believe that depending on SCM unique features, which have full bit write/erase capability, very low write/erase voltage, nondestructive read operation, and simple memory structure, the proposed SCM will become a new rival to existing NVM family.

The Importance of Nonvolatile Memory Technology to Industry

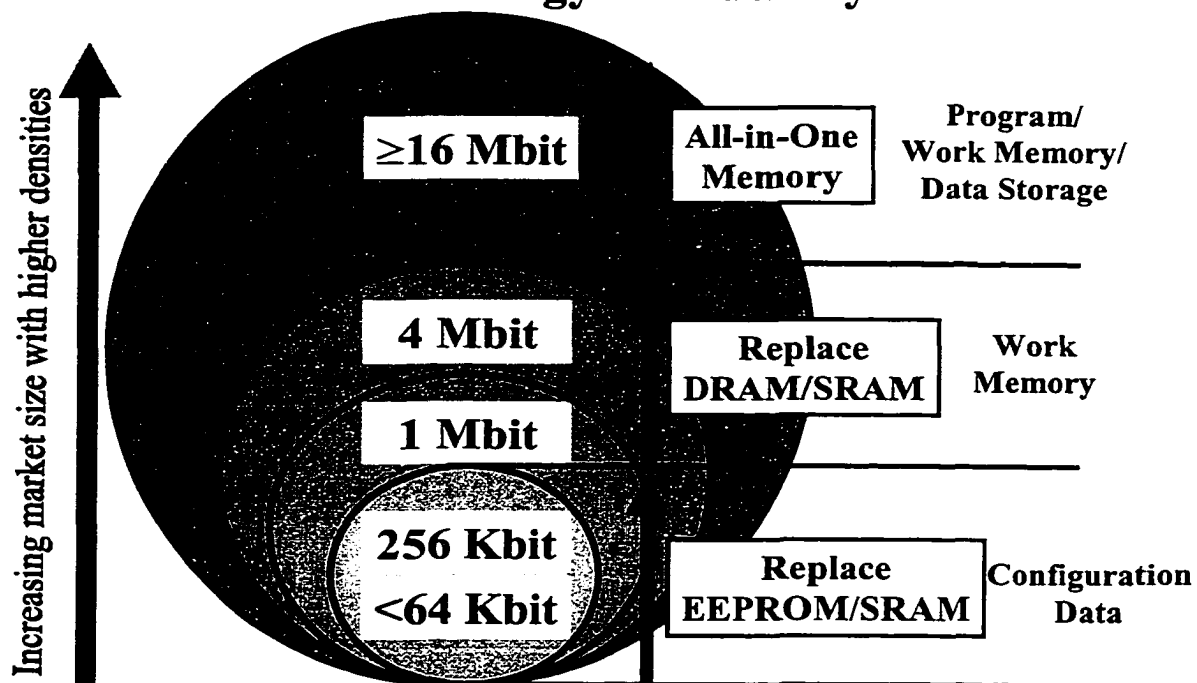


Figure 8.1: The role of NVM and the importance of this innovative NVM technology to the industry will surge as device densities increase, possibly leading to the market developments shown here.

Reference

- ¹ EDTN Network Electronic Buyers' News, "Samsung readies 4-Mbit FRAM", <http://www.semibiznews.com/>.

CHAPTER 9

Summary and Future Work

9.1 Summary

The main objectives of the research in Ph.D. dissertation are (1) to further investigate its origin and mechanism of electric-field-controlled charge centers near the metal-semiconductor (M-S) interface; (2) to extend SCM technology to III-V semiconductor material systems such as Au/GaAs/AlGaAs/GaAs/AlAs/GaAs(buffer layer)/n⁺-GaAs(substrate); (3) to simulate SCM device's energy diagram and to measure NVM's functional parameters to further design and optimize its structure; (4) to further study SCM device's nonvolatile memory characteristics; (5) to propose some more practical SCM structures by concluding and analyzing above mechanism. The following is the summary of the Ph.D. research work:

Objective 1: to further investigate its origin and mechanism of electric-field-controlled charge centers near the M-S interface.

- We proposed an “electric-field-enhanced tunneling” model to effectively analyze the deep-level charge centers’ characteristics of II-VI Al/Zn_xCd_{1-x}Se SCM devices. The theoretical simulation results from our proposed model indicate there exist deep centers with concentration ($3-4.5 \times 10^{14} \text{ cm}^{-3}$) and parabolic-barrier height (0.32V). The results give further implication that the predominant trap in Zn_xCd_{1-x}Se has the same origin as the well-known $\sim 0.32 \text{ eV}$ trap in ZnSe.
- In turn-on voltage experiment for III-V Au/AlGaAs/GaAs SCM device. We obtained the result $\frac{V_{th}(off-to-on)}{V_{th}(on-to-off)} = \frac{9}{4.5} \cong \frac{E_{em}}{E_{ca}} = \frac{0.43}{0.21}$. The fact provides a self-consistent evidence that the DX centers near the metal-semiconductor interface act as a source of the electric-field-controllable donors because its threshold voltage is related to the capture and emission energy of the DX centers.

Objective 2: to extend SCM technology to III-V semiconductor

**material systems such as Au/GaAs/AlGaAs/GaAs/AlAs/
GaAs (buffer layer)/n⁺-GaAs (substrate).**

- To further validate the SCM concept and extend its range, we designed and demonstrated SCM devices using III-V GaAs/AlGaAs semiconductor quantum structures. The III-V SCM (A device) structure is Au(300 nm)/i-GaAs(5 nm)/n-Al_xGa_{1-x}As(500 nm, x=0.30, Si: 5×10¹⁶ cm⁻³)/i-GaAs(5.6 nm)/i-AlAs(2 nm)/n⁺-GaAs(150 nm buffer layer, Si: 2×10¹⁸ cm⁻³) on n⁺-GaAs substrate. For the comparison purpose, we also designed other III-V device (B device) that is identical to the above structure except the 5.6 nm i-GaAs layer is omitted. The I-V data were measured after each device was electrically excited by a positive pulse and a negative pulse, respectively. The pulse height/width of 10 V/50 ms was applied. For the device A, we apparently discovered that the I-V curve after the positive (negative) pulse excitation is shifted towards higher (lower) turn-on voltage and the device A maintains its higher barrier height (off) or lower barrier height (on) state until another excitation arrives to alter its state. But for the device B, no I-V curve shifts were

observed under the same electrical excitations as expected. This result clearly demonstrates our SCM principle.

Objective 3: to simulate SCM energy diagram and to measure NVM's functional parameters to further design and optimize its structure.

- By solving self-consistently Poisson and Schrödinger equations, we simulated III-V SCM device's energy band diagram, electron density, electric field and quasi-bound energies and their wave functions in quantum well. For the device A, the sub-band energies are simulated to be 6.4 meV below and 117.5 meV above the Fermi level for the ground and the first excited state, respectively, in the AlGaAs/GaAs quantum well. The result demonstrates the device A can hold electrons in its quantum well. But the device B has no sub-band energy since it has no quantum well. The above simulation results are in good agreement with our experimental observations. We think the self-consistent Poisson and Schrödinger solver is a very useful tool to further design and optimize our SCM structure.

Objective 4: to further study III-V SCM device's nonvolatile memory characteristics.

- We mainly study the following four SCM characteristics: I-V characteristics, threshold voltage characteristics, endurance characteristics and retention characteristics. The I-V and threshold voltage characteristics are discussed above. The endurance result appears that the on-state current can hold on the level of 30 μA and the off-state current tends to increase from 21.5 to 23.5 μA during a period of 50 write/erase cycles for the device A. Based on the slope of the off-state current change, 2 $\mu\text{A}/50$ cycles, the device A's endurance is estimated to be 200. Retention result demonstrates that the current difference between on and off state is about 8 μA and is still detectable up to 10^4 s. Although these results are far away from the practical needs, they clearly demonstrate the SCM concept and warrant more research to validate this novel emerging technology.

Objective 5: to propose some more practical SCM structures by concluding and analyzing above mechanism.

- By concluding and analyzing SCM mechanism, SCM model's key is the reversible carrier transport between an electric-field-controlled charge source and an adjacent potential well (carriers are referred to hereinafter electrons for electron-based semiconductor devices and holes for hole-based semiconductor devices). The electric-field-controlled charge source may be provided by the following three ways: DX-center, deep heterostructure quantum well, and δ -doping quantum well. Therefore, we proposed the following three more practical structures: (1) SCM consists of two deep p-type SiGe quantum wells on a p-type Si substrate. The structure is compatible with conventional silicon processing for integration with other microelectronic elements on the same silicon substrate; (2) Two n-type InGaAs quantum wells on an n-type GaAs substrate are used to form the basic SCM's elements. This structure is compatible with GaAs electronic devices such as GaAs junction field-effect transistors and bipolar transistors; and (3) n-type δ -doping as another means forms a deep quantum wells in Schottky depletion region on n^+ -Si substrate. This structure may be fully compatible with silicon electronic devices.

9.2 Future work

Finally, we introduce a kind of circuit architecture of nonvolatile random access memory (NVRAM) as shown in Figure 9.1. Its feasibility and utility will be further examined in the future work.

Its basic principle is as follows. Different from other RAM, no transistors are applied in the memory cell. Each memory cell consists of two diodes and one memory device disclosed here. There are connected to three lines: READ/WRITE0, WRITE1, and WORD LINE. Using these three lines, each memory cell can be selected, read, and written. The READ/WRITE0 line is used to read data from or to write logical 0 state (off-state) to a selected memory cell. The WRITE1 line is used for only writing logical 1 state (on-state) to a selected memory cell. Each word line is connected to a transition gate that allows two-way current flow. When one word line is selected, this line is connected to ground, all other word lines are in floating state.

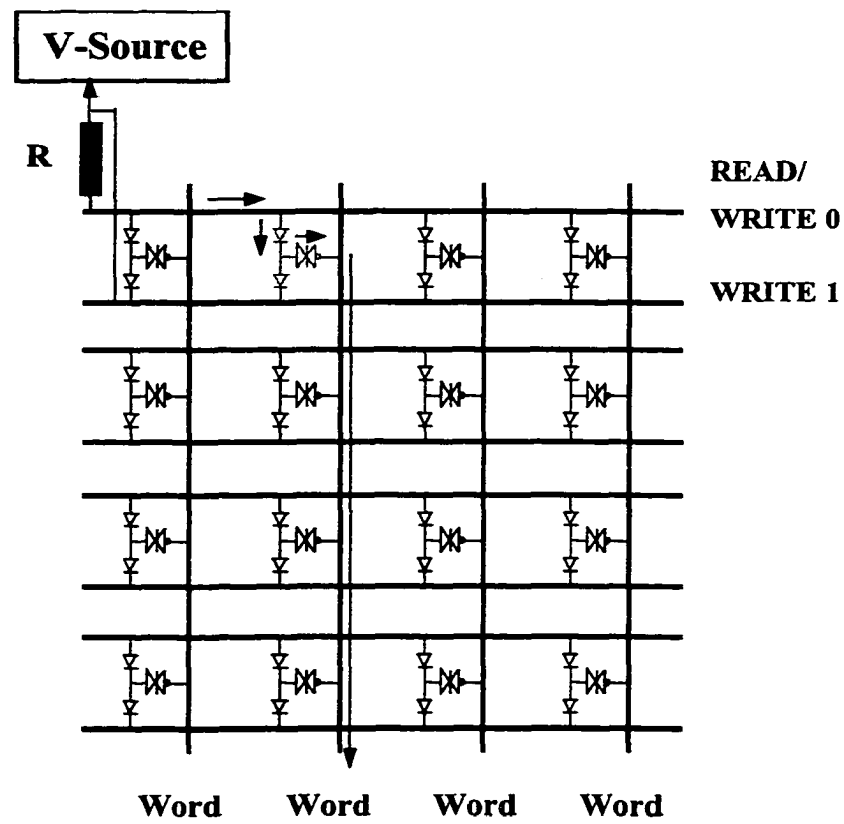


Figure 9.1: Schematic circuit diagram for nonvolatile random access memory utilizing our NVM devices disclosed before.

APPENDIX A

A.1 Matlab programs for electric field distributions

% this part of program is to calculate the electric field distributions

```

q=1.6e-19;
er=11.7;
e0=8.854e-14;
es=er*e0;
nd1=1.0e17;
nd=1.0e19;
alpha=0;
%alpha=5.0e-2;
nd2=nd*alpha;
d1=q*nd1/es;
d2=q*nd2/es;
nc=2.8e19;
vt=0.026;
vn=vt*log(nc/nd1);
mu=1.0e-4;
xn=0.1*mu;
a=0.015*mu;
a1=0.02*mu;
b=0.105*mu;
b1=0.11*mu;

```

```

x=b1*[0:1e-4:1];
ef1=zeros(length(x),1);
ef2=zeros(length(x),1);
ef=zeros(length(x),1);

for i=1:length(x)
    if x(i) <= a
        ef1(i)=d1*(x(i)-xn);
        ef2(i)=d2*(b1-b)-d2*(a1-a);
        ef(i)=ef1(i)+ef2(i);
    elseif x(i) <= a1
        ef1(i)=d1*(x(i)-xn);
        ef2(i)=d2*(b1-b)-d2*(a1-x(i));
        ef(i)=ef1(i)+ef2(i);
    elseif x(i) <= xn
        ef1(i)=d1*(x(i)-xn);
        ef2(i)=d2*(b1-b);
        ef(i)=ef1(i)+ef2(i);
    elseif x(i)<= b
        ef1(i)=0;
        ef2(i)=d2*(b1-b);
        ef(i)=ef1(i)+ef2(i);
    else
        ef1(i)=0;
        ef2(i)=d2*(b1-x(i));
        ef(i)=ef1(i)+ef2(i);
    end
end
end

```

```

subplot(3,1,1)
plot(x,ef1,'b')
ylabel('E(1)(V/cm)')
hold on
subplot(3,1,2)
plot(x,ef2,'g')
ylabel('E(2)(V/cm)')
hold on
subplot(3,1,3)
plot(x,ef1,'b',x,ef2,'g',x,ef,'r')
xlabel('Distance (cm)')
ylabel('E=E(1)+E(2)(V/cm)')
hold off

fid=fopen('ef.dat','w');
for i=1:length(x)
    fprintf(fid, '%12.8e %12.8f %12.8f %12.8f\n',x(i),ef1(i),ef2(i),ef(i));
end
fclose(fid);

```

A.2 Matlab programs for Schottky effect

% this program is to calculate potential energy and Schottky effect

```

q=1.6e-19;
er=11.7;
e0=8.854e-14;
es=er*e0;
nd1=1.0e17;
nd=1.0e19;

```

```

alpha=0;
%alpha=5.0e-2;
nd2=nd*alpha;
d1=q*nd1/es;
d2=q*nd2/es;
nc=2.8e19;
vt=0.026;
vn=vt*log(nc/nd1);
mu=1.0e-4;
xn=0.1*mu;
a=0.015*mu;
a1=0.02*mu;
b=0.105*mu;
b1=0.11*mu;

for i=1:length(x)-1
    if sign(ef(i)) ~= sign(ef(i+1))
        xo=x(i);
        break
    end
end

x=b1*[5e-3:1e-3:1];
phi0=zeros(length(x),1);
vimg=zeros(length(x),1);
ec0=zeros(length(x),1);
ec=zeros(length(x),1);

if xo <= a
    xmin=xn+(d2*(a1-a)-d2*(b1-b))/d1
    Remark='this point is in [0,a]'

```

```

c1=d1/2*((xmin-xn)^2)+d2*(b1-b)*xmin-d2*(a1-a)*xmin;
phib0=vn+abs(-d1/2*(xn^2)+c1)
for i=1:length(x)
    if x(i) <= a
        phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+d2*(a1-a)*x(i)+c1;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    elseif x(i) <= a1
        phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*((x(i)-a1)^2)-d2*(b1-b)*x(i)+d2/2*(a1^2-
            a^2)+c1;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    elseif x(i) <= xn
        phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+d2/2*(a1^2-a^2)+c1;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    elseif x(i)<= b
        phi0(i)=-d2*(b1-b)*x(i)+d2/2*(a1^2-a^2)+c1;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    else
        phi0(i)=d2/2*((x(i)-b1)^2)+d2/2*(a1^2-a^2+b^2-b1^2)+c1;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    end
end
end

```

```

elseif xo <= a1
    xmin=(d1*xn+d2*a1-d2*(b1-b))/(d1+d2)
    Remark='this point is in [a,a1]'
    c2=d1/2*((xmin-xn)^2)+d2/2*((xmin-a1)^2)+d2*(b1-b)*xmin;
    phib0=vn+abs(-d1/2*(xn^2)+d2/2*(a^2-a1^2)+c2)
    for i=1:length(x)
        if x(i) <= a
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+d2*(a1-a)*x(i)+d2/2*(a^2-
                a1^2)+c2;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= a1
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*((x(i)-a1)^2)-d2*(b1-b)*x(i)+c2;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= xn
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+c2;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i)<= b
            phi0(i)=-d2*(b1-b)*x(i)+c2;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        else
            phi0(i)=d2/2*((x(i)-b1)^2)+d2/2*(b^2-b1^2)+c2;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);

```

```

        ec(i)=vimg(i)+ec0(i);
    end
end
elseif xo <= xn
    xmin=xn-d2*(b1-b)/d1
    Remark='this point is in [a1,xn]'
    c3=d1/2*((xmin-xn)^2)+d2*(b1-b)*xmin;
    phib0=vn+abs(-d1/2*(xn^2)+d2/2*(a^2-a1^2)+c3)
    for i=1:length(x)
        if x(i) <= a
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+d2*(a1-a)*x(i)+d2/2*(a^2-
                a1^2)+c3;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= a1
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*((x(i)-a1)^2)-d2*(b1-b)*x(i)+c3;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= xn
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+c3;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i)<= b
            phi0(i)=-d2*(b1-b)*x(i)+c3;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        else

```

```

    phi0(i)=d2/2*((x(i)-b1)^2)+d2/2*(b^2-b1^2)+c3;
    vimg(i)=-q/16/pi/es/x(i);
    ec0(i)=vn-phi0(i);
    ec(i)=vimg(i)+ec0(i);
end
end
elseif xo <= b
    xmin=xo
    Remark='In this region [xn,b], Ef=Constant'
    Remark='Only when Nd2=0 or/and b1=b, Ef=0'
    c4=d2*(b1-b)*xmin;
    phib0=vn+abs(-d1/2*(xn^2)+d2/2*(a^2-a1^2)+c4)
    for i=1:length(x)
        if x(i) <= a
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+d2*(a1-a)*x(i)+d2/2*(a^2-
                a1^2)+c4;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= a1
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*((x(i)-a1)^2)-d2*(b1-b)*x(i)+c4;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= xn
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2*(b1-b)*x(i)+c4;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i)<= b
            phi0(i)=-d2*(b1-b)*x(i)+c4;

```

```

    vimg(i)=-q/16/pi/es/x(i);
    ec0(i)=vn-phi0(i);
    ec(i)=vimg(i)+ec0(i);
else
    phi0(i)=d2/2*((x(i)-b1)^2)+d2/2*(b^2-b1^2)+c4;
    vimg(i)=-q/16/pi/es/x(i);
    ec0(i)=vn-phi0(i);
    ec(i)=vimg(i)+ec0(i);
end
end
else
    xmin=b1
    Remark='this point is in [b,b1]'
    c5=-d2/2*((xmin-b1)^2);
    phib0=vn+abs(-d1/2*(xn^2)+d2/2*(b1^2-b^2+a^2-a1^2)+c5)
    for i=1:length(x)
        if x(i) <= a
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*(b1-b)*x(i)+d2/2*(a1-a)*x(i)+d2/2*(b1^2-
                b^2+a^2-a1^2)+c5;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= a1
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*((x(i)-a1)^2)-d2/2*(b1-b)*x(i)+d2/2*(b1^2-
                b^2)+c5;
            vimg(i)=-q/16/pi/es/x(i);
            ec0(i)=vn-phi0(i);
            ec(i)=vimg(i)+ec0(i);
        elseif x(i) <= xn
            phi0(i)=-d1/2*((x(i)-xn)^2)-d2/2*(b1-b)*x(i)+d2/2*(b1^2-b^2)+c5;
            vimg(i)=-q/16/pi/es/x(i);

```

```

        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    elseif x(i)<= b
        phi0(i)=-d2*(b1-b)*x(i)+d2/2*(b1^2-b^2)+c5;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    else
        phi0(i)=d2/2*((x(i)-b1)^2)+c5;
        vimg(i)=-q/16/pi/es/x(i);
        ec0(i)=vn-phi0(i);
        ec(i)=vimg(i)+ec0(i);
    end
end
end

plot(x,ec0,x,vimg,x,ec)
xlabel('Distance (cm)')
ylabel('Potential Energy (eV)')

fid=fopen ('pe.dat','w');
for i=1:length(x)
    fprintf(fid, '%12.8e %12.8f %12.8f %12.8f\n',x(i),phi0(i),vimg(i),ec0(i),ec(i));
end
fclose(fid);

```

A.3 Matlab programs for I-V relationship

```
% this part of program is to calculate the relationship
% of the current and applied voltage near the metal/semiconductor junction
% as an example of Metal-Si junction
```

```
q=1.6e-19;    %unit: C
m0=9.1094e-31; %unit: kg
mn=1.08*m0;
k=1.38e-23;   %unit: J/K
h=6.625e-34;  %unit: J-s
t=300;        %unit: K
Phion=0.4071;
Phioff=0.5809;
kT=0.0259;    %unit: eV
va=0.5;
r=5.0e-8;     %unit: m
Area=r^2;

x=linspace(-va,va,1e3);
Ion=zeros(length(x),1);
Ioff=zeros(length(x),1);

A=4*pi*q*mn*(k^2)/(h^3)*Area;
Iston=A*(t^2)*exp(-Phion/kT);
Istoff=A*(t^2)*exp(-Phioff/kT);

for i=1:length(x)
    Ion(i)=Iston*(exp(x(i)/kT)-1);
    Ioff(i)=Istoff*(exp(x(i)/kT)-1);
end
```

```

semilogy(x,Ion,x,Ioff)
hold on
ylabel('I(A)')
xlabel('Applied Voltage (V)')

fid=fopen('iv.dat','w');
for i=1:length(x)
    fprintf(fid, '%12.8f %12.8e %12.8e\n',x(i),Ion(i),Ioff(i));
end
fclose(fid);

```

A.4 HP-Basic programs for SCM measurement

```

10  !SCM Mesurment Program
20  !Programmed by Wei Zhang (May,1997), and further modified by Zhongwei
21  !Pan (1999).
30  Main_menu: !
40  OPTION BASE 1
50  COM /Datad/Data_id(25,25,201),Vd(201),Id(201),@Hp4142 !@Hp3488
60  File_name$="mem"
70  Row_begin=1
80  Row_end=5
90  Col_begin=1
100 Col_end=16
110 DIM Id$(15)
120 Xar_i=1
130 Yar_j=1
140 Sweep_mode=1  !1 for single sweep, 3 for double sweep
150 Mode=1
160 Tp=.05 !0.01 = 1ms, 0.05 = 50ms
170 Vp=0

```

```

180  Vd_begin=-.5
190  Vd_end=.5
200  V_ch=2
210  Id_comp1=1.0E-2
220  I_range1=-18      !-11=1nA,-13=100nA,-17=1mA,-19=100mA
230  Id_comp2=2.0E-3
240  I_range2=-17
250  I_max=Id_comp2
260  ASSIGN @Hp4142 TO 717
270! ASSIGN @Hp3488 TO 709
280  LOADSUB ALL FROM "graph1"
290  ON KEY 1 LABEL "v_range" GOTO V_range
300  ON KEY 2 LABEL "vp_Imax" GOTO Vp_imax
310  ON KEY 3 LABEL "Pulse_trig" GOTO Pulse
320! ON KEY 4 LABEL "sweep_trig" GOTO Sweep_trig
330  ON KEY 5 LABEL "save current" GOTO Show_c
340  ON KEY 6 LABEL "load data" GOTO Load_data
350  ON KEY 7 LABEL "save" GOTO Save_data
360  ON KEY 8 LABEL "Reset Instrument" GOTO Reset_i
361  ON KEY 4 LABEL "test" GOTO Test
370  CLEAR SCREEN
380  MASS STORAGE IS "C:\HPBASIC\mem_pro"
390  KEY LABELS PEN 1
400  USER 1 KEYS
410  KEY LABELS ON
420 Menu_end: !
430 GOTO Menu_end
440  !
450  !
460 V_range: !
470  CLEAR SCREEN

```

```

480! INPUT "The column number of Memory cell=?",Xar_i
490! INPUT "the row number of Memory cell=?",Yar_j
491! CALL Row_col(Xar_i,Yar_j)
500 KEY LABELS ON
510 INPUT "V_begin =",Vd_begin
520 INPUT "V_end =",Vd_end
530 INPUT "sweep mode is (1 for single, 3 for double)",Sweep_mode
540 IF Sweep_mode=3 THEN
550 Mode=2
560 END IF
570 V_range_end:~
580 GOTO V_range_end
590 ~
600 ~
610 Sweep_trig:~
620 ON KBD GOTO Sweep_trig_end
630 Vd_step=(Vd_end-Vd_begin)/100
640 FOR Var1=1 TO 201
650 IF Var1>101 THEN
660 Vd(Var1)=Vd_end-(Var1-101)*Vd_step
670 ELSE
680 Vd(Var1)=(Var1-1)*Vd_step+Vd_begin
690 END IF
700 NEXT Var1
710 GINIT
720 GRAPHICS ON
730 FOR Var_i=1 TO 16
740 FOR Var_j=1 TO 16
750 OUTPUT @Hp4142;"*rst"
760 OUTPUT @Hp4142;"cn";V_ch
770 OUTPUT @Hp4142;"dz";V_ch

```

```

780 CALL Id_vd_graph1(Vd_begin,Vd_end,-Imax,Imax,Var_i,Var_j,Vp,Ip)
790 FOR Var1=1 TO 201
800 OUTPUT @Hp4142;"dv";V_ch,0,Vd(Var1),Id_comp2
810 OUTPUT @Hp4142;"ri";V_ch,0
820 OUTPUT @Hp4142;"mm";1,V_ch
830 OUTPUT @Hp4142;"fmt";1
840 OUTPUT @Hp4142;"xe"
850 ENTER @Hp4142;Id$
860 Data_id(Var_i,Var_j,Var1)=VAL(Id$[4,15])
870 Xx=Vd(Var1)
880 Yy=Data_id(Var_i,Var_j,Var1)
890 PLOT Xx,Yy
900 NEXT Var1
910 OUTPUT @Hp4142;"cl"
920 NEXT Var_j
930 NEXT Var_i
940 OUTPUT @Hp4142;"*RST"
950 Sweep_trig_end:!
960 GOTO Sweep_trig_end
970 !
980 !
990 Vp_imax:!
1000 CLEAR SCREEN
1010 KEY LABELS ON
1020 INPUT "Start Pulse Voltage=",Vp1
1021 INPUT "Stop Pulse Voltage=",Vp2
1023 INPUT "Loop times(During each loop Vp will changed a constant
value)=",N
1030 INPUT "I_range(-11=1n,-12=10n,-13=100n,-14=1u,-15=10u,-17=1m,-
19=100m)=",I_range2
1031 INPUT "Pulse width(0.01=1ms,0.05=50ms)=",Tp

```

```
1033 INPUT "Td(Time delay of pulse)=",Td
1034 INPUT "Pulse period{Max[0.01,2*(pulse width)] to 0.5,0}=",Pp
1040 SELECT I_range2
1050 CASE -11,-12
1060   Imax=1.E-9
1070 CASE -12
1080   Imax=1.E-8
1090 CASE -13
1100   Imax=1.E-7
1110 CASE -14
1120   Imax=1.E-6
1130 CASE -15
1140   Imax=1.E-5
1150 CASE -16
1160   Imax=1.E-4
1170 CASE -17
1180   Imax=1.E-3
1190 CASE -18
1200   Imax=1.E-2
1210 CASE ELSE
1220   Imax=1.E-1
1230 END SELECT
1240 Vp_imax_end:~
1250 GOTO Vp_imax_end
1260 ~
1270 ~
1290 Pulse:~
1300 ON KBD GOTO Pulse_end
1310 Vd_step=(Vd_end-Vd_begin)/100
1320 FOR Var1=1 TO Mode*100+1
1330 IF Var1>101 THEN
```

```

1340   Vd(Var1)=Vd_end-(Var1-101)*Vd_step
1350   ELSE
1360   Vd(Var1)=(Var1-1)*Vd_step+Vd_begin
1370   END IF
1380   NEXT Var1
1381   R=(Vp2-Vp1)/N
1390   GINIT
1400   GRAPHICS ON
1402   FOR W=0 TO N
1410   FOR Var_i=1 TO 1
1420   FOR Var_j=W+1 TO W+1
1421   Vp=Vp1+W*R
1430! Vp=Vp-SGN(Vp)*W*ABS(Vp)/N
1440   OUTPUT @Hp4142;"*rst"
1450   OUTPUT @Hp4142;"cn";V_ch
1460   OUTPUT @Hp4142;"dz";V_ch
1470   OUTPUT @Hp4142;"FL";0,V_ch      !OFF smu filter
1480   OUTPUT @Hp4142;"PV";V_ch,0,0,Vp,Id_comp1
1490   OUTPUT @Hp4142;"PT";Td,Tp,Pp
1500   OUTPUT @Hp4142;"RI";V_ch,I_range1
1510   OUTPUT @Hp4142;"MM";3,V_ch
1520   OUTPUT @Hp4142;"XE"
1530   ENTER @Hp4142;Id$
1540   Ip=VAL(Id$[4,15])
1550   CALL Id_vd_graph1(Vd_begin,Vd_end,-Imax,Imax,Var_i,Var_j,Vp,Ip)
1560   OUTPUT @Hp4142;"DZ";V_ch
1570   OUTPUT @Hp4142;"fl";1,V_ch
1580   OUTPUT
      @Hp4142;"wv";V_ch,Sweep_mode,0,Vd_begin,Vd_end,101,Id_comp2,.3
1581   OUTPUT @Hp4142;"wm";1,2
1590   OUTPUT @Hp4142;"mm";2,V_ch

```

```

1600 OUTPUT @Hp4142;"ri";V_ch,I_range2
1610 OUTPUT @Hp4142;"fmt";5
1620 OUTPUT @Hp4142;"xe"
1630 FOR Var1=1 TO (Mode*100+1)
1640   ENTER @Hp4142 USING "#,3A,12D,X";$$,Id(Var1)
1641   IF Id(Var1)>=Imax THEN
1642     Id(Var1)=Imax
1643   END IF
1650   Data_id(Var_i,Var_j,Var1)=Id(Var1)
1660   Xx=Vd(Var1)
1670   Yy=Data_id(Var_i,Var_j,Var1)
1680   PLOT Xx,Yy
1690   NEXT Var1
1700   OUTPUT @Hp4142;"cl"
1710   NEXT Var_j
1720   NEXT Var_i
1724   NEXT W
1730   OUTPUT @Hp4142;"*RST"
1740 Pulse_end:~
1750 GOTO Pulse_end
1751~
1752~
1753 Test:~
1754 CLEAR SCREEN
1755 KEY LABELS ON
1756 INPUT "Start test pulse voltage=",Stpv1
1757 INPUT "stop test pulse voltage=",Stpv2
1758 INPUT "Test route times=",Tt
1759 INPUT "I_range(-11=1n,-12=10n,-13=100n,-14=1u,-15=10u,-17=1m,-
      19=100m)=",I_range2
1760 INPUT "Pulse width(0.01=1ms,0.05=50ms)=",Tp

```

```
1761 INPUT "Td(time delay of pulse)=",Td
1762 INPUT "Pulse period{Max[0.01,2*(pulse width)] to 0.5,0}=",Pp
1763 INPUT "Vd_begin=",Vd_begin
1764 INPUT "Vd_end=",Vd_end
1766 SELECT Ir
1767   CASE -11,-12
1768     Imax=1.E-9
1769   CASE -12
1770     Imax=1.E-8
1771   CASE -13
1772     Imax=1.E-7
1773   CASE -14
1774     Imax=1.E-6
1775   CASE -15
1776     Imax=1.E-5
1777   CASE -16
1778     Imax=1.E-4
1779   CASE -17
1780     Imax=1.E-3
1781   CASE -18
1782     Imax=1.E-2
1783   CASE ELSE
1784     Imax=1.E-1
1785   END SELECT
1786 E=0
1788 ON KBD GOTO Test_end
1789 GINIT
1790 GRAPHICS ON
1791 FOR W=0 TO Tt
1792   FOR Var_i=1 TO 1
1793     FOR Var_j=W+1 TO W+1
```

```

1796 Vd_step=(Vd_end-Vd_begin)/100
1797 FOR Var1=1 TO 201
1798 IF Var1>101 THEN
1799   Vd(Var1)=Vd_end-(Var1-101)*Vd_step
1800 ELSE
1801   Vd(Var1)=(Var1-1)*Vd_step+Vd_begin
1802 END IF
1803 NEXT Var1
1804 Vp=E
1806 OUTPUT @Hp4142;"*rst"
1807 OUTPUT @Hp4142;"cn";V_ch
1808 OUTPUT @Hp4142;"dz";V_ch
1809 OUTPUT @Hp4142;"fl";0,V_ch
1810 OUTPUT @Hp4142;"pv";V_ch,0,0,Vp,Id_comp1
1811 OUTPUT @Hp4142;"pt";Td,Tp,Pp
1812 OUTPUT @Hp4142;"ri";V_ch,I_range1
1813 OUTPUT @Hp4142;"mm";3,V_ch
1814 OUTPUT @Hp4142;"xe"
1815 ENTER @Hp4142;Id$
1816 Ip=VAL(Id$[4,15])
1817 CALL Id_vd_graph1(Vd_begin,Vd_end,-Imax,Imax,Var_i,Var_j,Vp,Ip)
1818 OUTPUT @Hp4142;"dz";V_ch
1819 OUTPUT @Hp4142;"fl";1,V_ch
1820 OUTPUT
      @Hp4142;"wv";V_ch,Sweep_mode,0,Vd_begin,Vd_end,101,Id_comp2,.3
1821 OUTPUT @Hp4142;"wm";1,2
1823 OUTPUT @Hp4142;"mm";2,V_ch
1824 OUTPUT @Hp4142;"ri";V_ch,I_range2
1825 OUTPUT @Hp4142;"fmt";5
1826 OUTPUT @Hp4142;"xe"
1827 FOR Var1=1 TO Mode*100+1

```

```

1828 ENTER @Hp4142 USING "#,3A,12D,X";$$,Id(Var1)
1829 IF Id(Var1)>=Imax THEN
1830   Id(Var1)=Imax
1831 END IF
1832 Data_id(Var_i,Var_j,Var1)=Id(Var1)
1833 Xx=Vd(Var1)
1834 Yy=Data_id(Var_i,Var_j,Var1)
1835 PLOT Xx,Yy
1836 NEXT Var1
1837 OUTPUT @Hp4142;"cl"
1838 NEXT Var_j
1839 NEXT Var_i
1840! Q=Vd_begin
1841! Vd_begin=Vd_end
1842! Vd_end=Q
1843 E=Stpv1+(Stpv2-Stpv1)*(W+1)/Tt
1844! Stpv2=Stpv1
1845! Stpv1=E
1846 NEXT W
1847 OUTPUT @Hp4142;"*rst"
1848 Test_end:~
1849 GOTO Test_end
1850!
1851!
1852 Save_data:~
1853 PRINT "saving data, wait....."
1854 MASS STORAGE IS "c:\hpbasic\mem_data"
1855 On_error: ~
1856 ON ERROR GOTO Off_error
1857 I=I+1
1858 Memory$="mem"&VAL$(I)&".dat"

```

```
1859 CREATE Memory$,120
1860 GOTO Assign_part
1861 Off_error: !
1862 OFF ERROR
1870 Err=ERRN
1880 IF Err=54 THEN
1890 PRINT "file exist, change name"
1900 GOTO On_error
1910 END IF
1920 Assign_part: !
1930 ASSIGN @Data TO Memory$;FORMAT ON      !"c:\hpbasic\mosfet$"
1940 FOR Var_i=1 TO 5
1950   FOR Var_j=1 TO 16
1960    FOR Var_l=1 TO (Mode*100+1)
1970     OUTPUT @Data;Vd(Var_l),Data_id(Var_i,Var_j,Var_l)
1980    NEXT Var_l
1990   NEXT Var_j
2000  NEXT Var_i
2010 MASS STORAGE IS "c:\hpbasic\mem_pro"
2020 PRINT "data saved to hd"
2030 ASSIGN @Data TO *
2040 Save_data_end: !
2050 GOTO Save_data_end
2060 !
2070 !
2080 Load_data: !
2090 CLEAR SCREEN
2100 MASS STORAGE IS "c:\hpbasic\mem_data"
2110 PRINT TABXY(4,5);CHR$(136)&"Do you want to see the data in the
      memory or in the disk?"
```

```

2120 PRINT TABXY(4,6);CHR$(137)&"If the data in memory,type 1;If the data
      in th disk, type 2"
2130 INPUT Sel_m_d
2140 SELECT Sel_m_d
2150 CASE 1
2160 GOTO Direct_draw
2170 CASE 2
2180 INPUT "Please input the name of the file",Id$
2190 ASSIGN @Data TO Id$;FORMAT ON
2200 FOR Var_i=1 TO 5
2210  FOR Var_j=1 TO 16
2220   FOR Var1=1 TO (Mode*100+1)
2230    ENTER @Data;Vd(Var1),Data_id(Var_i,Var_j,Var1)
2240   NEXT Var1
2250  NEXT Var_j
2260 NEXT Var_i
2270 ASSIGN @Data TO *
2280 END SELECT
2281!
2282!
2290 Direct_draw: !
2300 !GRAPHIC
2310 !PROGRAMMED BY WEI ZHANG,OCT.25,1995
2320 GINIT
2330 GRAPHICS ON
2340 CLEAR SCREEN
2350 FOR Var1=1 TO (Mode*100+1)
2360 IF Largest<Data_id(Xar_i,Yar_j,Var1) THEN
2370  Largest=Data_id(Xar_i,Yar_j,Var1)
2380 END IF
2390 IF Smallest>Data_id(Xar_i,Yar_j,Var1) THEN

```

```
2400  Smallest=Data_id(Xar_i,Yar_j,Var1)
2410  END IF
2420  NEXT Var1
2430  CALL
      Id_vd_graph(Vd(1),Vd(101),Smallest,Largest,15,15,.7,Xar_i,Yar_j,"Vd(V)","
      I(A)")
2440  FOR Var1=1 TO (Mode*100+1)
2450   Xx=Vd(Var1)
2460   Yy=Data_id(Xar_i,Yar_j,Var1)
2470   PLOT Xx,Yy
2480  NEXT Var1
2490  MASS STORAGE IS "c:\hpbasic\mem_pro"
2500  KEY LABELS ON
2510  Yar_j=Yar_j+1
2520  IF Yar_j>16 THEN
2530   Yar_j=1
2540   Xar_i=Var_i+1
2550  END IF
2560  ON KBD GOTO Direct_draw
2570  Load_data_end: !
2580  GOTO Load_data_end
2581 !
2582 !
2590  Show_c: !
2600  Row_begin=Xar_i
2610  Row_end=Xar_i
2620  Col_begin=Yar_j
2630  Col_end=Yar_j
2640  PRINT "saving data, wait....."
2650  MASS STORAGE IS "c:\hpbasic\mem_data"
2660  On_error1: !
```

```
2670 ON ERROR GOTO Off_error1
2680 I=I+1
2690 Memory$="sel"&VAL$(I)&".dat"
2700 CREATE Memory$,120
2710 GOTO Assign_part1
2720 Off_error1: !
2730 OFF ERROR
2740 Err=ERRN
2750 IF Err=54 THEN
2760 PRINT "file exist, change name"
2770 GOTO On_error1
2780 END IF
2790 Assign_part1: !
2800 ASSIGN @Data TO Memory$;FORMAT ON    !"c:\hpbasic\mosfet$"
2810 FOR Var_i=Row_begin TO Row_end
2820 FOR Var_j=Col_begin TO Col_end
2830 FOR Var1=1 TO (Mode*100+1)
2840 OUTPUT @Data;Vd(Var1),Data_id(Var_i,Var_j,Var1)
2850 NEXT Var1
2860 NEXT Var_j
2870 NEXT Var_i
2880 MASS STORAGE IS "c:\hpbasic\mem_pro"
2890 PRINT "data saved to hd"
2900 ASSIGN @Data TO *
2910 Show_c_end: !
2920 GOTO Show_c_end
2921!
2922!
2930 Reset_i: !
2940 CLEAR SCREEN
2950 KEY LABELS PEN 1
```

```

2960 USER 2 KEYS
2970 KEY LABELS ON
2980 DELSUB Id_vd_graph1 TO END
2990 OUTPUT @Hp4142;"*rst"
3000! OUTPUT @Hp3488;"creset 1,2,3,4"
3010 OUTPUT KBD;CHR$(255)&"!SCRATCH"&" COM"&CHR$(255)&"E";
3020 END
3610 SUB Row_col(Row_begin,Col_begin)
3740! Vs1_ch=14
3750! Vs2_ch=24
3755! ASSIGN @Hp4142 TO 717
3765!ASSIGN @Hp3488 TO 709
3820 !INPUT "Please input the number of beginning row=?",Row_begin
3821 !INPUT "Please input the number of beginning col=?",Col_begin
3940! OUTPUT @Hp3488;"creset 1,2,3,4"
3950! OUTPUT @Hp4142;"*rst"
3960! OUTPUT @Hp4142;"cn";Vs1_ch,Vs2_ch
4010! OUTPUT @Hp3488;"slist
      100,101,102,103,200,201,202,203,300,301,302,303,400,401,402,403"
4020! OUTPUT @Hp4142;"dv";Vs1_ch,12,4.2      !EN signal 0
4030! OUTPUT @Hp4142;"DV";Vs2_ch,12,4.2
4031! OUTPUT @Hp4142;"dZ";Vs2_ch      !clock signal
4040! FOR Iii=1 TO Row_begin-1
4041! OUTPUT @Hp3488;"step"
4042! NEXT Iii
4050! OUTPUT @Hp3488;"step"
4060! OUTPUT @Hp4142;"dZ";Vs1_ch      !EN signal 1
4070! IF I<=4 THEN
4080! OUTPUT @Hp3488;"Cmon 1"
4090! END IF
4100! IF I>4 AND I<=8 THEN

```

```

4110! OUTPUT @Hp3488;"cmon 2"
4120! END IF
4130! IF I>8 AND I<=12 THEN
4140! OUTPUT @Hp3488;"Cmon 3"
4150! END IF
4160! IF I>12 THEN
4170! OUTPUT @Hp3488;"cmon 4"
4180! END IF
4190! PAUSE
4192! FOR J=1 TO Col_begin-1
4200!  OUTPUT @Hp4142;"dV";Vs2_ch,12,4.2
4470!  OUTPUT @Hp4142;"dZ";Vs2_ch      !clock signal
4480! NEXT J
4550 SUBEND

810 SUB Id_vd_graph1(X_min,X_max,Y_min,Y_max,Ii,Jj,Vp,Tp)
820 !
830 Times=.5
840 INTEGER Pp
850 Pp=Jj MOD 4
860 CONTROL CRT,12;1      !CONTROL STATUS LINE SHOW
870 !PRINT CHR$(12)
880 !
890 Xmax=100*MAX(1,RATIO)
900 Ymax=100*MAX(1,1/RATIO)
910 SELECT Pp
920 CASE 1
930 W_x=0
940 W_y=Ymax/2
950 CASE 2

```

```
960 W_x=Xmax/2
970 W_y=Ymax/2
980 CASE 3
990 W_x=0
1000 W_y=0
1010 CASE ELSE
1020 W_x=Xmax/2
1030 W_y=0
1040 END SELECT
1050 VIEWPORT W_x,W_x+Times*Xmax,W_y,W_y+Times*Ymax
1060 WINDOW 0,Xmax,0,Ymax
1070 !
1080 AREA PEN 0
1090 !AREA COLOR .2,.3,.1
1100 MOVE 0,0
1110 RECTANGLE Xmax,Ymax,FILL
1120 LONG 6
1130 MOVE Xmax/2,Ymax
1140 PEN 1
1150 CSIZE 6*Times
1160 LABEL "E_Pulse I-V Curve"&VAL$(Vp)&","&VAL$(Tp)
1170 DEG
1180 LDIR 90
1190 CSIZE Times*4.5
1200 MOVE 0,Ymax/2
1210 LABEL "I(A)"
1220 LONG 4
1230 LDIR 0
1240 MOVE Xmax/2,0
1250 LABEL "V(V)"
1260 !
```

```

1270 VIEWPORT
      W_x+.16*Times*Xmax,W_x+.9*Times*Xmax,W_y+.15*Times*Ymax,W_y
      +.9*Times*Ymax !ALOW TO ADJUST RITIO
1280 LINE TYPE 1
1290 PEN 6
1300 GRID (Xmax)/10,10
1310 LINE TYPE 1
1320 PEN 10
1330 !
1340 !FRAME
1350 WINDOW X_min,X_max,Y_min,Y_max !CURVE AREA
1360 AXES (X_min-X_max)/10,(Y_max-Y_min)/10,X_min,Y_min,5,5,Times*5
1370 AXES (X_min-X_max)/10,(Y_max-Y_min)/10,X_max,Y_max,5,5,Times*5
1380 CLIP OFF !SET CLIP BOUNDARIES TO HARD CLIP BOUNDARY
1390 CSIZE Times*4,.5
1400 LORG 6
1410 PEN 4
1420 FOR I=X_min TO X_max STEP (X_max-X_min)/2
1430  MOVE I,Y_min
1440  LABEL I
1450 NEXT I
1460 CSIZE Times*3.8,.5
1470 LORG 8
1480 FOR I=Y_min TO Y_max STEP (Y_max-Y_min)/2
1490  MOVE X_min,I
1500  LABEL USING "#,MD.DE";I
1510 NEXT I
1520 !MOVE 0,0
1530 !AREA PEN 0
1540 !RECTANGLE 20,20,FILL
1550 CLIP ON

```

```
1560 !
1570 SUBEND
1580 SUB
      Id_vd_graph(X_min,X_max,Y_min,Y_max,W_x,W_y,Times,Ii,Jj,X_indicato
      r$,Y_indicator$)
1590 !
1600 CONTROL CRT,12;1      !CONTROL STATUS LINE SHOW
1610 !PRINT CHR$(12)
1620 !
1630 Xmax=100*MAX(1,RATIO)
1640 Ymax=100*MAX(1,1/RATIO)
1650 VIEWPORT W_x,W_x+Times*Xmax,W_y,W_y+Times*Ymax
1660 WINDOW 0,Xmax,0,Ymax
1670 !
1680 AREA PEN 0
1690 MOVE 0,0
1700 RECTANGLE Xmax,Ymax,FILL
1710 AREA PEN 1
1720 LORG 6
1730 MOVE Xmax/2,Ymax
1740 PEN 1
1750 CSIZE 6*Times
1760 LABEL "memory matrix cell OF "&VAL$(Ii)&","&VAL$(Jj)
1770 DEG
1780 LDIR 90
1790 CSIZE Times*4.5
1800 MOVE 0,Ymax/2
1810 LABEL Y_indicator$
1820 LORG 4
1830 LDIR 0
1840 MOVE Xmax/2,0
```

```

1850 LABEL X_indicator$
1860 !
1870 VIEWPORT
      W_x+.16*Times*Xmax,W_x+.9*Times*Xmax,W_y+.15*Times*Ymax,W_y
      +.9*Times*Ymax !ALOW TO ADJUST RITIO
1880 LINE TYPE 4
1890 PEN 6
1900 GRID (Xmax)/10,10
1910 LINE TYPE 1
1920 PEN 10
1930 !
1940 !FRAME
1950 WINDOW X_min,X_max,Y_min,Y_max !CURVE AREA
1960 AXES (X_min-X_max)/10,(Y_max-Y_min)/10,X_min,Y_min,5,5,Times*5
1970 AXES (X_min-X_max)/10,(Y_max-Y_min)/10,X_max,Y_max,5,5,Times*5
1980 CLIP OFF !SET CLIP BOUNDARIES TO HARD CLIP BOUNDARY
1990 CSIZE Times*4,.5
2000 LORG 6
2010 PEN 4
2020 FOR I=X_min TO X_max STEP (X_max-X_min)/2
2030 MOVE I,Y_min
2040 LABEL I
2050 NEXT I
2060 CSIZE Times*3.8,.5
2070 LORG 8
2080 FOR I=Y_min TO Y_max STEP (Y_max-Y_min)/2
2090 MOVE X_min,I
2100 LABEL USING "#,MD.DE";I
2110 NEXT I
2120 CLIP ON
2130 !

```

```

2140 SUBEND
2150 SUB Dump_s
2160 KEY LABELS OFF
2170 RUNLIGHT OFF
2180 DUMP DEVICE IS 10
2190 DUMP GRAPHICS
2200 SUBEND

```

A.5 HP-Basic programs for LCR measurement

```

5 DIM
  N(6,20),A(600),B(600),Z(600),O(600),X(600),Y(600),A$(25),S$(5)[8],Ss$(40]
10 GOTO 15900
20 CLEAR SCREEN
30 REM **MEAS SETUP**
40 REMOTE 717
50 LOADSUB Mset FROM "SUB_LIBN:;701"
60 CALL Msets
70 DELSUB Msett
240 REM **MEAS LOOP & OUTPUT**
250 PRINT "ENTER THE LOW FREQ"
260 INPUT L
270 PRINT "LOW FREQ=";L
280 PRINT "ENTER THE HIGH FREQ"
290 INPUT H
300 PRINT "HIGH FREQ=";H
310 L1=INT(LGT(L))
320 H1=INT(LGT(H))
330 IF 10^H1<H THEN H1=H1+1
340 IF H1>6 THEN H1=6
350 PRINT "PLEASE ENTER THE BIAS VOLTAGE (V)"

```

```

351 PRINT "IF YOU WANT TO MAKE MORE THAN ONE MEASUREMENT"
352 PRINT "EACH BIAS MUST BE SEPERATED BY A SPACE, Ex.'-2 -1.5 0 1
      2""
353 !IUTPUT 717;"VOLT 30MV"
355 GOSUB 7000
359 FOR M=0 TO U-1
361 PRINT "BIAS=";S$(M);"(V)"
362 A$="BIAS:VOLT "&S$(M)
364 OUTPUT 717;A$
365 K=0
370 FOR I=L1 TO H1-1
380 FOR J=0 TO 19
390 N(I,J)=INT(10^(I+J/20)))
400 IF N(I,J)<20 THEN N(I,J)=20
410 A$="FREQ "&VAL$(N(I,J))&"Hz"
420 PRINT A$
430 OUTPUT 717;"DISP:PAGE MEAS"
440 OUTPUT 717;A$
450 OUTPUT 717;"*TRG"
460 ENTER 717;A(K),B(K)
461 OUTPUT 717;"FREQ?"
462 ENTER 717;C"
463 X(K)=LGT(C)"
470 PRINT K,A(K),B(K)
480 IF N(I,J)=10^H1 THEN GOTO 540
490 K=K+1
500 NEXT J
510 NEXT I
520 N(I,J)=10^H1
530 GOTO 410
540 LOCAL 717

```

```

541 OUTPUT 717;"BIAS:STAT 0"
543 Tt$=S$(M)
544 GOSUB 10113
550 GOSUB 8000
560 GOSUB 5000
561 PEN 2
570 GOSUB 5800
580 GOSUB 5650
581 INPUT "DO YOU WANT TO SEE ANOTHER CURVE? (Y/N)",IS
582 IF IS="Y" THEN
583 GOSUB 1012
584 GOSUB 8000
585 GOSUB 5000
586 PEN 2
587 GOSUB 5800
588 GOSUB 5650
589 END IF
599 GOSUB 6700
700 NEXT M
750 GOTO 15900
1590 CLEAR SCREEN
1591 PRINT " *****"
1600 PRINT "*****"
1610 PRINT "***** THIS HEWLETT PACKARD 4284A LCR
          MEASUREMENT SYSTEM *****"
1611 PRINT "***** IS DEVELOPED BY Mr.Zhijia LI (JULY 1991) *****"
1612 PRINT "***** IS MODIFIED BY Mr.Jianqin ZHOU (APRIL 1997) *****"
1613 PRINT "***** IS COMPLETED BY Mr.Zhongwei PAN (MAY 1998) *****"
1630 PRINT "*****"
1631 PRINT "*****"
1640 PRINT "

```

```

1650 PRINT "PLEASE SELECT X-AXIS VARIABLE:"
1660 PRINT "ENTER 1 FOR FREQUENCY    ENTER 2 FOR BIAS VOLTAGE"
1661 PRINT "ENTER 0 TO EXIT"
1662 PRINT "
1670 PRINT "PLEASE CHOOSE AN MEASUREMENT FUNCTION:"
1671 PRINT "ENTER 1  TO CHOOSE CPD;    ENTER 2  TO CHOOSE CPQ"
1672 PRINT "ENTER 3  TO CHOOSE CPG;    ENTER 4  TO CHOOSE CPRP"
1673 PRINT "ENTER 5  TO CHOOSE CSD;    ENTER 6  TO CHOOSE CSQ"
1674 PRINT "ENTER 7  TO CHOOSE CSRS;   ENTER 8  TO CHOOSE LPQ"
1675 PRINT "ENTER 9  TO CHOOSE LPD;    ENTER 10 TO CHOOSE LPG"
1676 PRINT "ENTER 11 TO CHOOSE LPRP;   ENTER 12 TO CHOOSE LSD"
1677 PRINT "ENTER 13 TO CHOOSE LSQ;    ENTER 14 TO CHOOSE LSRS"
1678 PRINT "ENTER 15 TO CHOOSE RX;     ENTER 16 TO CHOOSE ZTD"
1679 PRINT "ENTER 17 TO CHOOSE ZTR;    ENTER 18 TO CHOOSE GB"
1680 PRINT "ENTER 19 TO CHOOSE YTD;    ENTER 20 TO CHOOSE YTR"
1682 PRINT "ENTER 0  TO EXIT"
1683 PRINT "
1692 INPUT "YOUR X-AXIS VARIABLE CHOICE IS",C$
1711 INPUT "YOUR MEASUREMENT FUNCTION CHOICE IS",F$
1721 GOSUB 9992
1730 IF C$="1" THEN GOTO 1795
1740 IF C$="2" THEN GOTO 1900
1750 IF C$="0" THEN GOTO 10128
1760 GOTO 1590
1770!GINIT
1780!PLOTTER IS CRT,"INTERNAL"
1790!GCLEAR
1795 GOSUB 8200
1830 IF B$="1" THEN GOTO 20
1840 IF B$="2" THEN GOTO 4000
1850 GOTO 1795

```

```
1900 GOSUB 8200
1970 IF B$="1" THEN GOTO 2000
1980 IF B$="2" THEN GOTO 4000
1990 GOTO 1900
2000 CLEAR SCREEN
2010 REM **MEAS SETUP**
2020 REMOTE 717
2030 LOADSUB Mset FROM "SUB_LIBN:;701"
2040 CALL Mset
2050 DELSUB Mset
2210 REM **MEAS LOOP & OUTPUT**
2270 PRINT "ENTER THE LOW BIAS(V)"
2280 INPUT L1
2290 PRINT "LOW BIAS=";L1;"(V)"
2300 PRINT "ENTER THE HIGH BIAS(V)"
2310 INPUT H1
2320 PRINT "HIGH BIAS=";H1;"(V)"
2325 PRINT "ENTER THE BIAS STEP"
2330 INPUT W
2331 PRINT "ENTER THE MEASUREMENT TIMES"
2332 INPUT S
2335 IF -40>L1 THEN L1=-40
2340 IF 40<H1 THEN H1=40
2342 CLEAR SCREEN
2345 PRINT "ENTER THE FREQUENCY"
2346 PRINT "IF YOU WANT TO MAKE MORE THAN ONE
      MEASUREMENT"
2347 PRINT "EACH BIAS MUST SEPERATED BY A SPACE, Ex.'1E2 1E3
      1E4'"
2348 GOSUB 7000
2354 FOR M=0 TO U-1
```

```
2355 PRINT "FREQ=";S$(M);"(Hz)"
2356 A$="FREQ "&S$(M)&"Hz"
2357 OUTPUT 717;A$
2358 FOR J=1 TO S$
2360 K=0
2361 !OUTPUT 717;"VOLT 30MV"
2370 FOR I=L1 TO H1 STEP W
2371 IF ABS(I)<.001 THEN I=0
2380 A$="BIAS:VOLT "&VAL$(I)
2390 PRINT A$
2400 OUTPUT 717;"DISP:PAGE MEAS"
2410 OUTPUT 717;A$
2420 OUTPUT 717;"*TRG"
2425 !WAIT 1
2430 ENTER 717;O(K),Z(K)
2431 A(K)=A(K)+O(K)
2433 B(K)=B(K)+Z(K)
2434 X(K)=L1+K*W
2435 PRNT K,X(K),A(K),B(K)
2440 K=K+1
2450 NEXT I
2451 NEXT J
2460 LOCAL 717
2461 OUTPUT 717;"BIAS:STAT 0"
2463 Tt$=S$(M)
2464 K=K-1
2465 GOSUB 10113
2470 GOSUB 8000
2480 GOSUB 6000
2481 PEN 2
2490 GOSUB 5800
```

```
2500 GOSUB 5650
2501 INPUT "DO YOU WANT TO SEE ANOTHER CURVE? (Y/N)",IS
2502 IF IS="Y" THEN
2503   GOSUB 10121
2504   GOSUB 8000
2505   GOSUB 6000
2506   PEN 2
2507   GOSUB 5800
2508   GOSUB 5650
2509 END IF
2510 GOSUB 6700
2520 NEXT M
2550 GOTO 1590
4000 REM ** LOAD DATA **
4010 PRINT "PLEASE ENTER THE FILE NAME(S)"
4020 PRINT "EACH NAME MUST BE SEPERATED BY A SPACE"
4030 GOSUB 7000
4031 H1=0
4032 L1=1.E+6
4033 !Y1=0
4034 !Y2=1.E+6
4040 MASS STORAGE IS ":",704"
4050 FOR M=0 TO U-1
4060 ASSIGN @F_1 TO S$(M)
4061 ENTER @F_1;M$,Tt$
4070 ENTER @F_1;Hh1,L11,Yy1,Yy2,K
4071 FOR I=0 TO K
4072  ENTER @F_1;X(I),A(I),B(I)
4073 NEXT I
4080 ASSIGN @F_1 TO *
4090 H1=MAX(H1,Hh1)
```

```
4100 L1=MIN(L1,L11)
4110 !Y1=MAX(Y1,Yy1)
4120 !Y2=MIN(Y2,Yy2)
4130 NEXT M
4131 GOSUB 10113
4132 GOSUB 8000
4140 MASS STORAGE IS ":",701"
4141 !S=(Y1-Y2)/5
4145 GINIT
4150 IF C$="1" THEN
4151   GOSUB 5000
4152   PEN 2
4154   GOSUB 5800
4155   GOSUB 7500
4157   INPUT "DO YOU WANT TO SEE ANOTHER CURVE? (Y/N)",IS
4158   IF IS="Y" THEN
4159     GOSUB 10121
4160     GOSUB 8000
4161     GOSUB 5000
4162     PEN 2
4164     GOSUB 5800
4165     GOSUB 7500
4167   END IF
4168 END IF
4169 IF C$="2" THEN
4170   GOSUB 6000
4171   PEN 2
4173   GOSUB 5800
4174   GOSUB 7500
4176   INPUT "DO YOU WANT TO SEE ANOTHER CURVE? (Y/N)",IS
4177   IF IS="Y" THEN
```

```

4178   GOSUB 10121
4179   GOSUB 8000
4180   GOSUB 6000
4181   PEN 2
4183   GOSUB 5800
4184   GOSUB 7500
4186   END IF
4187 END IF
4188 !GOSUB 4800
4189 !GOSUB 7500
4190 PRINT "PRESS ENTER KAY RETURN TO MAIN MENU"
4195 INPUT W$
4200! IF W$<>" " THEN GOTO 4190
4210 PLOTTER IS CRT,"INTERNAL"
4220 GCLEAR
4230 CLEAR SCREEN
4240 GOTO 1590
4800 REM ** LOAD DATA **
4806 FOR M=0 TO U-1
4807 MASS STORAGE IS ":",704"
4809 ASSIGN @F_1 TO S$(M)
4810 ENTER @F_1;M$,Tt$
4811 ENTER @F_1;Hh1,L11,Yy1,Yy2,K
4812 FOR I=0 TO K
4813 ENTER @F_1;X(I),A(I),B(I)
4814 NEXT I
4815 MASS STORAGE IS ":",701"
4816 Lt=1+M
4818 LINE TYPE Lt
4819 IF Lt=2 THEN LINE TYPE 8
4820 PEN 2+M

```

```

4825 GOSUB 5800
4835 NEXT M
4845 RETURN
5000 REM ** ?-F FRAME ** _____
5010 T$=Yt$&"-Freq."
5020 Y$=Yt$
5030 X$="FREQUENCY(Hz)"
5040 Z$="BIAS(V)"
5180 LOADSUB Grphset FROM "SUB_LIBN:,701"
5190 CALL Grphset(T$,X$,Y$,L1,H1,Y1,Y2,S)
5200 DELSUB Grphset
5480 AXES 1,S,L1,Y2,1,5,3
5490 CLIP OFF
5500 LORG 6
5510 CSIZE 2.5,.5
5520 FOR I=L1 TO H1
5530 MOVE I,Y2-S/20
5540 LABEL "1E"&VAL$(I)
5550 NEXT I
5551 MOVE H1,Y2-.7*S
5560 LORG 8
5565 LABEL "Semiconductor Lab, EE Dept. of CCNY"
5570 FOR I=0 TO 5
5580 MOVE L1-(H1-L1)/80,Y2+I*S
5590 LABEL VAL$(Y2+I*S)
5600 NEXT I
5601 MOVE .85*(H1-L1)+L1,Y1+.7*S
5602 LORG 6
5603 LABEL Z$
5610 RETURN
5650 REM ** HARD COPY OPTION ** _____

```

```
5660 PRINT "DO YOU WANT A HARD COPY? (Y/N)"
5670 INPUT W$
5680 CLEAR SCREEN
5690 IF W$ <> "Y" THEN GOTO 5740
5700 GINIT
5710 PLOTTER IS 705,"HPGL"
5720 GRAPHICS ON
5730 IF C$="1" THEN GOSUB 5000
5731 IF C$="2" THEN GOSUB 6000
5733 GOSUB 5800
5734 GOTO 5660
5740 PLOTTER IS CRT,"INTERNAL"
5750 GCLEAR
5760 CLEAR SCREEN
5770 RETURN
5800 REM ** PLOTTING **
5810 FOR I=0 TO K
5840 PLOT X(I),Y(I)
5850 NEXT I
5851 PENUP
5852  $X_x = (.78 + .02 * M) * (H1 - L1) + L1$ 
5853  $Y_y = Y1 + (.50 - .11 * M) * S$ 
5854 MOVE Xx,Yy
5855 RPLOT .06*(H1-L1),0,-1
5856 RPLOT .07*(H1-L1),0,-2
5858 LINE TYPE 1
5859 LORG 2
5860 CSIZE 2
5862 LABEL Tt$
5863 RETURN
6000 REM ** ?-V FRAME **
```

```

6005 T$=Yt$&"-Volt."
6010 X$="BIAS(V)"
6020 Y$=Yt$
6030 Z$="FREQUENCY(Hz)"
6160 LOADSUB Grphset FROM "SUB_LIBN:,701"
6170 CALL Grphset(T$,X$,Y$,L1,H1,Y1,Y2,S)
6180 DELSUB Grphset
6410 AXS .05*(H1-L1),S,L1,Y2,2,5,3
6420 CLIP OFF
6430 LORG 6
6440 CSIZE 2.5,.5
6450 FOR I=L1 TO H1 STEP (H1-L1)*.1
6455 IF ABS(I)<.0001 THEN I=0
6460 MOVE I,Y2-S/20
6470 LABEL I
6480 NEXT I
6490 LORG 8
6491 MOVE H1,Y2-.7*S
6495 LABEL "Semiconductor Lab, EE Dept. of CCNY"
6500 FOR I=0 TO 5
6510 MOVE L1-(H1-L1)/80,Y2+I*S
6520 LABEL VAL$(Y2+I*S)
6530 NEXT I
6531 MOVE .85*(H1-L1)+L1,.7*S+Y1
6532 LORG 6
6534 LABEL Z$
6540 RETURN
6700 REM ** STORE DATA **
6705 PRINT "DO YOU WANT TO STORE THE DATA? (Y/N)"
6710 INPUT V$
6720 IF V$<>"Y" THEN GOTO 6760

```

```

6730 LOADSUB Sdata FROM "SUB_LIBN:,701"
6740 CALL Sdata(M$,Tt$,H1,L1,Y1,Y2,K,X(*),A(*),B(*))
6750 DELSUB Sdata
6760 RETURN

7000 REM ** READ STRINGS ** _____
7010 INPUT Ss$
7011 CLEAR SCREEN
7014 U=0
7015 Ss$=Ss$&" "
7016 REPEAT
7017 P=POS(Ss$," ")
7018 IF P<=1 THEN
7019   S$(U)=Ss$
7020   GOTO 7028
7021 END IF
7022 S$(U)=Ss$[1,P-1]
7023 Ss$=Ss$[P+1]
7024 U=U+1
7025 UNTIL LEN(Ss$)=1
7028 RETURN

7500 REM **HARD COPY OPTION 2 ** _____
7510 PRINT "DO YOU WANT A HARD COPY? (Y/N)"
7520 INPUT W$
7521 CLEAR SCREEN
7530 IF W$<>"Y" THEN RETURN
7535 GINIT
7540 PLOTTER IS 705,"HPGL"
7560 GRAPHICS ON
7570 IF C$="1" THEN GOSUB 5000
7580 IF C$="2" THEN GOSUB 6000
7590 GOSUB 4800

```

```
7600 GOTO 7510
8000 REM **DATA PROCESS**
8010 M1=Y(0)
8020 M2=Y(0)
8030 FOR I=0 TO K-1
8040 M1=MAX(Y(I),M1)
8050 M2=MIN(Y(I),M2)
8060 NEXT I
8070 IF M2<10^(-6) THEN GOTO 8110
8080 M$=" "
8081 E=1
8090 !E=10^6
8100 GOTO 8112
8110 M$=" "
8111 E=1 !E=10^12
8112 FOR I=0 TO K
8115 Y(I)=Y(I)*E
8124 NEXT I
8130 N1=M1*E
8140 N2=M2*E
8150 PRINT "Ymax=";N1;M$
8160 PRINT "Ymin=";N2;M$
8165 PRINT "PLEASE ENTER THE Y SCALE"
8170 INPUT "Ytop=",Y1
8175 INPUT "Ybottom=",Y2
8176 S=(Y1-Y2)/5
8177 CLEAR SCREEN
8178 GINIT
8179 PLOTTER IS CRT,"INTERNAL"
8180 RETURN
8190 REM ** MENU **
```

```
8200 CLEAR SCREEN
8210 PRINT
8220 PRINT
8230 PRINT
8240 PRINT "ENTER 1 TO DO MEASUREMENT"
8250 PRINT "ENTER 2 TO RETRIEVE DATA"
8260 INPUT "YOUR CHOICE IS",B$
8265 CLEAR SCREEN
8270 RETURN
9992 IF F$="1" THEN
9993  OUTPUT 717;"FUNC:IMP CPD"
9994  P1$="Cp(F)"
9995  P2$="D"
9996 END IF
9998 IF F$="2" THEN
9999  OUTPUT 717;"FUNC:IMP CPQ"
10000 P1$="Cp(F)"
10001 P2$="Q"
10002 END IF
10004 IF F$="3" THEN
10005  OUTPUT 717;"FUNC:IMP CPG"
10006  P1$="Cp(F)"
10007  P2$="Cond.(S)"
10008 END IF
10010 IF F$="4" THEN
10011  OUTPUT 717;"FUNC:IMP CPRP"
10012  P1$="Cp(F)"
10013  P2$="Rp(ohm)"
10014 END IF
10016 IF F$="5" THEN
10017  OUTPUT 717;"FUNC:IMP CSD"
```

```
10018 P1$="Cs(F)"
10019 P2$="D"
10020 END IF
10022 IF F$="6" THEN
10023  OUTPUT 717;"FUNC:IMP CSQ"
10024  P1$="Cs(F)"
10025  P2$="Q"
10026 END IF
10028 IF F$="7" THEN
10029  OUTPUT 717;"FUNC:IMP CSRS"
10030  P1$="Cs(F)"
10031  P2$="Rs(ohm)"
10032 END IF
10034 IF F$="8" THEN
10035  OUTPUT 717;"FUNC:IMP LPQ"
10036  P1$="Lp(H)"
10037  P2$="Q"
10038 END IF
10040 IF F$="9" THEN
10041  OUTPUT 717;"FUNC:IMP LPD"
10042  P1$="Lp(H)"
10043  P2$="D"
10044 END IF
10046 IF F$="10" THEN
10047  OUTPUT 717;"FUNC:IMP LPG"
10048  P1$="Lp(H)"
10049  P2$="Cond.(S)"
10050 END IF
10052 IF F$="11" THEN
10053  OUTPUT 717;"FUNC:IMP LPRP"
10054  P1$="Lp(H)"
```

```
10055 P2$="Rp(ohm)"
10056 END IF
10058 IF F$="12" THEN
10059  OUTPUT 717;"FUNC:IMP LSD"
10060  P1$="Ls(H)"
10061  P2$="D"
10062 END IF
10064 IF F$="13" THEN
10065  OUTPUT 717;"FUNC:IMP LSQ"
10066  P1$="Ls(H)"
10067  P2$="Q"
10068 END IF
10070 IF F$="14" THEN
10071  OUTPUT 717;"FUNC:IMP LSRS"
10072  P1$="Ls(H)"
10073  P2$="Rs(ohm)"
10074 END IF
10076 IF F$="15" THEN
10077  OUTPUT 717;"FUNC:IMP RX"
10078  P1$="R(ohm)"
10079  P2$="React.(ohm)"
10080 END IF
10082 IF F$="16" THEN
10083  OUTPUT 717;"FUNC:IMP ZTD"
10084  P1$="Imped.(ohm)"
10085  P2$="Phase(deg)"
10086 END IF
10088 IF F$="17" THEN
10089  OUTPUT 717;"FUNC:IMP ZTR"
10090  P1$="Imped.(ohm)"
10091  P2$="Phase(rad)"
```

```
10092 END IF
10094 IF F$="18" THEN
10095   OUTPUT 717;"FUNC:IMP GB"
10096   P1$="Cond.(S)"
10097   P2$="Suscept.(S)"
10098 END IF
10100 IF F$="19" THEN
10101   OUTPUT 717;"FUNC:IMP YTD"
10102   P1$="Admitt.(S)"
10103   P2$="Phase(deg)"
10104 END IF
10106 IF F$="20" THEN
10107   OUTPUT 717;"FUNC:IMP YTR"
10108   P1$="Admitt.(S)"
10109   P2$="Phase(rad)"
10110 END IF
10112 RETURN
10113 Yt$=P1$
10115 FOR I=0 TO K
10116   Y(I)=A(I)
10118 NEXT I
10119 RETURN
10121 Yt$=P2$
10122 CLEAR SCREEN
10124 FOR I=0 TO K
10125   Y(I)=B(I)
10126 NEXT I
10127 RETURN
10128 CLEAR SCREEN
10129 OUTPUT 717;"BIAS:STAT 0"
10130 END
```

```

15740 SUB Sdata(M$,Tt$,H1,L1,Y1,Y2,K,X(*),A(*),B(*))
15750 CLEAR SCREEN
15760 PRINT "PLEASE ENTER THE FILE NAME"
15770 INPUT F$
15780 MASS STORAGE IS ":",704"
15790 CREATE ASCII F$,100
15800 ASSIGN @Path_1 TO F$
15810 OUTPUT @Path_1;M$,Tt$
15820 OUTPUT @Path_1;H1,L1,Y1,Y2,K
15821 FOR I=0 TO K
15830 OUTPUT @Path_1;X(I),A(I),B(I)
15840 NEXT I
15850 ASSIGN @Path_1 TO *
15860 MASS STORAGE IS ":",701"
15870 SUBEND
15880 REM _____
15930 REM ** LOAD DATA **

```

```

1  !SUBROUTINE FOR LCR PROGRAM
10  SUB Mset
20  !**MEASUREMENT PARAMETERS SETUP**
30  OUTPUT 717;"DISP:PAGE MSET"
40  !OUTPUT 717;"FUNC:IMP CPRP"
50  !OUTPUT 717;"VOLT 1V"
60  OUTPUT 717;"TRIG:SOUR BUS"
70  OUTPUT 717;"TRIG:DEL 0"
80  OUTPUT 717;"AMPL:ALC OFF"
90  OUTPUT 717;"OUTP:DC:ISOL OFF"
100 OUTPUT 717;"OUTP:HPOW ON"
110 OUTPUT 717;"FUNC:IMP:RANG:AUTO ON"

```

```

120 OUTPUT 717;"APER LONG,1"
121 OUTPUT 717;"VOLT 10MV"
130 OUTPUT 717;"FUNC:SMON:VAC ON"
140 OUTPUT 717;"FUNC:SMON:IAC ON"
150 OUTPUT 717;"FUNC:DEV1:MODE OFF"
160 OUTPUT 717;"FUNC:DEV2:MODE OFF"
170 OUTPUT 717;"FUNC:DEV1:REF 0"
180 OUTPUT 717;"FUNC:DEV2:REF 0"
190 OUTPUT 717;"FORM ASCII"
200 OUTPUT 717;"INIT:CONT ON"
201 OUTPUT 717;"BIAS:STATE ON"
210 SUBEND
220 REM _____
300 SUB Grphset(T$,X$,Y$,L1,H1,Y1,Y2,S)
310 REM **GRAPHICS SETUP**
370 GRAPHICS ON
380 LORG 6
390 Xm=100*MAX(1,RATIO)
400 Ym=100*MAX(1,1/RATIO)
410 FOR I=-.3 TO .3 STEP .1
420 MOVE Xm/2+I,Ym
430 LABEL T$
440 NEXT I
450 DEG
460 LDIR 90
470 CSIZE 3.5
480 MOVE 0,Ym/2
490 LABEL Y$
500 LORG 4
510 LDIR 0
540 MOVE Xm/2,.07*Ym

```

```

550 LABEL X$
551 ! CSIZE 2$
560 ! MOVE .8*Xm,.95*Ym
570 ! LABEL Z$
580 VIEWPORT .12*Xm,.98*Xm,.15*Ym,.9*Ym
590 FRAME
600 WINDOW L1,H1,Y2,Y1
610 SUBEND
620 REM _____
700 REM ** STORE DATA **
710 SUB Sdata(M$,Tt$,H1,L1,Y1,Y2,K,X(*),A(*),B(*))
720 CLEAR SCREEN
730 PRINT "PLEASE ENTER THE FILE NAME"
740 INPUT F$
750 MASS STORAGE IS ":",704"
760 CREATE ASCII F$,100
770 ASSIGN @Path_1 TO F$
780 OUTPUT @Path_1;M$,Tt$
790 OUTPUT @Path_1;H1,L1,Y1,Y2,K
791 FOR I=0 TO K
800 OUTPUT @Path_1;X(I),A(I),B(I)
810 NEXT I
820 ASSIGN @Path_1 TO *
830 MASS STORAGE IS ":",701"
840 SUBEND
850 REM _____
900 REM ** LOAD DATA**
960 SUB Ldata(S$(*),M$,Tt$,K,X(*),A(*))
970 CLEAR SCREEN
1000 MASS STORAGE IS ":",704"
1010 ASSIGN @F_1 TO S$(M)

```

```

1020 ENTER @F_1;M$,Tt$
1030 ENTER @F_1;Hh1,L11,Yy1,Yy2,K
1031 FOR I=0 TO K
1040 ENTER @F_1;X(I),A(I)
1041 NEXT I
1050 ASSIGN @F_1 TO *
1060 MASS STORAGE IS ":",701"
1070 FOR I=0 TO K
1080 PRINT X(I),A(I)
1090 NEXT I
1100 SUBEND

```

A.6 Terminology

ACCESS TIME: The amount of time that nonvolatile memory takes to write data or to read it once the request has been received from the processor is called the access time. Typical access times vary from 9 nanoseconds to 70 nanoseconds, depending on the kind of NVM. Access time consists of latency and transfer time. Latency is the time to coordinate signal timing and refresh data after reading it.

AGEING: is in fact a less well-defined term generally indicating the degradation of the ferroelectric properties with time.

COERCIVE FIELD (E_c) is defined as the horizontal intercept of the hysteresis loop or the field at which the net polarization becomes zero. In a

single domain crystal, E_c can be interpreted as the field at which the polarization switches from one state to another. In a multi-domain crystal, however, E_c will lose its interpretation, as there is no single field at which all domains can switch.

Dynamic Random Access Memory (DRAM) uses a kind of capacitor that needs frequent power refreshing to retain its charge. Because reading a DRAM discharges its contents, a power refresh is required after each read. Apart from reading, just to maintain the charge that holds its content in place, DRAM must be refreshed about every 15 microseconds. DRAM is the least expensive kind of RAM.

Electrically Erasable Programmable Read-Only Memory [E²PROM (EEPROM)] is programmable by Fowler-Nordheim tunneling in which electrons tunnel through a thin dielectric to/from a floating gate and to/from a conducting channel. Unlike EPROM chips, E²PROMs do not need to be removed from the computer to be modified. However, an E²PROM chip has to be erased and reprogrammed in its entirety, not selectively. It also has a limited life – that is, the number of times it can be reprogrammed is limited to tens or hundreds of thousands of times. In an E²PROM that is frequently reprogrammed while the computer is in use, the life of the E²PROM can be an important design consideration.

ELECTRICAL FATIGUE is defined as the reduction of the switchable polarization with increasing number of switching cycles. This fatigue limits the endurance of the memory, i.e. the maximum number of read/write (=switching) cycles that can be applied to a memory element still allowing discrimination between the two memory states (i.e. polarization "up" or "down").

ENDURANCE: A measure of the number of programming/erase cycles that a programmable NRAM array can achieve while retaining data integrity (see data retention.) This should not be confused with the number of times that a system could program a byte in the nonvolatile memory device. 100,000-minimum guaranteed endurance cycles are the current industry requirement. In many cases, the customer will not need high endurance, but they will use endurance as a measure of device reliability.

FLASH: Flash memory (sometimes called "flash RAM") is a type of constantly-powered nonvolatile memory that can be erased and reprogrammed in units of memory called blocks. Flash memory gets its name because the microchip is organized so that a section of memory cells are erased in a single action or "flash." It is a special form of E²PROM which, unlike flash memory, is erased and rewritten at the byte level, which is slower than flash memory updating. Flash memory is often used

to hold control code such as the Basic Input/Output System (BIOS) in a personal computer. When BIOS needs to be changed (rewritten), the flash memory can be written to in block (rather than byte) sizes, making it easy to update. On the other hand, flash memory is not useful as RAM because RAM needs to be addressable at the byte (not the block) level. FLASH memory incorporates the floating gate of the EPROM and hot electron injection for the write process, with Fowler-Nordheim tunneling for the erase process. The charge injection process removes or adds electrons from the floating gate. This floating gate provides a gate voltage similar to a single gate transistor. The cell volume is about the size of an EPROM. The information stored in the chip can be erased section by section unlike the bit by bit erase for the E²PROM. This design now approaches the read/write speed of DRAM and SRAM with the additional feature of non-volatility.

FOWLER-NORDHEIM TUNNELING: A low current physical mechanism for erasing, and in some cases programming a nonvolatile memory device. In this mechanism, charge is removed from the floating gate of the memory cell through a thin layer of tunnel oxide.

HOT ELECTRON INJECTION: A high current physical mechanism for programming a Flash device or an EPROM. In this mechanism, charge is

injected onto the floating gate of the memory cell through a thin layer of tunnel oxide.

IMPRINT: the decrease of the ability to program (switch) the memory element to the opposite state when programmed for long periods of time in one state. This imprint failure has been correlated to the polarization-driven field-shift of the hysteresis loop. The shift is in the field direction to stabilize the present polarization direction.

MEMORY: Memory is the electronic holding place for instructions and data that a computer's microprocessor can reach quickly. When a computer is in normal operation, its memory usually contains the main parts of the operating system and some or all of the application programs and related data that are being used.

MEMORY DENSITY: The storage capacity of a memory device. The size of a memory device typically is measured in millions of bits (megabits-Mb). System memory requirements, however, are specified in millions of bytes (megabytes-Mb).

NRAM: Nonvolatile RAM is a special kind of RAM that retains data when the computer is turned off or there is a power failure. Like the computer's ROM, it is powered by a battery within the computer. It can also work by writing its contents to and restoring them from an E²PROM.

PROGRAMMING: The method for changing data from a logical "1" to a logical "0" in a nonvolatile memory array. Programming is accomplished in a Flash device one byte or word at a time. Not all bits in the byte need to be programmed. In a single transistor stacked-gate NOR Flash, all bytes must be pre-programmed and erased prior to re-programming. For Flash devices that have an internal programming algorithm, the state machine on the Flash device will automatically program the byte of data on the data bus.

RAM is a shorter synonym for **Random Access Memory**. This kind of memory is located on one or more microchips that are physically close to the microprocessor in the computer. Most desktop and notebook computers sold today include at least 32 megabytes of RAM, and are upgradeable to include more. The more RAM the computer has, the less frequently it has to access instructions and data from the more slowly accessed hard disk form of storage. Because any storage location can be accessed directly, RAM is called "random access". RAM is organized and controlled in a way that enables data to be stored and retrieved directly to specific locations. In general, RAM is much like an arrangement of post-office boxes in which each box can hold a 0 or a 1. Each box has a unique address that can be found by counting across columns and then counting

down by row. In RAM, this set of post-office boxes is known as an array and each box is a cell. To find the contents of a box (cell), the RAM controller sends the column/row address down a very thin electrical line etched into the chip. There is an address line for each row and each column in the set of boxes. If data is being read, the bits that are read flow back on a separate data line. In the most common form of RAM, dynamic RAM, each cell has a charge or lack of charge held in something similar to an electrical capacitor. A transistor acts as a gate in determining whether the value in the capacitor can be read or written. In static RAM, instead of a capacitor-held charge, the transistor itself is a positional flip/flop switch, with one position meaning 1 and the other position meaning 0. RAM can be divided into (1) main RAM, which stores every kind of data and makes it quickly accessible to a microprocessor and (2) video RAM, which stores data intended for your display screen, enabling images to get to your display faster. Main RAM can be divided into static RAM (SRAM) and dynamic RAM (DRAM). The dual-port design is the main difference between main storage RAM and video RAM.

ROM: Read-Only Memory; ROM is "built-in" computer memory containing data that normally can only be read, not written to. ROM contains the programming that allows your computer to be "booted up" or

regenerated each time you turn it on. Unlike a computer's random access memory (RAM), the data in ROM is not lost when the computer power is turned off. The ROM is sustained by a small long-life battery in your computer.

SDRAM: Synchronous DRAM is a generic name for various kinds of DRAM that are synchronized with the clock speed that the microprocessor is optimized for. This tends to increase the number of instructions that the processor can perform in a given time. The speed of SDRAM is rated in MHz rather than in nanoseconds (ns). This makes it easier to compare the bus speed and the RAM chip speed. You can convert the RAM clock speed to nanoseconds by dividing the chip speed into 1 billion ns (which is one second). For example, an 83 MHz RAM would be equivalent to 12 ns.

SRAM: Static Random Access Memory, more expensive, requires four times the amount of space for a given amount of data than dynamic RAM, but, unlike dynamic RAM, does not need to be power-refreshed and is therefore faster to access. One source gives a typical access time as 25 nanoseconds in contrast to a typical access time of 60 nanoseconds for dynamic RAM. (More recent advances in dynamic RAM have improved access time). Static RAM is used mainly for the level-1 and level-2 caches that the microprocessor looks in first before looking in dynamic RAM.

A.7 Publications and patents

1. Zhongwei Pan, and Kai Shum, Appl. Phys. Lett. **76**, 505 (2000).
2. Kai Shum, and Zhongwei Pan, Patent: “High Density Nonvolatile Semiconductor Random Access Memory” submitted on Sept. 25, 2000 (pending). <Please contact Professor Kai Shum if you are interested in our patent, his telephone number is (212)-650-7268, and E-mail address is shum@ee-mail.engr.ccny.cuny.edu>

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Scaling energy barriers to save data

Without magnetic disks to help them out, computers can't remember much. That's because nearly all electronic memory in computers goes blank when the power goes off.

Kai Shum of the City University of New York (CUNY) and his colleagues have developed a new approach to avoid computer amnesia. To create so-called nonvolatile electronic memory, the researchers built one-bit, prototype memory cells from layers of metal and semiconductors, manipulating the energy barriers that appear naturally at the interfaces.

In the Jan. 24 *APPLIED PHYSICS LETTERS*, Shum and Zhongwei Pan, also of CUNY, report the success of a III-V device, a cell made from semiconductor compounds composed of elements from columns III and V of the periodic table. Shum and coworkers made a comparable II-VI device in 1997. They will next try to create a memory cell from elements in column IV, which include silicon, the industry's standard semiconductor, Shum says. "Once we demonstrate this in silicon, it's big news," he predicts.

Other types of nonvolatile microcircuit memories are available commercially, but magnetic disks remain the cheaper alternative. Harry C. Shaw of NASA's Goddard Space Flight Center in Greenbelt, Md., calls the CUNY design "very promising technology."

A large obstacle looms, however. The new devices fail after not many rounds of switching between zero and one states—about 200 cycles for the III-V version. Shum foresees possible improvement with silicon, which generally has fewer defects than other semiconductors do.

—P.W.

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