RFIC Applications with CMOS Technology

by

Bailin Chen

A dissertation submitted to the Graduate Faculty in Engineering in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York.

2006

UMI Number: 3231966

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Abstract

RFIC APPLICATIONS WITH CMOS TECHNOLOGY

by

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In the last decade, CMOS technology has experienced rapid advancement as the minimum feature size has been steadily scaled down to a sub-micro region, so that today the channel length for MOS FET devices range from 0.8 um to 0.13 um. Unity current gain frequency f_T of an NMOS FET has increased from 10 GHz to 90 GHz. When the channel length of an NMOS FET is 0.5 um or shorter, both transconductance and unity current gain frequency is comparable to and can even surpass that of a traditional GaAs MESFET radio frequency (RF) active device. This has opened new application areas for traditional digital CMOS technology. Today, CMOS is one of the technology choices for radio frequency integrated circuits (RFIC), featured by its low cost and more circuit functionalities in a single chip. However, the CMOS process faces some challenges in RF applications. In particular, one of those challenges is the low Q of RF passive components due to the substrate loss caused by conductive silicon.

In this work, 0.5 um CMOS active devices have been characterized in comparison with their GaAs counter part - MESFETs. The RF inductor on a SiO_2-silicon substrate has been explored in a systematic way using different resistivity silicon wafers. The microstrip line on a SiO_2-silicon substrate and other CMOS passive components, such as capacitors and resistors, have also been studied. Finally a 0.5 um CMOS fiber-optic

preamplifier has been designed and measured to evaluate the RF integrated circuit performance in CMOS. Very low noise performance was achieved compared to other published results that used a similar gate length CMOS process, and a new two-stage transimpedance amplifier topology was adopted for an optical system preamplifier design. A transimpedance amplifier's performance, with the same circuit topology, has also been explored, by circuit simulation, in a 0.35 um channel length CMOS process.

Acknowledgments

I wish to express my sincere gratitude to my research advisor, Professor Norman Scheinberg, for his guidance, support, encouragement and especially his active involvement in every step of the research. I would like to thank my friends at Anadigics for their support and generous help. I would also like to thank the members of the examining committee for their time.

I deeply thank my family members, my wife Shaoxian, my two daughters, Michelle, Nicole, my parents and my sister Xiaofeng for giving me their love and tremendous support.

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Introduction **Brief History of the MOS FET**

The MOS FET device was rooted in the field effect phenomenon. The field effect transistor (FET), the first solid-state transistor, was proposed by J. E. Lilienfeld in the 1920's (Fig. 1) [1]. But there was no working device ever built at the time because the technology was not yet ready. Twenty years later in 1946, a group of researchers in Bell Laboratory revived the idea of a making field-effect transistor. It is interesting to note that during the course of the research in 1947 [2], a transistor with an unexpected physical mechanism, the bipolar junction transistor (BJT), was invented. Research efforts for making field effect transistors continued until several years later, in 1953, a first functional junction field-effect transistor (JFET) was invented (Fig. 2).

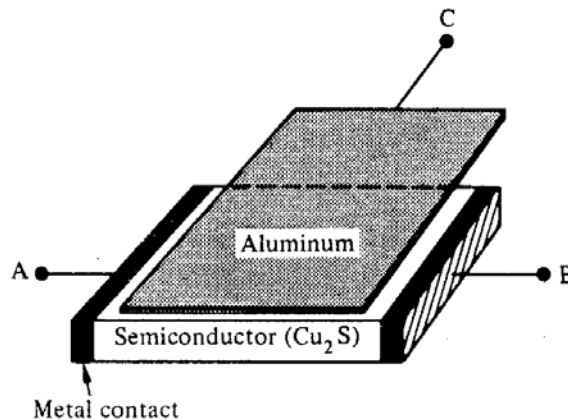


Fig. 1 Idealization of the Lilienfeld transistor (Pierret, Robert F., *Field Effect Devices*, 2nd Edition, © 1990, pp. 1. Reprinted by permission of Pearson Education, Inc., Upper Saddle River, NJ.)

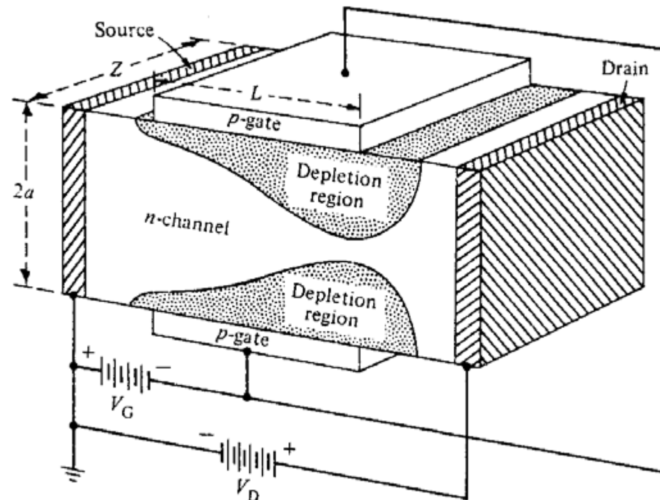


Fig. 2 Schematic diagram of the junction field effect transistor (® [1953] IEEE) [46].

After more than ten years research since the BJT was invented, the first MOS FET was reported (Fig. 3). Since then, the BJT and JFET and MOS FETs have become the three basic solid state components for all electronic circuits. Among them, the MOSFET has infinite gate impedance and a complementary device – the PMOS FET is available. This feature enables CMOS (complementary MOS) digital circuits to consume less power than circuits built with other type components. Thanks to the development of integrated circuit (IC) technology, this CMOS low power feature has successfully rendered itself to large scale and very-large scale integrated circuits. CMOS technology was quickly used to build both the memory chips and the central processing units (CPU) for computers. Driven by the rapid growth of digital and analog electronic applications, in particular the personal computer (PC) application, CMOS technologies have achieved enormous success in various electronic applications with a steady technological advancement over the decades.

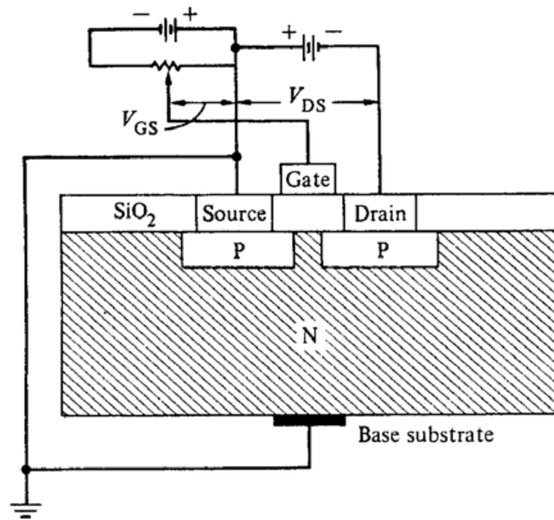


Fig. 3 Cross section of a MOSFET with correct biasing polarity.

Before the 1990's, the electronic integrated circuits industry was primarily driven by computer related digital circuits. In the meantime, BJT, JFET and CMOS technologies were also extensively used in analog integrated circuits. But integrated circuits in radio frequency is rather late because the operating frequency of silicon BJT and CMOS transistors before the mid 1990's was not high enough to support most RF applications.

Parallel to the silicon BJT, JFET, and CMOS technology developments, other materials besides silicon were also studied. Among which, GaAs was adopted as a material to build devices superior to the silicon counter parts in terms of operating frequency, particularly for military applications. The fact is that GaAs indeed possesses some extraordinary physical properties, such as its higher electron drift velocity [45] (Fig. 4) and an insulating substrate material (Fig. 5). Its higher electron drift velocity allows GaAs device, such as the metal-semiconductor FET (MESFET), to operate at a much higher frequency, up to 20 GHz. The GaAs MESFET is ideal for RF applications not only because of its higher f_T but also because its semi-insulating property allows higher Q

passive components, such as inductors, to be integrated on chip. Therefore GaAs technologies were traditionally considered as high frequency, high-speed technologies while silicon technologies were considered as low frequency, low speed technologies.

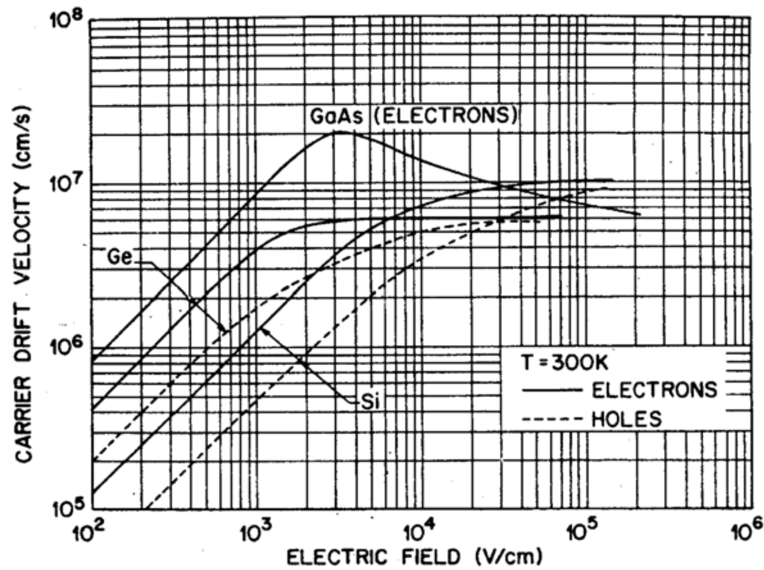


Fig. 4 Measured carrier velocity versus electric field for high purity Ge, Si, and GaAs [45].

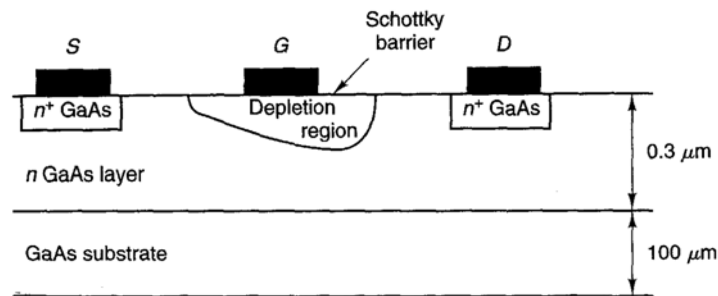


Fig. 5 GaAs FET cross section.

The picture for silicon technologies has been largely changed in the last decade. Both silicon bipolar and CMOS technologies have been greatly improved. The feature size of CMOS process has been steadily scaled down as the technology advanced. This

results in shorter and shorter channel length, and higher and higher operating frequency. When the channel length was scaled down to 0.5 um, a NMOS FET shows comparable performance to the same channel length GaAs MESFET, and its operating frequency is high enough to be used in radio frequency integrated circuits. Since CMOS technology is compatible to digital integrated circuitry, integrating RF circuits with a CMOS process would have the advantage of including more circuit functionality in a single chip rather than using separate GaAs RF ICs. GaAs technologies are still extensively used in RF and microwave integrated circuits today and can offer superior quality circuit performance in for example, power amplifier IC's. On the other hand, high integration capability and improved RF circuit performance makes CMOS RF a choice for many applications. The physical properties of silicon and GaAs is shown in Table 1 for comparison [45]. It is worth noting that silicon has much better thermal conductivity than GaAs. This is very important when considering the reliability of integrated circuits.

Table 1. Material Properties of Si and GaAs at 300° K [45]

Property	**Silicon**	**GaAs**
Intrinsic resistivity (Ω - cm)	2.2×10^5	4.4×10^8
Dielectric constant	11.9	13.1
Thermal conductivity (W / cm - °K)	1.5	0.46
Bandgap at 300 K (eV)	1.12	1.42
Electron mobility (cm^2 / V – s)	1500	8500
Hole mobility (cm^2 / V - s)	450	400

In the following chapter, a 0.5 um channel length CMOS FET and GaAs MESFET have been characterized relevant to their RF applications. The characterization

of noise, linearity, and gain of a silicon MOSFET vs a GaAs MESFET are presented. The performance of state of the art CMOS technology will be presented as well. A newer silicon technology, bipolar CMOS (BiCMOS) technology, combines the advantages of relative higher operating frequency BJT and low power CMOS FET into a single process and has emerged in the last ten years. It has been extensively used in RF integrated circuits as well. However, the discussion of this technology is beyond the scope of this study.

Chapter 1 RF Characteristics of a CMOS FET

RF circuits were realized in discrete form for a long time after the integrated circuit was invented. While low cost silicon bipolar and CMOS processes were extensively used to build digital and analog ICs, their operating frequencies were not high enough to operate in RF region. GaAs technology, which developed later, was the first technology used to integrate radio frequency circuits into ICs. GaAs's higher electron mobility and electron velocity yield a higher operating frequency device. This high frequency device coupled with GaAs semi-insulating material nature made GaAs technologies superior to silicon technologies for RF applications. Therefore GaAs MESFET technology dominated RF-IC production for a period of time and is still widely used in RF-IC products. But silicon technologies did not stand still. The feature size of the CMOS process has been steadily scaled down as the technology advanced. This smaller CMOS feature size has increased the CMOS operating frequency in the last decade, enabling this technology to compete with its GaAs counterpart-MESFET technology for RF applications.

RF circuits play crucial roles in various communication systems, such as optical communication systems and wireless communication systems. In those communication systems, RF circuits in a receiver's front-end section detect the high frequency signal and amplify it to an appropriate level for the following stages. The active devices required to build such RF circuits should amplify the received signal with enough gain since the received signal could be very weak after suffering tremendous loss through propagation. Because the signals are very weak, often arriving at the receiving end at a level near the

thermal noise threshold, active devices in an RF receiver have to be low noise devices. The active device ideally only performs linear amplification to the received signal without causing nonlinear distortion. The above three important requirements for the RF active devices are represented as the RF parameters: gain, noise, and non-linearity. In the following discussion, those important RF circuit characteristics for a MOS FET device are presented. A 0.5 um channel length modern CMOS technology has been used to fabricate 400 um width N and P channel MOS FET samples. The sample's RF characteristic has been measured in a 50 Ω RF test system. A 0.5 um channel length GaAs MESFET has also been measured for performance comparison.

1.1 RF small signal model of a MOS FET device

The MOS sample FETs are carefully laid out as a common source configuration for RF measurement (Fig. 1.1). The source terminals of the FET are connected to the substrate through multiple via holes to reduce source parasitic resistance. The small signal circuit model of N and P channel MOS FET has been extracted with two port S parameter measurement data (Fig. 1.2). Small signal model parameters of a GaAs MESFET are listed, along with the silicon NMOS FET parameters for comparison. The small signal model parameters of silicon MOS FETs and GaAs FETs are extracted under the same drain voltage and current condition. It can be seen from the listed small signal model parameters that, for the 0.5 um channel length technologies, an NMOS FET device performance is close to that of the GaAs MESFET. The NMOS FET trans-conductance g_m is the same as the g_m for a GaAs FET. But the NMOS FET carries more parasitic capacitance than a GaAs FET does. Consequently the current unity gain frequency f_T is

lower in an NMOS FET than for a GaAs FET device. Silicon PMOS FET exhibits about half the NMOS FET trans-conductance and half the current unity gain frequency because of lower hole drift velocity. These data show, for 0.5 um channel length technology, that in gain and operating frequency an NMOS FET is certainly comparable to a GaAs MESFET.

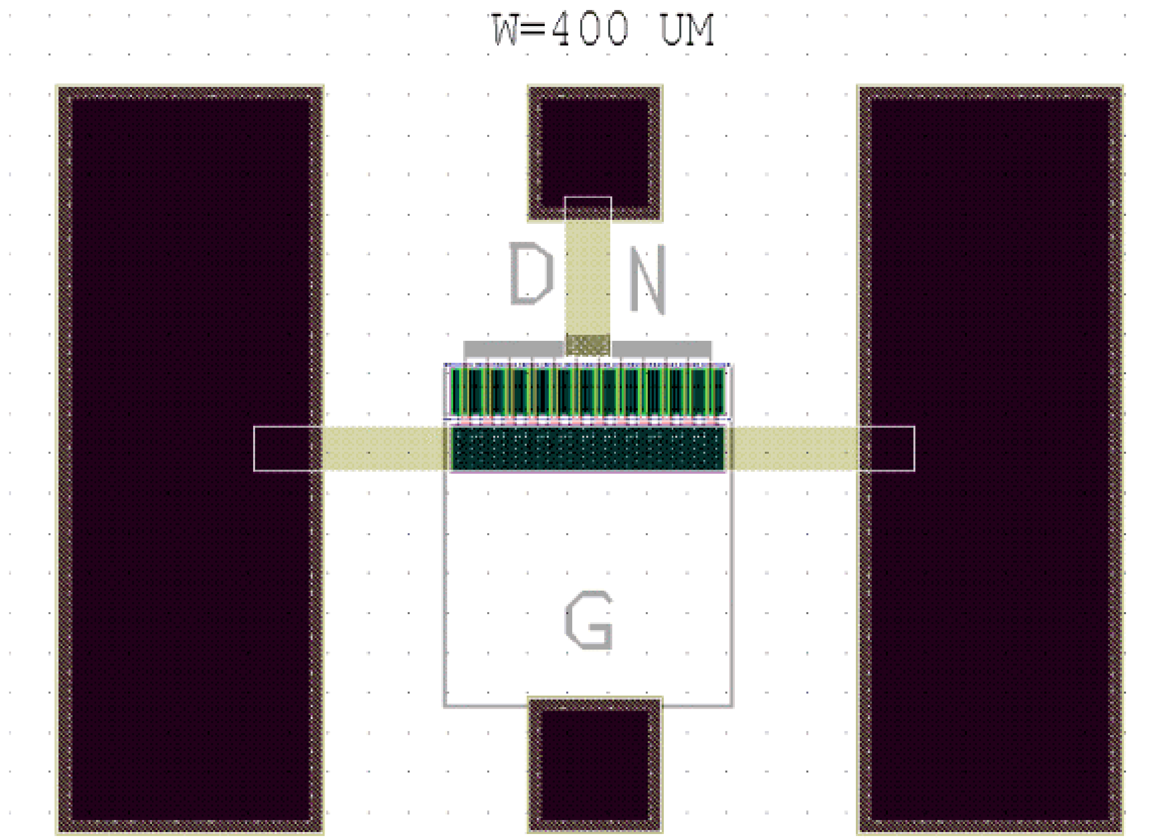
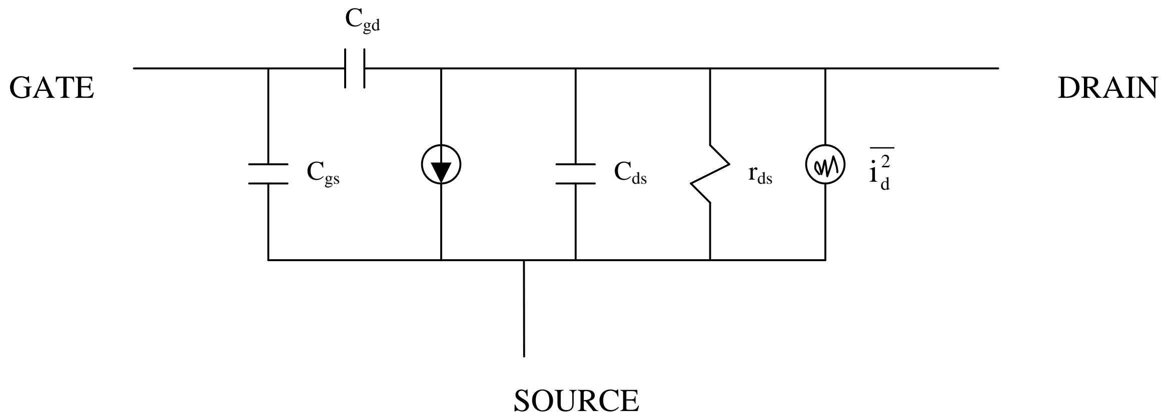


Fig. 1.1 MOS FET layout



NMOSFET	GaAs FET
g_m=0.15 S/mm	g_m=0.15 S/mm
C_{gs}=1.6 pF/mm	C_{gs}=1.0 pF/mm
C_{gd}=0.3 pF/mm	C_{gd}=0.1 pF/mm
r_{ds}=170 Ω/mm	r_{ds}=100 Ω/mm
f_T =15 GHz	f_T=20 GHz

Fig. 1.2 Small signal model

1.2 Noise performance

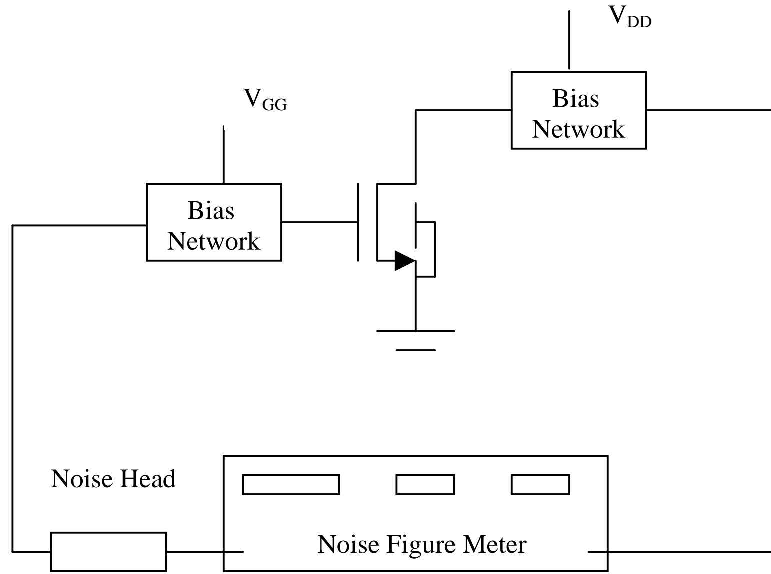
MOS FET noise primarily comes from two noise sources: channel thermal noise and flicker noise. Channel thermal noise is due to drain-source current flowing through a resistive channel. This wide band noise affects the noise performance of a CMOS integrated circuit over a wide frequency range, so it is a major noise concern for high frequency circuit design such as wide-band low noise amplifier design and high frequency narrow-band low noise amplifier design.

The flicker noise is low frequency noise. It is attributed to CMOS process imperfection. The magnitude of its power spectral density is proportional to the reciprocal of frequency f. Therefore we also call it 1/f noise. Since the power of this noise is located at low frequencies, it affects the close in spectral noise performance of RF oscillators. In the RF oscillator circuit this low frequency noise modulates the oscillating signal causing a wave form jittering around equilibrium in the time domain. In the frequency domain, because of 1/f noise modulation, the oscillating frequency is convoluted by 1/f noise frequency component resulting in crowded noise spectrum in the neighborhood of the oscillating carrier frequency. MOS FET noise is represented by two noise-generators in parallel.

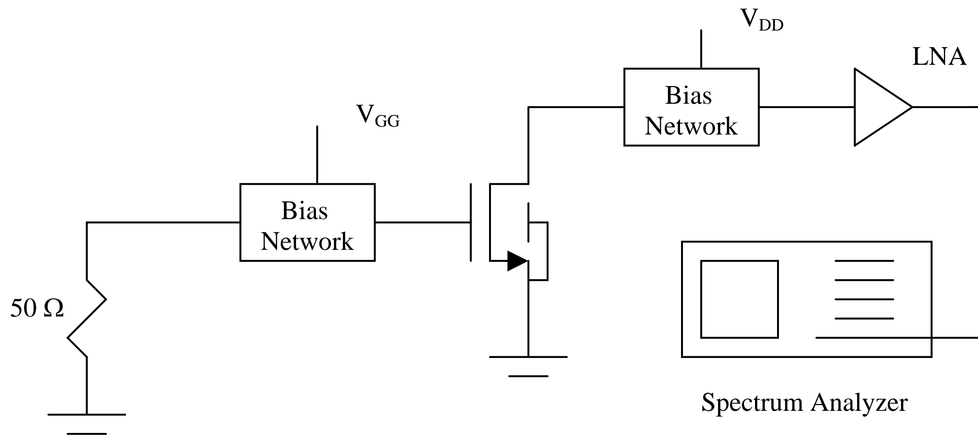
$$\overline{i_d^2} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + K\frac{I_D^a}{f}\Delta f \qquad (1.1)$$

$\overline{i_d^2}$ is noise-current spectrum in bandwidth Δf and I_D is the drain bias current. K is a constant for a given device, and exponent a is a constant between 0.5 and 2. g_m is the device transconductance at the operating point. Both 0.5 um MOS FET and GaAs MESFET noise has been measured in a 50-Ω impedance environment (Fig. 1.3(a), (b)). This measurement is done by a noise figure meter from 10 MHz to 1 GHz, but because of limitations in the noise figure equipment, a spectrum analyzer is used to measure noise from 4 KHz to 20 MHz. The measured data (Fig. 1.4) is presented in noise figure (NF) which is defined in equation (1.2). It is expressed as a ratio of input signal to noise ratio (P_i/N_i) to the output signal to noise ratio (P_{out}/N_{out}) of the device.

$$NF(dB) = 10\log_{10} \frac{P_i / N_i}{P_{out} / N_{out}} \quad (1.2)$$



(a) Noise figure measurement set up with a noise figure meter.



(b) Noise measurement set up with a spectrum analyzer.

Fig. 1.3 Noise measurement set up

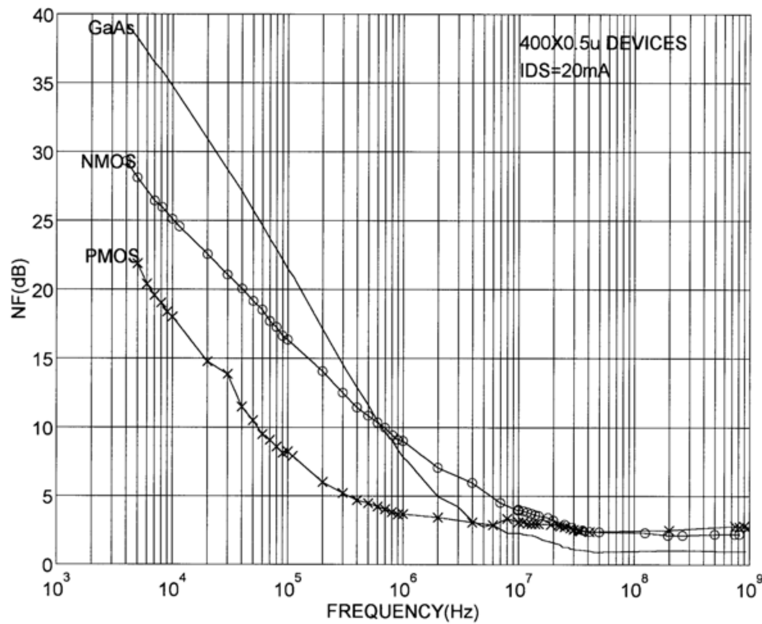


Fig. 1.4 MOS and GaAs FET noise characteristic.

From measured noise data, we see that low frequency 1/f noise linearly decreases with frequency on a log-log scale for both MOS FETs and GaAs FETs. At high frequencies, wide band thermal noise dominates device total noise, exhibiting a constant noise floor. The frequency where 1/f noise intercepts the flat thermal noise is called the 1/f noise corner frequency. For better oscillator performance, a lower 1/f noise corner frequency device is desired. NMOS FETs exhibit similar or slightly higher 1/f noise corner frequency than do GaAs FETs. PMOS FETs exhibits the lowest 1/f corner frequency, but the PMOS FET's relatively lower g_m will require a larger device to achieve enough loop gain for oscillation to occur. The larger PMOS FET in turn results in smaller drain source resistance r_{ds}, which degrades the spectral purity of the oscillator output. At higher frequencies, the noise figure of a GaAs FET is 1 dB better than it's NMOS FET counterpart.

The noise measurement results above have been used to model the device noise for circuit simulation. The calculated result from the SPICE noise models (1.3), (1.4) is compared to the measured data in (Fig. 1.5(a), (b)).

NMOS: $$\overline{i_d^2} = 4kT\left(\frac{2}{3}g_m\right) + \frac{\left(0.75\times10^{-27}\right)\cdot I_D^{1.2}}{COX\cdot L_{eff}^2\cdot f} \qquad (1.3)$$

GaAs: $$\overline{i_d^2} = 2.8\cdot kT\cdot g_m\cdot e^{\left(0.85\cdot\frac{I_{DS}}{I_{DSS}}\right)} + \left(2\times10^{-12}\right)\frac{I_D}{f} \qquad (1.4)$$

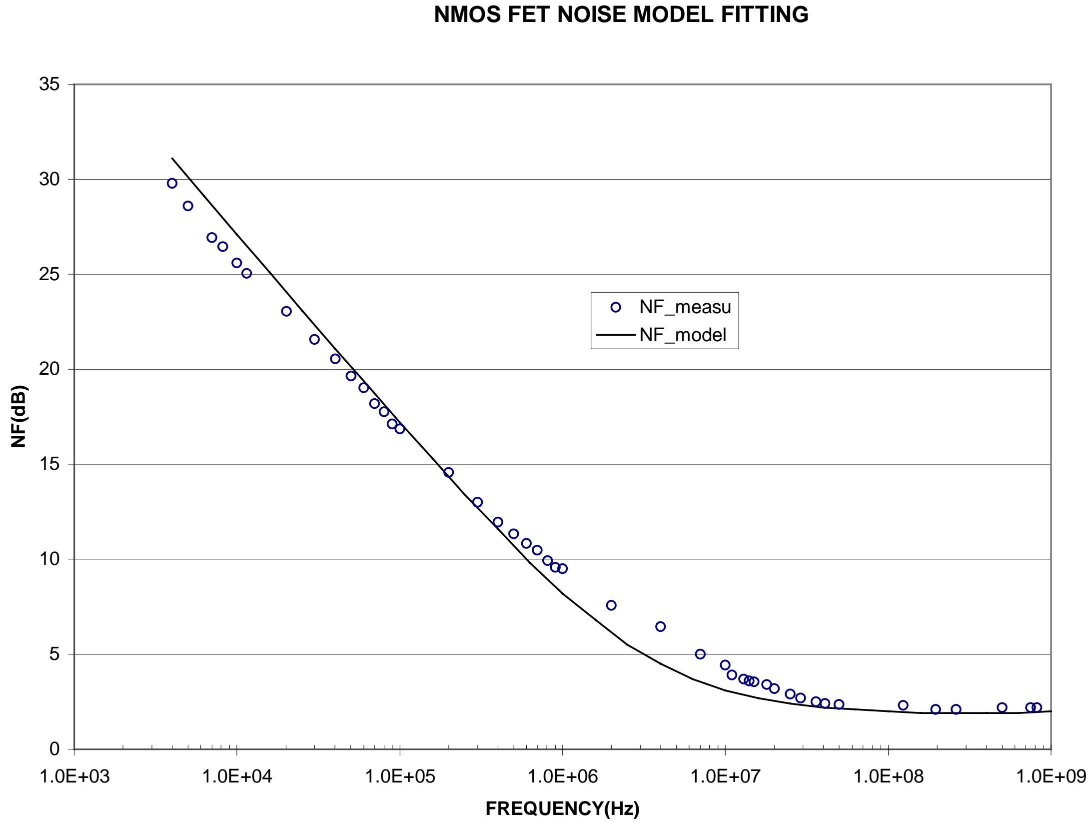


Fig. 1.5 (a) NMOS FET noise model fitting.

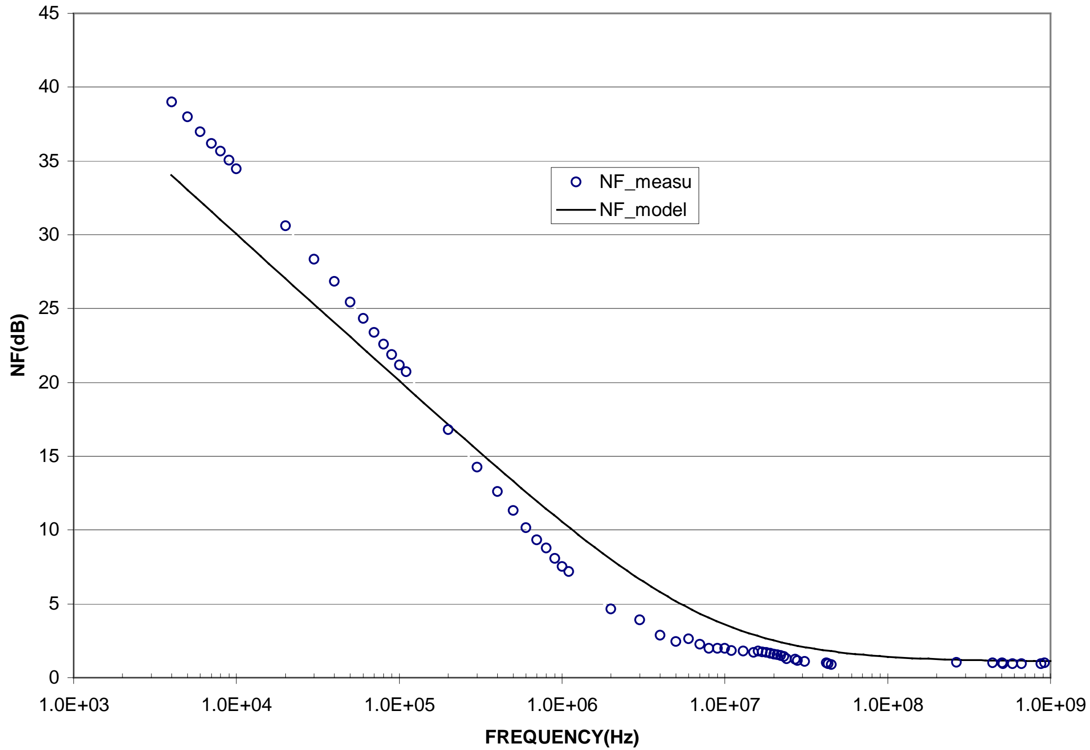


Fig. 1.5 (b) GaAs noise model fitting.

1.3 Linearity

In addition to gain and noise performance, the RF device linearity is another important characteristic. Assuming that the active devices in an RF amplifier are ideal linear devices, the output of the amplifier would be a linear function of the input. The output waveform would be exactly the same shape as the input waveform except for the linear amplification applied; no new frequency components would be created. But in reality all active devices are nonlinear. A linear device is only an approximation under certain condition. A signal through an amplifier could be severely distorted in large signal condition due to a non-linear input-output transfer function (Fig. 1.6).

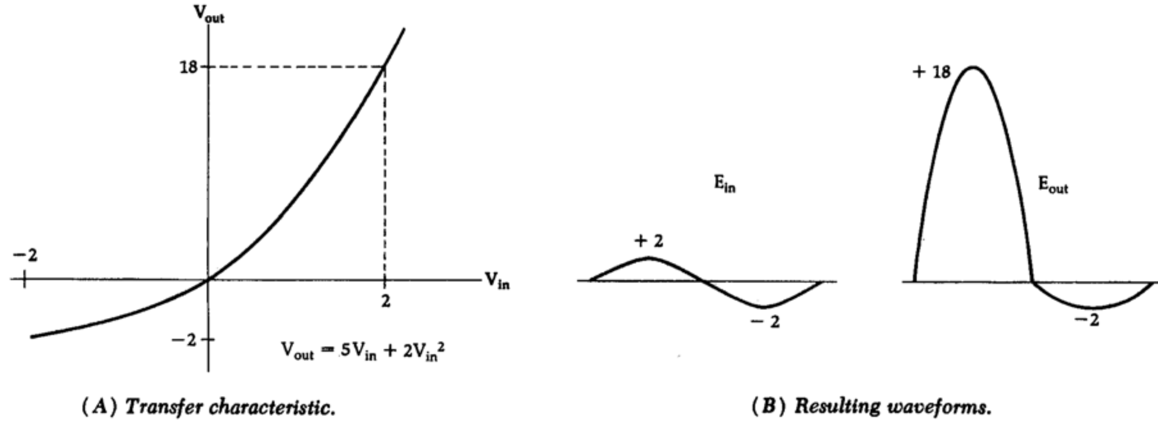


Fig. 1.6 Nonlinear amplifier characteristic.

Even in small signal conditions there are always spurious components added to the output signal in the form of harmonic generation or inter-modulation distortion. To explain this type of distortion a nonlinear transfer function is used.

$$V_{out} = AV_{in} + BV_{in}^2 + CV_{in}^3 \quad (1.5)$$

V_{in} is input voltage, V_{out} is output voltage. If the input signal consists of two signals of equal magnitude but at different frequencies, new frequencies components would appear in the output signal.

$$V_{in} = V[\cos(\omega_1 t) + \cos(\omega_2 t)] \quad (1.6)$$

Expanding the right side of equation (1.5) and discarding the dc term, we obtain the following fundamental components.

$$\omega = \omega_1, \omega_2 : A[V(\cos(\omega_1 t) + \cos(\omega_2 t))] + \frac{9}{4} \cdot CV^3[\cos(\omega_1 t) + \cos(\omega_2 t)] \quad (1.7)$$

And higher order components.

$$\omega = 2\omega_1, 2\omega_2 : \frac{BV^2}{2}[\cos(2\omega_1 t) + \cos(2\omega_2 t)] \quad (1.8)$$

$$\omega = \omega_1 \pm \omega_2 \; : \; BV^2[\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t] \tag{1.9}$$

$$= 3\omega_1, 3\omega_2 \; : \; \frac{CV^3}{4}[\cos(3\omega_1 t) + \cos(3\omega_2 t)] \tag{1.10}$$

$$= 2\omega_1 \pm \omega_2 \; : \; \frac{3}{4}CV^3[\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t] \tag{1.11}$$

$$= 2\omega_2 \pm \omega_1 \; : \; \frac{3}{4}CV^3[\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t] \tag{1.12}$$

(1.7) represents the linear gain of the amplifier. The second term in (1.7) can be neglected since V is very small in this discussion and C << A. Among the higher order components, (1.9), (1.11), (1.12) are usually more important to the circuit performance. Particularly so, (1.11) and (1.12) since the frequencies of these unwanted inter-modulation products often fall in or close to the band of the signal of interest. (1.9) is called second inter-modulation product. (1.11) and (1.12) is called third inter-modulation product. As we can see, V_{out} is linear function of input voltage V at the fundamental frequencies but is the square of V for the second harmonic and the cube of V for the third harmonic. Non-linearity can be measured by applying two signal tones of equal amplitude closely spaced in frequency (f1 and f2) at the input, and measuring the rise with input level of the second inter-modulation product at (f1-f2) and third at (2f1-f2), such as (Fig. 1.7). On a logarithmic plot, the second inter-modulation level rises at a slope of 2 relative to the fundamental signal tone at output (not shown), the third inter-modulation level rises at a slope of 3 relative to the fundamental signal tone at output. The line of second inter-modulation product intersects with line of the fundamental tone at a point called the 2nd intercept point. Similarly, the third inter-modulation product line intersects with the line of the

fundamental tone at a point called the 3rd intercept point. The intercept point is usually extrapolated from measurements made at low signal levels.

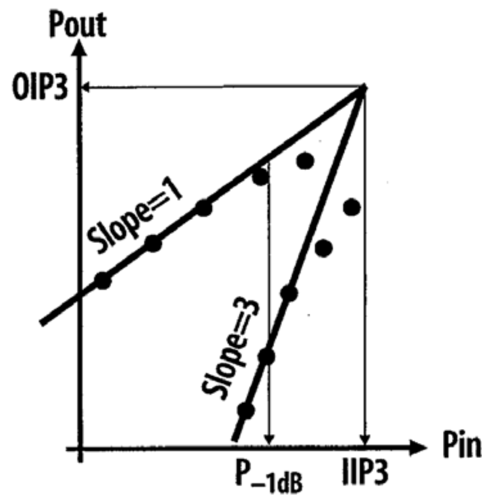


Fig. 1.7 Extrapolated intercept point at output or input.

The linearity characteristics of the MOS FET and GaAs FET have been evaluated against their intercept points (Fig. 1.8 and Fig. 1.9). The input intercept point gives the magnitude of the two equal amplitude input signals for which an output inter-modulation product (2nd or 3rd) intercepts with the output fundamental signal. Output intercept point simply indicates the magnitude of the output inter-modulation product (2nd or 3rd) at which it intercepts with the output fundamental signal. The output intercept point data equals input intercept point data multiplied by the device gain. For linear devices, high input and output intercept points are expected.

The intercept data are taken at 50 MHz using two signal tones at the input. These data shows that the transistors become more linear at larger bias current (both in the second and the third inter-mod). NMOS FETs appear more linear than GaAs FETs at lower current but they are comparatively worse at higher current. The PMOS FET is the

most linear device among the three, but gain is the lowest. Before leaving this section, the 0.5 channel length NMOS FET characteristics have been summarized in Table 1.1 in comparison with a 0.5 um widely used GaAs FET. It is obvious that 0.5 um silicon NMOS FET has comparable gain, f_T, and linearity performance but is shy on noise figure. It is clear that CMOS is a viable choice for certain RFIC applications.

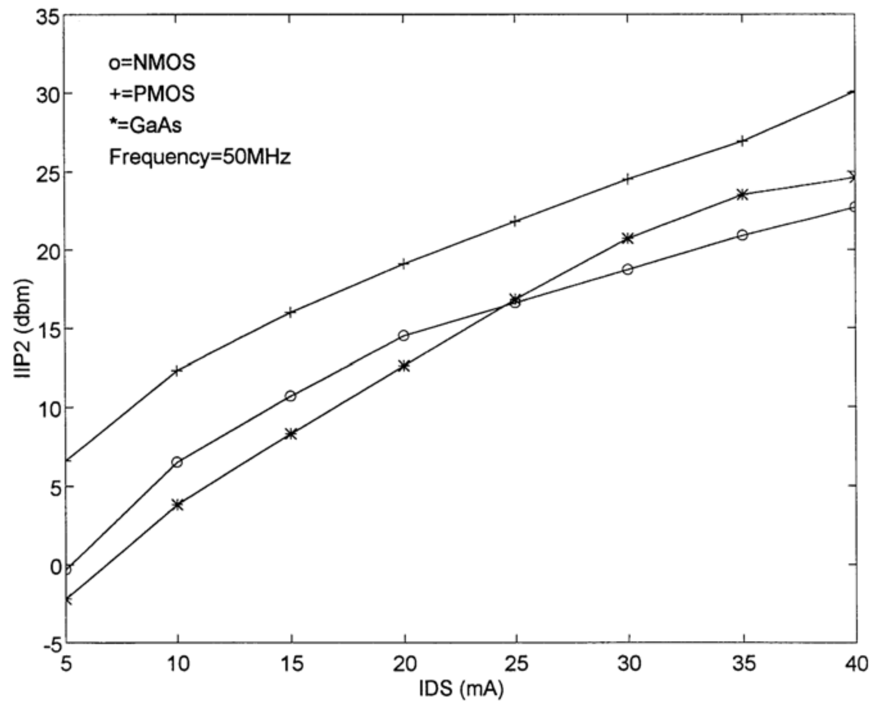


Fig. 1.8 (a) MOS and GaAs FET second input intercept plot.

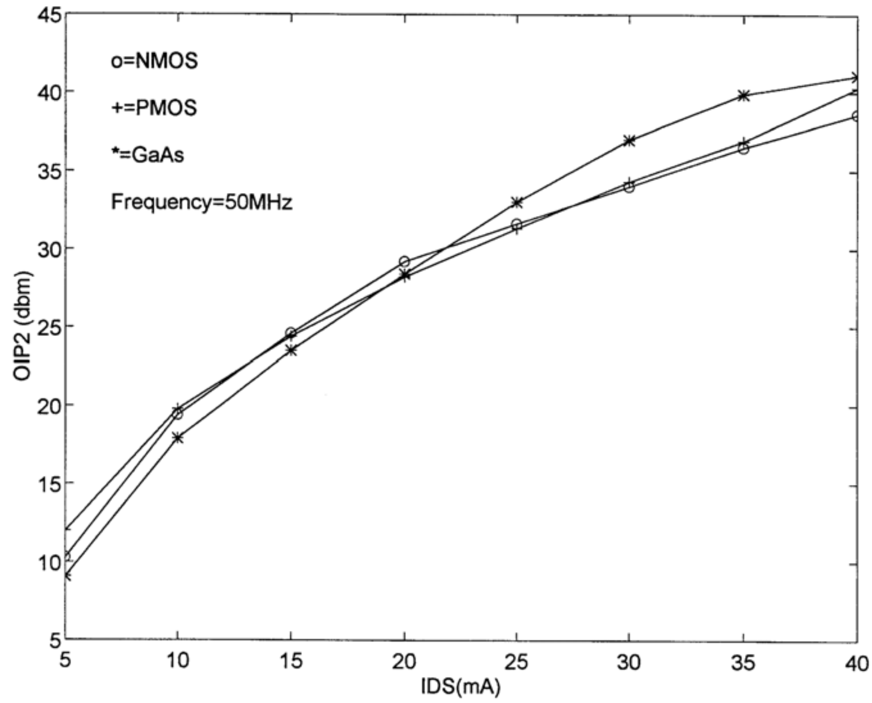


Fig. 1.8 (b) MOS and GaAs FET second output intercept plot.

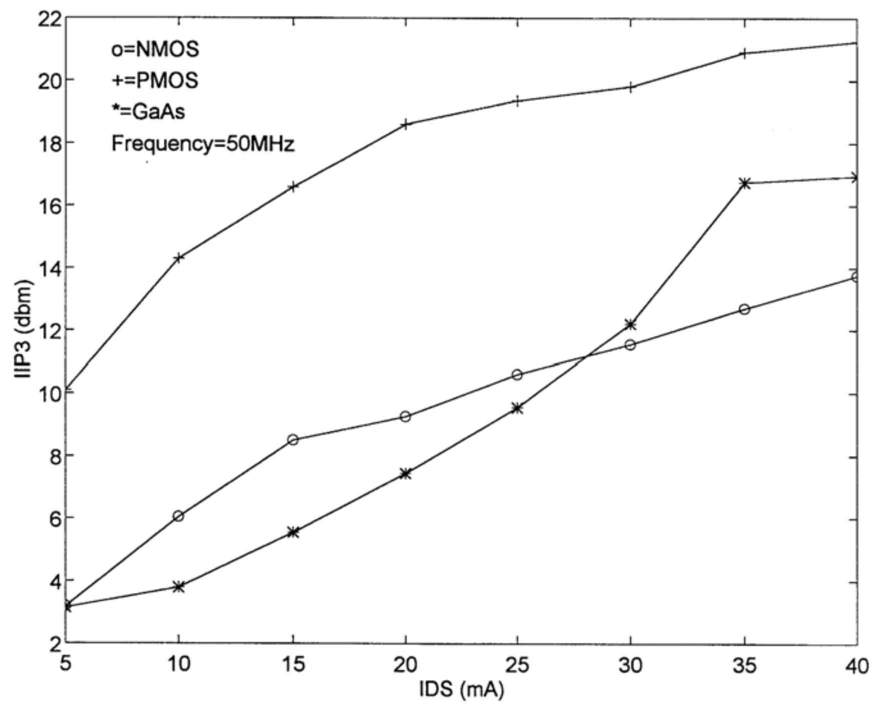


Fig. 1.9 (a) MOS and GaAs FET third input intercept plot.

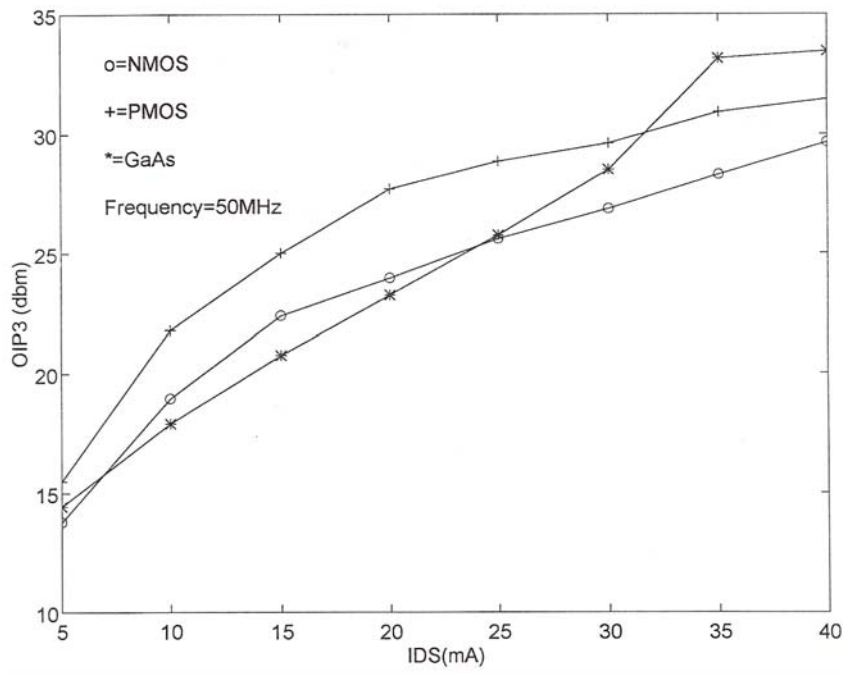


Fig. 1.9 (b) MOS and GaAs FET third output intercept plot.

Table 1.1 RF Characteristic Comparison between GaAs FET and MOS FET

400 um FET is used. FET is biased at 20 mA at Vds=3 volts.

	g_m	f_T	C_{gs}	C_{gd}	r_{ds}
	(S/mm)	(GHz)	(pF/mm)	(pF/mm)	(Ω/mm)
PMOS FET	0.08	8	1.3	0.3	180
NMOS FET	0.15	15	1.6	0.3	170
GaAs FET (1)	0.15	20	1.0	0.1	100
	NF (2)	IIP2	OIP2	IIP3	OIP3
	(dB)	(dB)	(dB)	(dB)	(dB)
PMOS FET	2.5	19.1	28.2	18.6	27.7
NMOS FET	2.0	14.5	29.2	9.3	24.0
GaAs FET	1.0	12.6	28.4	7.5	23.3

(1) GaAs FET with medium power process is used.

(2) Noise figure data is taken at 400 MHz.

1.4 Recent development of CMOS technology

Primarily driven by the personal computer industry's demand for faster and faster digital integrated circuits, the channel lengths of MOS FETs have been continuously scaled down in recent years at an ever faster pace. This technology scaling results in higher and higher f_T and lower thermal noise (Fig. 1.10, Fig. 1.11) [3], [4]. The unity current-gain frequency f_T of the NMOS FET reaches 90 GHz with channel length scaling down to 0.1 um. The thermal noise exhibits a steady decline compared to longer channel

MOS FETs. While more advanced MOS FETs greatly benefit RFIC applications in terms of higher operating frequency and lower thermal noise they impose some challenges to RFIC performance. Their 1/f performance and linearity are worse than the older generation MOS FET [4], [5], [6].

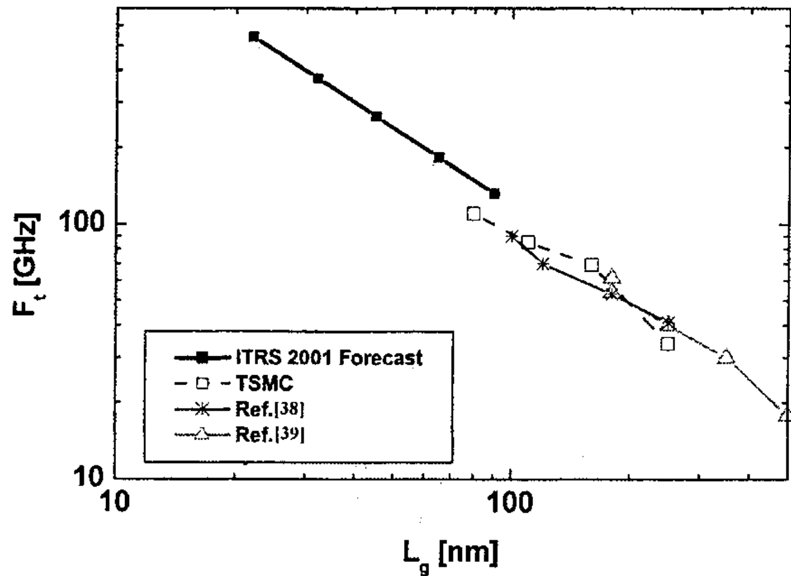


Fig. 1.10 f_T vs channel length (® 2003 IEEE) [4].

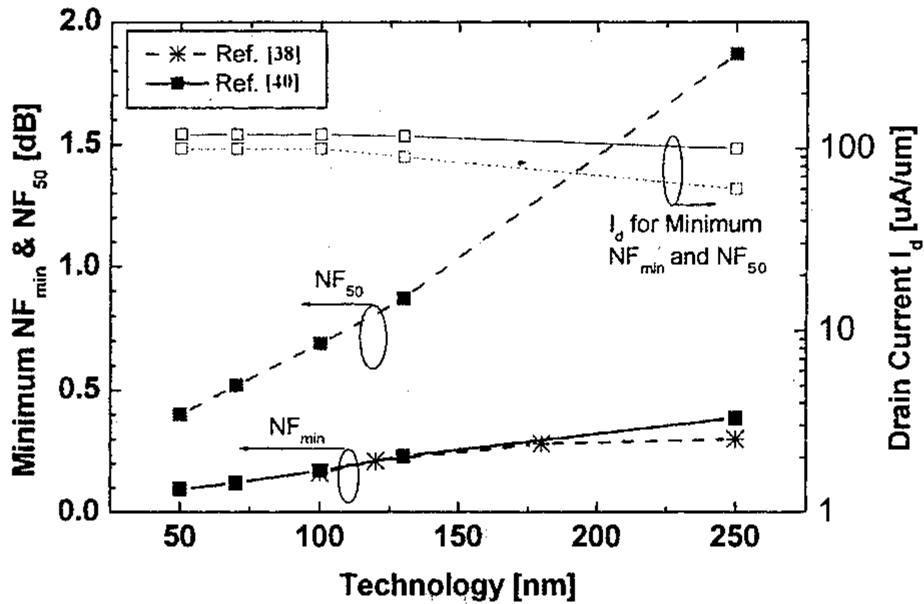


Fig. 1.11 Noise figure (NF) vs channel length (®2003 IEEE) [4].

Another challenge for CMOS RF integrated circuits arises from the conductive silicon substrate which causes different parts of the circuit to interfere with each other. To reduce this interference several inter-device isolation techniques can be implemented [7]. Simply using high resistivity silicon substrate in CMOS process to reduce substrate interference has been reported in the last ten years [8], [9]. A MOS FET built on this resistive substrate has been reported exhibiting the same DC characteristics and similar RF characteristics to the normal substrate resistivities MOS FET. However achieving a reliable digital compatible CMOS process in a high resistivity material remains to be seen.

A more traditional approach to the problem of improving device isolation is the use of a grounded "guard ring" that surround the sensitive active devices. This approach is shown in Fig. 1.12(a). The effectiveness of this technique depends on the width of the guard ring, substrate resistivity, and the inductance between the guard ring and ground. In general, the isolation improves with increasing spacing, guard ring width, and substrate resistivity.

With a fixed substrate resistivity, a further improvement in isolation can be achieved through the use of a deep low-resistivity n-well placed underneath the active device; when biased to a low-impedance and low-noise potential, it acts as an effective shield to signals injected from nearby sources. This approach is shown in the cross section in Fig. 1.12(b). Deep trench isolation techniques can also be employed to improve isolation between devices, as shown in Fig. 1.12(c), although the improvement in device isolation with this approach is modest compared to the other two approaches. Clearly, a

combination of lightly doped substrates, deep n-wells, and guard rings can provide for improved isolation in an RF integrated circuit.

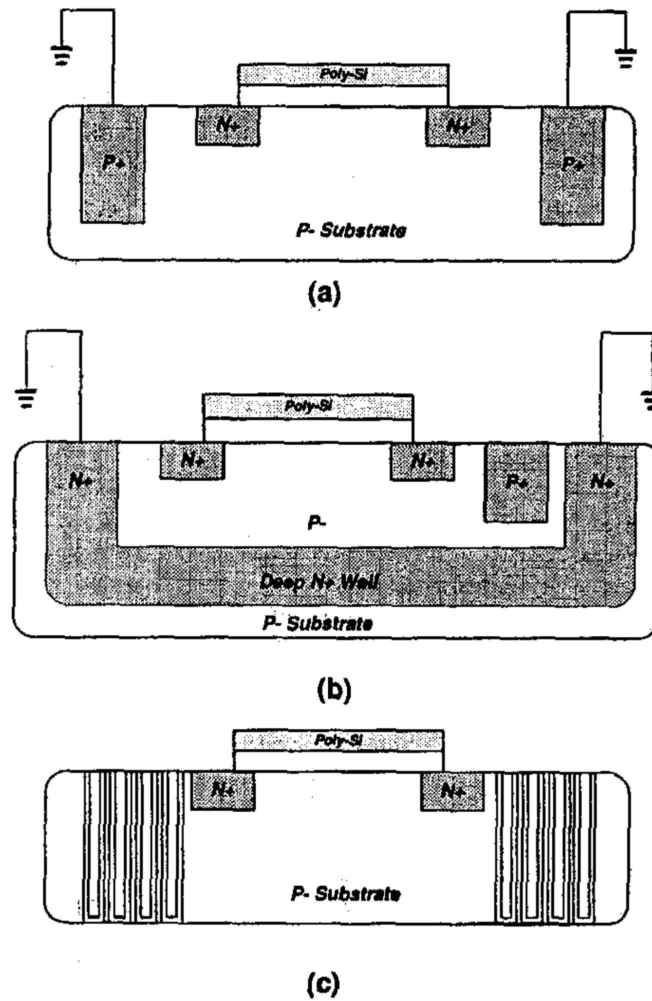


Fig. 1.12 Different isolation techniques used for RF-SOC applications in bulk technologies [7]: (a) P+ substrate guard-ring isolation, (b) buried n- layer isolation, and (c) deep trench isolation.

Chapter 2 Inductor on an MOS Silicon Substrate

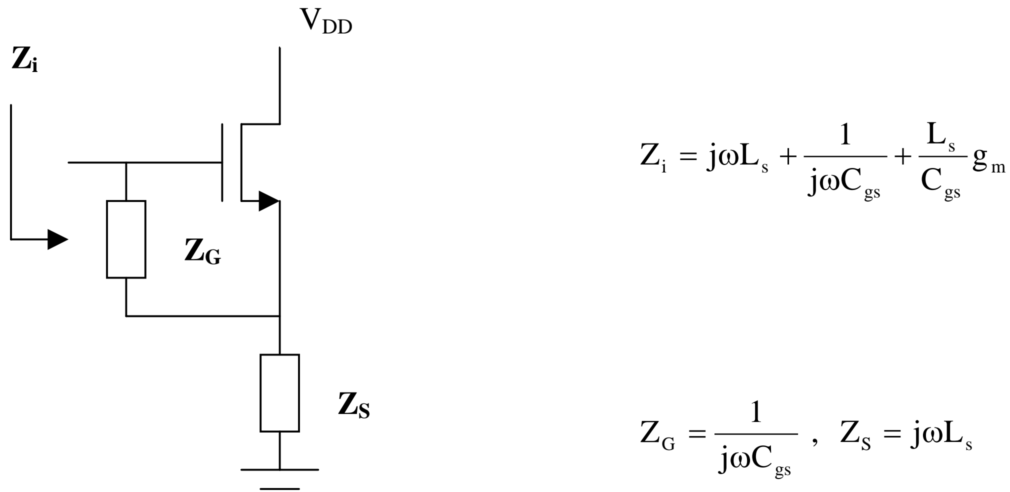
We have just discussed the MOS FET RF performance. As an active device, the MOS FET RF characteristic is directly related to the CMOS RF circuit performance. But of equal importance is the RF characteristic of passive components in a CMOS process. That leads to additional requirements for a CMOS process comparing to its traditional digital applications.

Since the development of traditional CMOS technology has been driven by digital circuit applications, notably represented by the personal computer, the process was not tuned to meet RF integrated circuit requirements. The passive components have been of little importance. Inductors were not used in CMOS processes. In contrast, passive components are of great importance in any RF design; their performance is one of the key issues in RF CMOS integration, especially for higher operating frequency [9]. On the other hand, the on chip inductor has been used in GaAs RF integrated circuits for years, where, due to its semi-insulating substrate, a higher quality on chip inductor is easily realized

In recent years many innovative efforts have been spent on improving the CMOS process to meet RF integrated circuit needs without disturbing its digital applications. Required RF passive components have been added to the process. Most importantly, an inductor has been introduced to the CMOS process. In this chapter, the inductor in a CMOS process will be discussed. Resistors and capacitors in a CMOS process will be discussed in the next chapter.

2.1 Inductor's application for CMOS RF integrated circuits

As a magnetic energy storage component, inductors are frequently used in RF integrated circuits to implement impedance matching and tuning functions for the low noise amplifier (LNA), and for frequency mixer and voltage controlled oscillator (VCO) circuits. In an LNA circuit (Fig. 2.1), for example, inductor Ls is used in the source of the FET to tune out gate capacitance, so that impedance Zi would be matched to the driving impedance at a specified frequency.



$$Z_i = j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{L_s}{C_{gs}} g_m$$

$$Z_G = \frac{1}{j\omega C_{gs}}, \quad Z_S = j\omega L_s$$

Fig. 2.1 Use of an inductor Ls for impedance matching.

To evaluate the merit of an inductor, its quality factor Q is defined by

$$Q = \frac{\text{Energy(stored)}}{\text{Energy(lost per cycle)}} \tag{2.1}$$

If the inductor is connected as a one port configuration, Q is measured by

$$Q = \frac{\text{Im(Zin)}}{\text{Re(Zin)}} \tag{2.2}$$

Zin is the impedance of an inductor when connected as a one port component.

Generally there are two different inductors implemented in CMOS integrated circuits: the bond wire inductor and the planar inductor (Fig. 2.2(a), (b)). A bond wire is a metal wire usually used to connect the IC to its package pins. While a bond wire can be used as a high Q inductor, tolerance is a major problem [10]. Planar inductors, on the other hand, are built by using CMOS process interconnection metal layers to form spiral inductors. Planar spiral inductors have lower Q but many improvements have been made for it to meet RFIC requirements. Now planar spiral inductors have been incorporated into standard CMOS process for RF applications. We will therefore focus our discussion on planar spiral inductors.

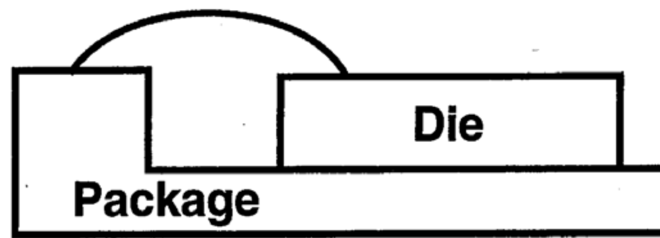


Fig. 2.2 (a) Bond wire inductor.

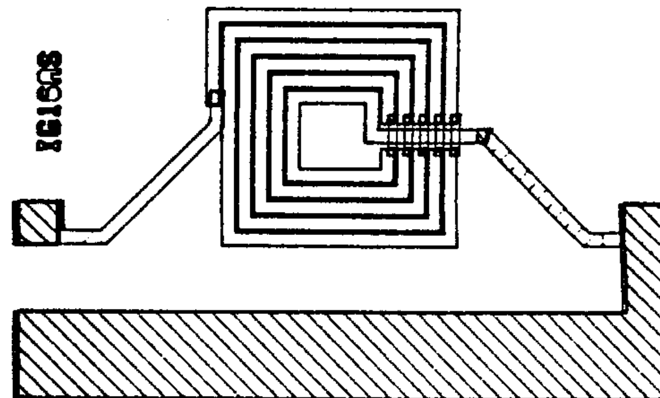


Fig 2.2 (b) Planar spiral inductor.

2.2 CMOS Inductor loss analysis and its performance

The CMOS Spiral inductor is built by interconnect metal layers on silicon dioxide which is grown on a silicon substrate (Fig. 2.3). Since the substrate material used for conventional digital CMOS process is highly conductive ($\rho < 0.1$ Ω-cm) [4], the inductor suffers substrate eddy current loss in addition to metal strip loss as compared to a GaAs inductor. Q value of the inductors built on this process is fairly low (Q ~ 5 or lower) [11], [12], making this kind of inductors difficult to use for RF circuit applications. Other researches [13], [14], [15], [16], [17] show that metal thickness, oxide thickness, and substrate resistivity can all affect inductor's performance. But the most important factors are metal thickness and substrate resistivity.

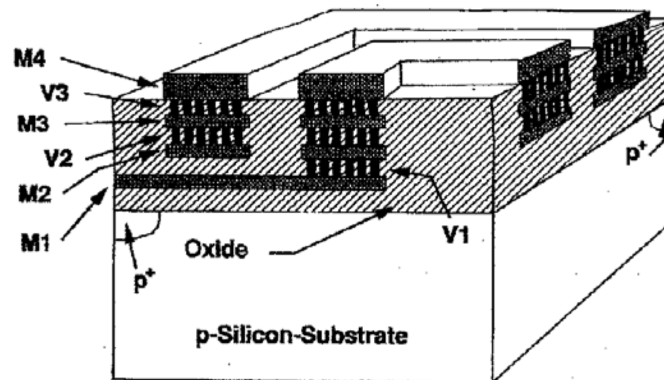


Fig. 2.3 MOS inductor cross section (® 1996 IEEE) [14].

In our research [18], the effect of the substrate resistivity on the inductor Q is investigated in a systematic way. Some data is also presented on the effect of metal strip thickness and metal height. Two rectangular spiral inductors are fabricated from gold

interconnect metal, whose conductivity is close to that of aluminum. One inductor is fabricated from 1.5 um thick metal deposited on top of 2 um thick silicon dioxide. The other inductor is fabricated from 3.5 um thick metal also deposited on top of 2 um thick silicon dioxide. The silicon wafers chosen have different resistivities, ranging from 0.5 Ω-cm to 2 KΩ-cm. Gallium Arsenide wafers without the oxide are used as well for comparison. Some of the inductors fabricated out of the thick metal are "air bridge inductors". A cross sectional view of an air bridge is shown in Fig. 2.4. As their name implies, the inductors fabricated with air bridges have most of their length suspended in air. Although this kind of inductor is rarely used in silicon integrated circuits it is routinely used in GaAs RF integrated circuits as a method to effect crossovers and to reduce interconnect capacitance. In this study we used the air bridge type inductor to investigate the effect on inductor Q of inductor height above the substrate. The layouts for the air bridge and for the standard inductor are shown in Fig. 2.5. All of the inductors in this study are of the sizes given below:

1.5 um Thick Metal Inductor	3.5 um Thick Metal Inductor
Nominal Inductance = 18 nH	Nominal Inductance = 18 nH
Metal Width = 16 um	Metal Width = 16 um
No. of Turns = 8.5	No. of Turns = 8.5
Metal Spacing = 2 um	Metal Spacing = 5 um
Inner Diameter = 75 um	Inner Diameter = 75 um

The large inductor area, resulting from the large metal width (16 um) and the large number of turns, guarantee that substrate losses would be maximized. This would make it easier to observe the effects of different substrate resistances on inductor Q.

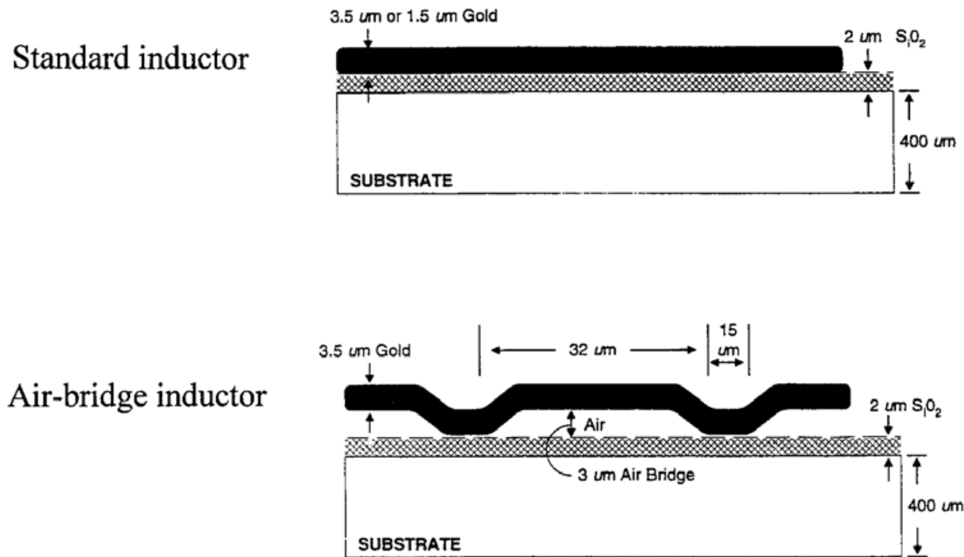


Fig. 2.4 Cross sectional view of standard and air-bridge spiral inductor.

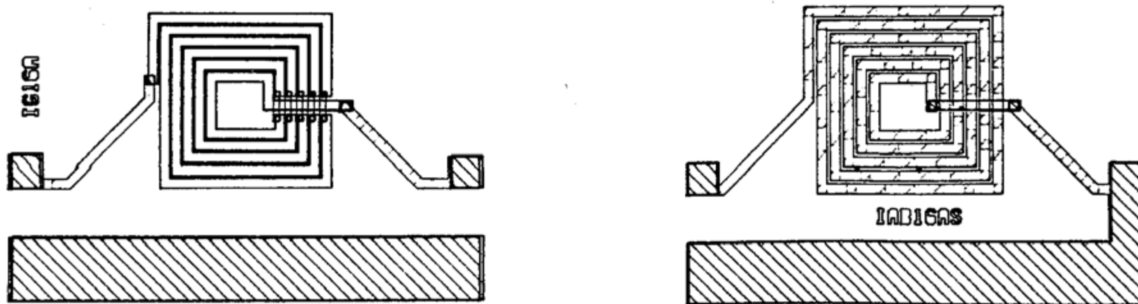


Fig. 2.5 Layout of standard and air bridge spiral inductor.

One port S parameter measurements have been taken, from 45 MHz to 3.045 GHz for the two different type inductors. The S parameter data are then converted to one port series impedance, Zin. Inductor Q is calculated as the ratio of the imaginary part of Zin to the real part of Zin and then plotted from 45 MHz to 1.5 GHz (Fig. 2.6 (a), (b)). Inductor Q shown in Fig. 2.6 (a), (b) is frequency dependent. It is clear that inductor Q is strongly affected by the metal thickness (which related to metal loss) and substrate resistivity. In Fig. 2.6 (a), a family of 1.5 um thick inductor Q-curves with different substrate resistivities is plotted versus x-axis frequency. In Fig. 2.6 (b), a family of 3.5 um thick inductor Q-curves with different substrate resistivities is plotted versus frequency.

The results in Fig. 2.6 (a), (b) show that the maximum Q (Q_{max}) of 3.5 um thick metal inductors is significantly higher than 1.5 um thick metal inductors, clearly indicating thicker metal results in higher Q_{max}. One the other hand, for the fixed metal thickness, the inductor Q_{max} and f_{sr} (self resonate frequency) improves with higher substrate resistivity with the exception of two data points (inductors Q_{max} for substrates with resistivity of 0.5 Ω-cm and 5 Ω-cm will be explained later). With the 2 kΩ-cm substrate, inductor Q's are close to the inductor Q of GaAs substrate. This result confirms that both metal strip loss and substrate loss affect silicon inductor performance.

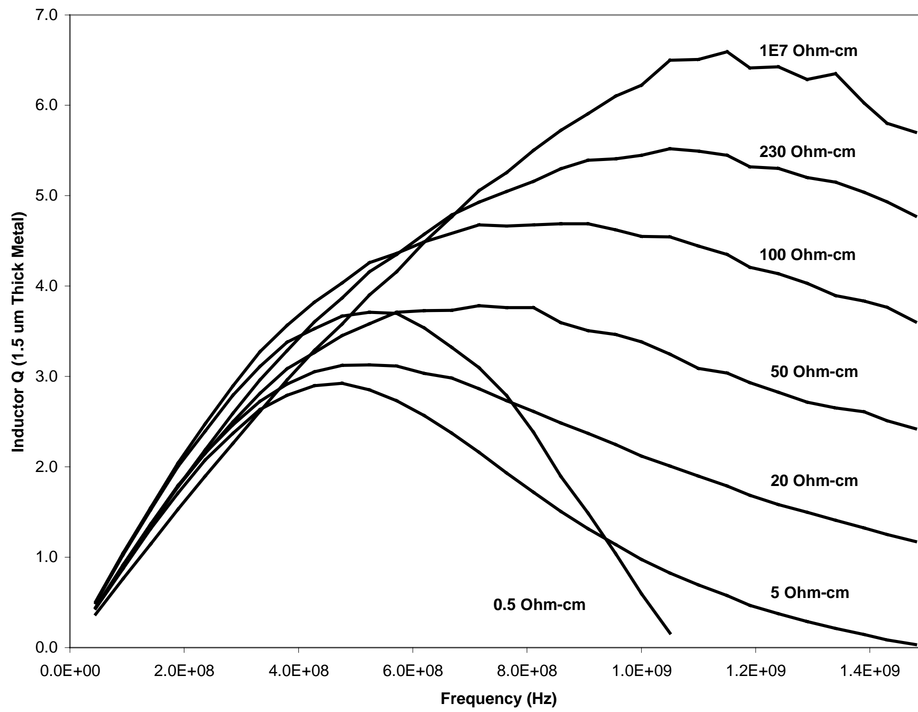


Fig. 2.6 (a) Measurement of 1.5 um thick metal inductor.

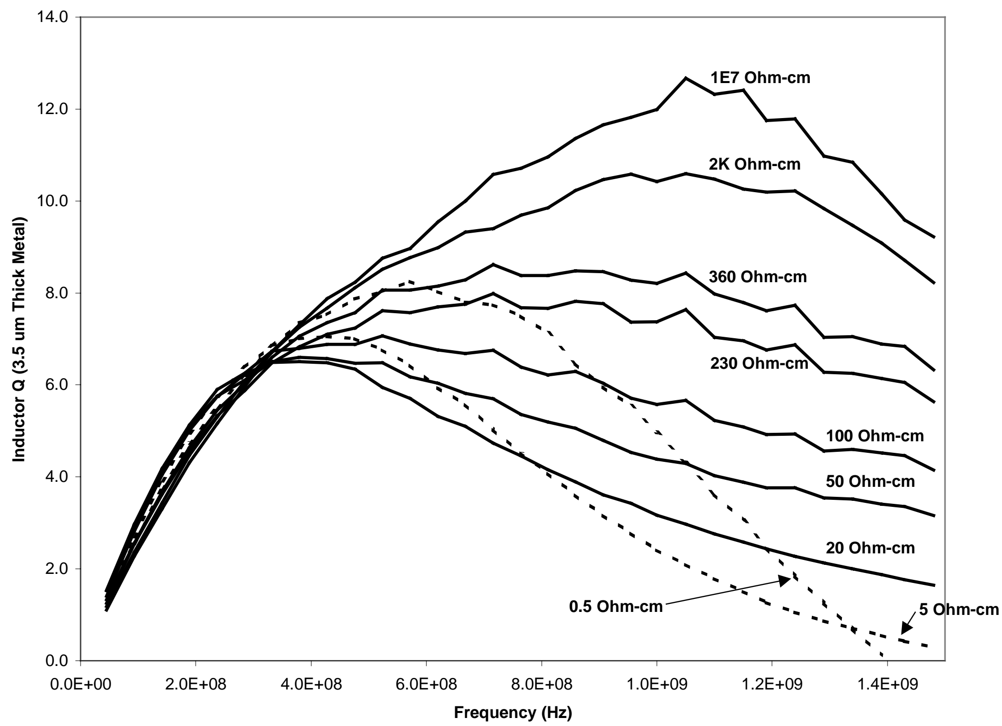


Fig. 2.6 (b) Measurement of 3.5 um thick metal inductor.

The inductor metal strip loss and substrate loss can be explained by inspecting the inductor circuit model (Fig. 2.7). At low frequency, all parasitics of the inductor (C_{OX}, C_P, R_B, C_B) in Fig. 2.7 become irrelevant, leaving only intrinsic inductor series with metal DC resistance. Inductor Q is linear function of signal frequency.

$$Q = \frac{j\omega L}{R} \tag{2.3}$$

As frequency of the signal increases, inductor Q will increase as well, but frequency dependent metal strip loss and the parasitics of the inductor start affecting more and more the inductor's electrical behavior. Frequency-dependent metal-strip loss (R) increases with frequency. Electrical coupling from the inductor metal strip to the silicon substrate (C_{OX}) and the inter winding coupling (C_P) effect increases with frequency, leading Q to peak, and then starting falling afterwards. Ultimately Q will fall to zero where the parasitic capacitance (C_P, C_B) resonates with intrinsic inductor at self resonate frequency f_{sr}.

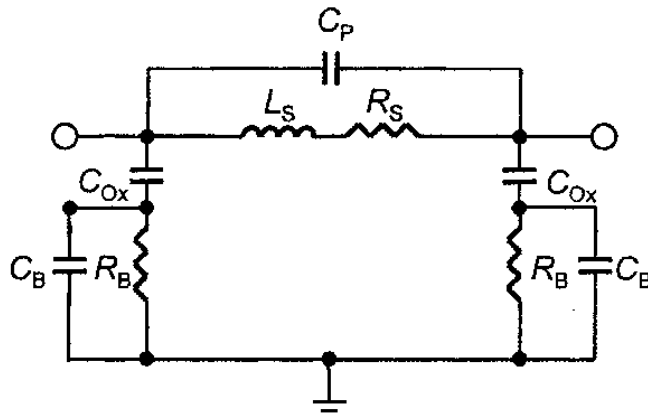


Fig. 2.7 Inductor model.

1) Metal strip loss

Metal strip losses include DC ohmic loss and frequency dependent loss. At DC the current in the metal strip is uniform distributed, only ohmic loss exists. However, as frequency increases, the current density becomes nonuniform. Two frequency dependent effects occur at high frequencies: skin effect and proximity effect. Skin effect is a well known high frequency effect, it pushes the AC current to the surface of a meal strip. In addition to the skin effect, the magnetic field generated by neighboring metal strips further changes the metal strip current distribution and results in a higher current density at the inner edge of the metal strip specially at inner turn of the inductor. This is described as the proximity effect and has a great impact on the increase of high frequency resistance of the metal strips (Fig. 2.8) [19]. In order to reduce metal strip losses, stacking multiple metal layers to form one effective thicker metal strip can significantly increase Q. More conductive copper also has been used in recent years to replace traditional aluminum material to improve the inductor performance (Fig. 2.9) [20].

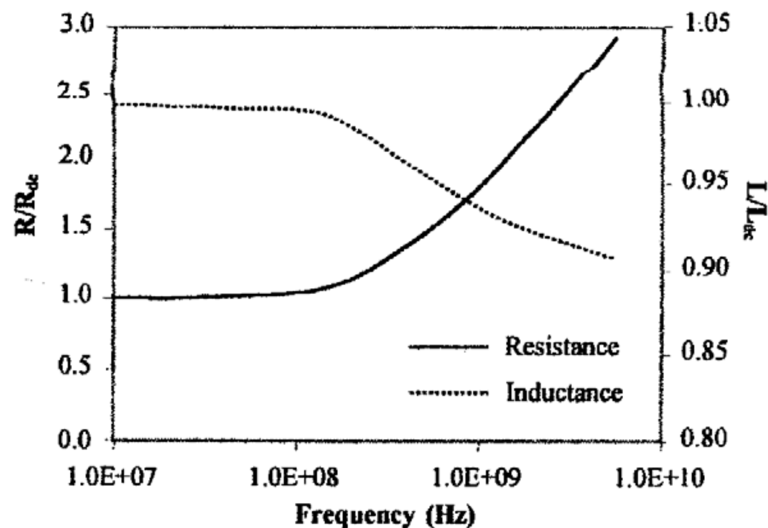


Fig. 2.8 Current-crowding frequency-dependent R(f) and L(f) characteristics.

Normalized resistance and inductance. (R_{dc}=0.19 Ω, L_{dc}=3.7 nH.)

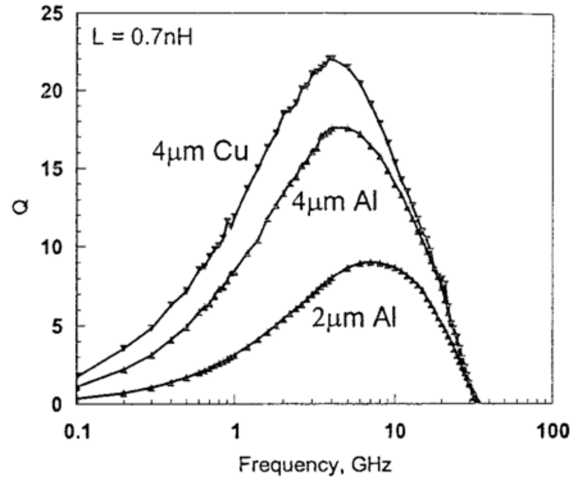


Fig. 2.9 Q factor as a function of metal and thickness (® 2001 IEEE) [20].

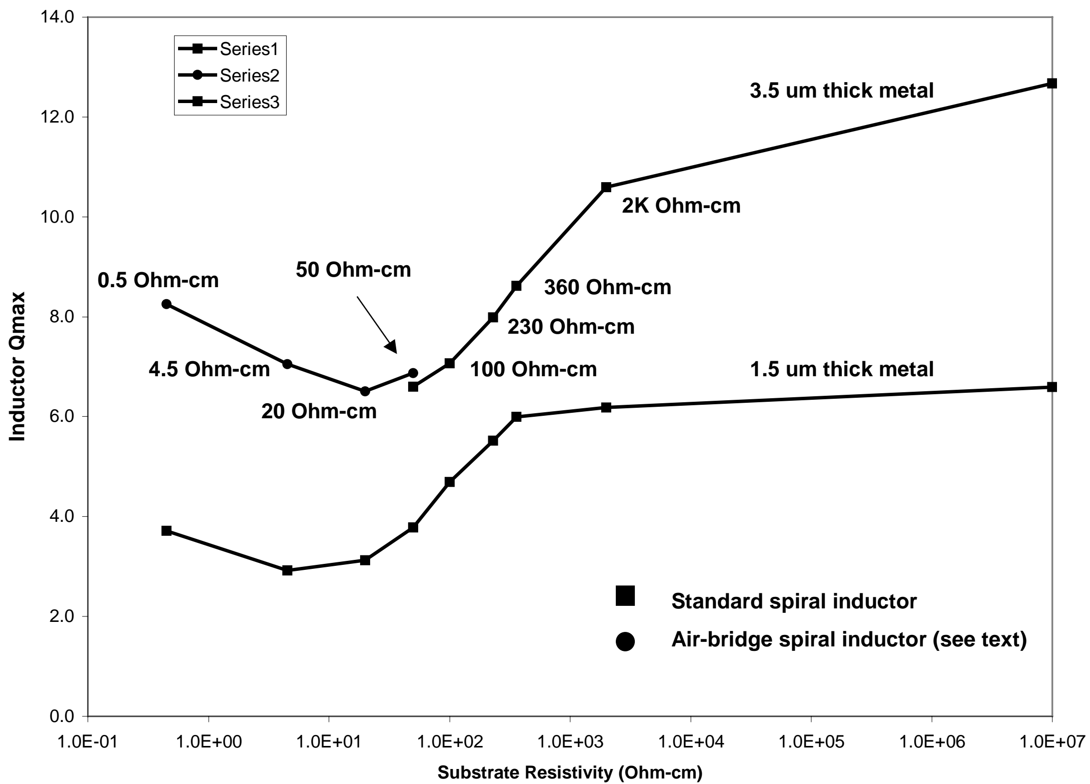


Fig. 2.10 Inductor Qmax is plotted as a function of substrate resistance for two different thickness metals. For resistivity ≤ 50 Ω-cm, air bridge inductors are used. For resistivity ≥ 50 Ω-cm, standard inductors are used.

2) Substrate loss

Since the spiral inductor is fabricated on a conductive silicon substrate in a CMOS process, the substrate further reduces the inductor's performance, affecting its Q, f_{max}, f_{sr}. This effect is primarily due to ohmic loss (I^2R) caused by the electric field penetration into the silicon substrate through C_{ox}. For the substrate with resistivity less than 1 Ω-cm, substrate eddy current induced by the magnetic field (not included in Fig. 2.7 circuit equivalent model) may also impact the inductor's performance [12], [19].

The result of Q_{max} of inductors versus substrate resistivity in our research is shown in Fig. 2.10. Fig. 2.10 is based on Q_{max} data from Fig. 2.6, the trend of inductor Q_{max} improvement with increasing substrate resistivity is observed (Fig. 2.10). Both standard and air bridge inductors are measured at substrate resistivity of 50 Ω-cm as shown in Fig. 2.10. Although the air bridge design raised the inductor an additional 3 um above the substrate as compared to the standard inductor, it had little effect on the value of Q_{max} .

In view of inductor Q_{max} improvement with higher substrate resistivity ($\rho \geq 20$ Ω-cm), one would expect the inductor Q_{max} to decrease as the resistivity decreases with substrate resistivity of 5 Ω-cm and 0.5 Ω-cm. On the contrary, as we can see, Q_{max} actually increases as the resistivity decreases at this region. This phenomenon is observed in inductor model simulation and explained by recent research [12]. The reason for this is that the energy loss caused by R_B in the parasitic capacitors is actually decreased with 0.5 Ω-cm substrate compared to 5 Ω-cm substrate. Therefore inductor Q_{max} increased.

By definition, the Q for a one port inductor is determined by the energy stored in the inductor (and parasitic capacitors) divided by the energy lost per cycle in the parasitic resistors. At high substrate resistivity ($\rho \geq 20$ Ω-cm), R_B (Fig. 2.7) is relatively large, electric energy is stored in C_{ox}, C_B. R_B is in parallel with C_B and introduces losses to the energy stored in C_B. Decreasing the substrate resistivity would cause smaller R_B, so more loss is introduced and the inductor Q decreases. When the resistivity of the substrate is decreased to 5 Ω-cm, R_B is small enough that C_B no longer plays a role in storing energy. Then C_{ox}, the much larger capacitor, now in series with smaller R_B, determines the stored electric energy. Therefore, the smaller resistivity yields smaller R_B and smaller loss from $C_{ox.}$ Q_{max} increases. But further decreasing substrate resistivity would not further increase Q_{max} because eddy current in the substrate starts to reduce the inductance by generating a magnetic field that oppose the magnetic field in the inductor.

3) Inductor performance optimization

The results of our research and other publications cited above indicate that silicon inductor performance is strongly affected by the metal loss and substrate loss. Increasing metal thickness to reduce metal loss could significantly improve inductor Q for RF applications. To reduce substrate losses, current RF CMOS integrated circuits use higher resistivity (~10 Ω-cm) substrate to replace the traditional low resistivity (~0.01 Ω-cm) substrate. Besides metal thickness and substrate resistivity, a CMOS inductor's performance is also affected by the oxide thickness beneath the inductor and its lateral dimensions, such as metal strip width, spacing, and outer diameter. To optimize inductor performance for a specific RF application in limited layout area, accurate inductor

modeling is necessary. Although several approaches have been proposed to calculate the inductor model parameters ([19], [21], [22], [23]), the accuracy of various methods to model the inductor for RF design still needs to be improved. However simulation results based upon these models could provide useful guidelines to achieve optimum inductor design for given RF applications. By using multiple metal layers to form single effective metal strip and thicker oxide over substrate, inductors Q on silicon has been significantly improved and inductors have been extensively used in current RF CMOS integrated circuits.

4) Current research

Although early research [24] suggested that removing the silicon substrate underneath an inductor could effectively eliminate substrate effect, it is not compatible with current standard CMOS process. As an effort to further reduce CMOS substrate effect, such as on chip cross talking through the silicon substrate and the substrate loss, the use of even higher resistivity substrate ($\rho > 1$ KΩ-cm) material for RF CMOS process has been recently reported [9].

Chapter 3 Capacitors and Resistors in a CMOS Process

There are a few different types of capacitors and resistors in a CMOS process. Capacitors have been used in analog CMOS integrated circuits for a long time. But the traditional CMOS process did not offer good RF capacitors. Resistors are seldom used in traditional CMOS integrated circuits. So caution is recommended when those components are used in RF integrated circuits.

3.1 Capacitors

Capacitors are frequently used in RF circuits. In RF oscillator circuits, capacitors and inductors form the resonant tank circuits to resonate at specified frequency (Fig. 3.1). Capacitors are also used with resistors to form various filters in RF circuits to perform frequency selection. Unlike inductors, capacitors in CMOS technologies can be fabricated in several ways and the quality factor Q of some of them is also much higher.

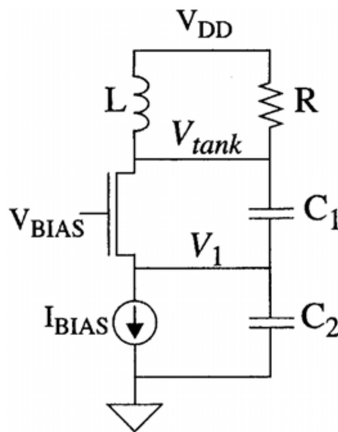


Fig. 3.1 Colpitts oscillator (Reprinted with the permission of Cambridge University Press) [25].

1) The MOS capacitor

Without process modification, the only capacitor available in traditional CMOS process is an MOS capacitor. The MOS capacitor simply uses MOS FET gate capacitance (Fig. 3.2 (a)) for the capacitor formation. A MOS FET gate forms one plate and the source, drain and channel form another. Because of the thin gate oxide, the MOS capacitor can provide large capacitance per unit area (1~5 fF/um^2) [25]. But this capacitor is gate voltage dependent, so when using an MOS capacitor it is important to keep the transistor in strong inversion; otherwise, the capacitance will be small, lossy, and highly nonlinear. Even if biased in the inversion region, the large serial channel resistance and parasitic capacitance (not shown) (Fig. 3.2 (b)) of the MOS capacitor result in a low quality factor Q. Therefore the MOS capacitor is only used in non-critical application when high capacitance is desired.

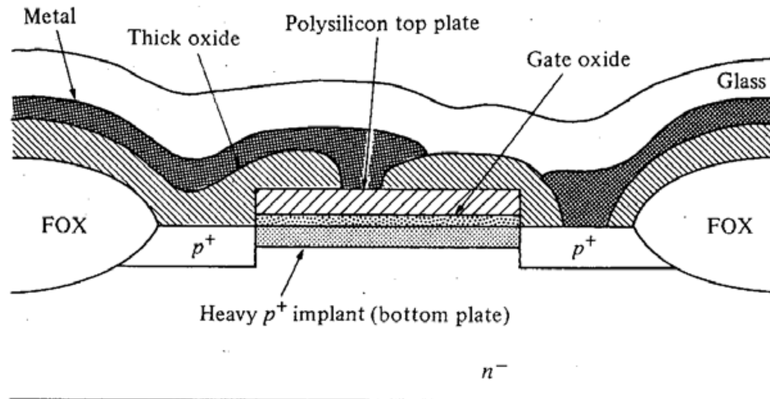


Fig. 3.2 (a) MOS capacitor: Polysilicon-oxide-channel.

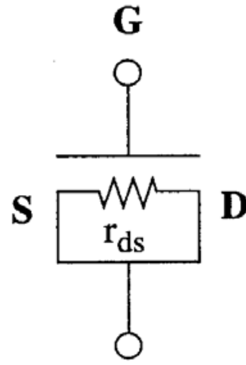


Fig. 3.2 (b) Gate capacitor model (Reprinted with the permission of Cambridge University Press) [25].

2) Poly-Poly capacitor

Many MOS technologies used to implement analog functions have two layers of polysilicon (Fig. 3.3). An additional top layer of polysilicon can be used to form poly-poly capacitors with a bottom polysilicon gate. The plate separation is usually comparable to the gate oxide thickness of the MOS transistors, so similar capacitance density can be obtained in a poly-poly capacitor, but with much less voltage dependence compared with the MOS capacitor. The poly-poly capacitor's series resistance is moderate, but a large parasitic capacitance associated with the poly-poly capacitor exists from bottom plate to the underlying layer, which could be either the substrate or a well diffusion. This bottom plate parasitic capacitance is proportional to the bottom plate area and typically has a value from 10 to 30 percent of the capacitor itself [26]. This parasitic capacitance often severely limits circuit performance.

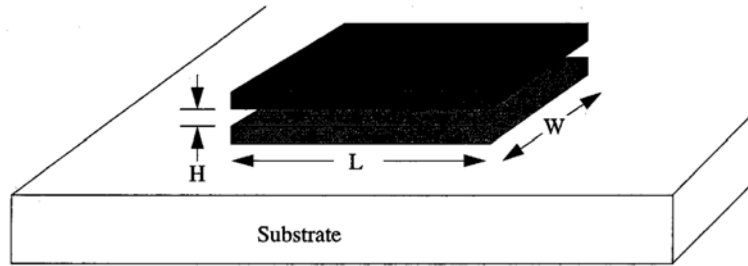


Fig. 3.3 Poly-Poly parallel plate capacitor (Reprinted with the permission of Cambridge University Press) [25].

3) MIM (Metal-Insulator-Metal) capacitor

All of the interconnect layers may be used to make plate capacitors, much like the poly-poly capacitor mentioned earlier. A key disadvantage of such capacitors, however, is that the capacitance per unit area is small because the oxide used to isolate one layer from another is rather thick (0.5~1 um). Therefore, such capacitors usually occupy a large area, which waste the valuable real estate of an integrated circuit.

In order to reduce the area of the overall die, thinner dielectrics and higher dielectric constant materials have been pursued, but then additional process steps need to be added to the CMOS process. MIM capacitance densities of 2.7 fF/um^2 with Q's of 150 were recently reported by using nitride dielectric [7]. Since the MIM capacitor is made from metal, its series resistance is low. In turn, the capacitor's Q is high. In a multiple metal layer process, the capacitor can be placed high up, allowing significant reduction of the parasitic capacitance to the substrate when compared to a poly-poly capacitor.

4) Lateral capacitor

To reduce the capacitor area in a standard digital CMOS process without introducing extra process steps, a lateral capacitors can be used. This capacitor is formed by electrical coupling between adjacent metal lines within same metal layer (Fig. 3.4). As can be seen in (Fig.3.4), two terminals of the capacitor are labeled P1 and P2. As technologies evolve to reduce feature sizes, the minimum adjacent metal spacing shrinks but thickness changes little; therefore, the die area required for a given lateral capacitance decreases in scaled technologies. Lateral capacitors can be used in conjunction with vertical capacitors by arranging the segments of a different metal layer in a complementary pattern.

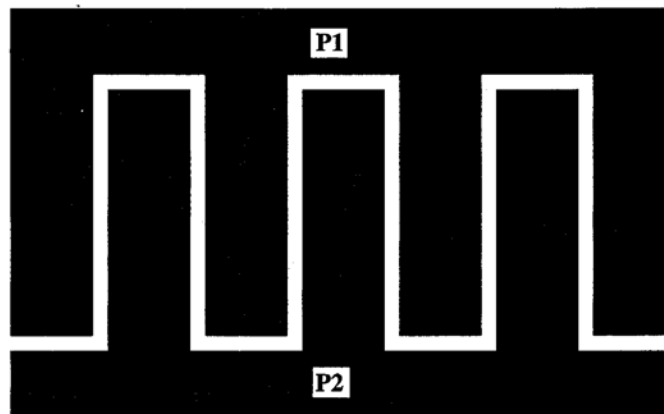


Fig. 3.4 Example of lateral flux capacitor (Reprinted with the permission of Cambridge University Press) [25].

3.2 Resistors

There are a few different resistors in a CMOS process. The choice of resistor generally depends on the value, tolerance, temperature coefficient, and parasitic capacitance of the resistor.

1) Poly resistor

In silicon-gate MOS technologies, at least one layer of polysilicon is required to form the gates of the transistors, and this layer is often used to form resistors. Most polysilicon layers in current MOS technologies is silicided to reduce resistance. The nominal sheet resistance of this layer is on the order of 5 Ω/sq, so polysilicon is appropriate mainly for moderate small value resistors. It's tolerance is often poor (e.g., 35%), and it's temperature coefficient is typical about 1000 ppm/°C. A poly resistor exhibits a reasonably low parasitic capacitance to the substrate and its resistance is almost independent of the voltage across its terminal.

2) Diffused resistor

The diffused layer used to form the source and drain of the n-channel and p-channel devices can be used to form a diffused resistor. Its resistivity and temperature coefficient are similar to the poly resistors. But its parasitic (junction) capacitance is significantly higher and also voltage dependent. This limits the useful frequency range of the resistor and the dynamic range of voltages applied. Additionally, care must be taken to avoid forward biasing at either end of the resistor.

3) Well resistor

A well may be used to form high value resistors. A relatively lightly doped well region provides a sheet resistance on order of 10 kΩ/sq. Unfortunately, there are many

undesired properties with this resistor. A well resistor displays a large tolerance (~50%), a high temperature coefficient (~3000 ppm/°C), and a high voltage coefficient. The PN junction formed between the well and the substrate results in substantial parasitic capacitance.

4) MOS transistor as a resistor

An MOS transistor biased in the triode region can be used to perform the function of a resistor. The drain-source resistance can be derived by differentiating the equation for drain current in the triode region with respect to the drain-source voltage.

$$R = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu C_{ox}} \cdot \frac{L}{W} \cdot \frac{1}{(V_{GS} - V_t - V_{DS})} \qquad (3.1)$$

This equation shows that the value of an MOS resistor can be controlled by gate bias. In some applications, this resistor can be used in feedback loop to realize certain gain control. Another advantage of the MOS resistor is that a large value resistor can be realized in a small area by properly biasing the gate voltage. Both features have been used in our later design practice. The principle drawback of this resistor is the high degree of non-linearity; that is, the drain-source resistance is not constant but depends on the drain-source voltage. As one can expect, when drain-source voltage is large enough, the MOS transistor would enter a saturation region and the drain-source resistance would become very large despite the gate bias.

Chapter 4 Interconnect Line on an MOS Silicon Substrate

A CMOS integrated circuit is made up of passive and active components connected by on-chip interconnect lines, all of which are fabricated on a common silicon substrate. In the early years of CMOS integrated circuits, the resistance of interconnections and parasitic capacitance between interconnect line and substrate-ground were ignored because the circuit speed and bandwidth was low. Their existence was insignificant to the circuit performance. As the minimum feature size of the integrated circuits technology was reduced, the maximum circuit speed and bandwidth have steadily increased. As a result, the wave length is significantly shorter and close to the magnitude of the circuit scale; resistance and parasitic capacitance of the interconnections start to have significant impact on circuit performance. For instance, for frequency f equal to 1 GHz, the signal wave length λ_0 at speed of light (3×10^{-8} m/s) in free space would be

$$\lambda_0 = \frac{c}{f} = \frac{3\times10^8\,\mathrm{m/s}}{10^9\,\mathrm{Hertz}} = 0.3\mathrm{m} \tag{4.1}$$

If the signal of same frequency is transmitted over an MOS microstrip interconnect line with effective dielectric constant ε_{eff} (ε_{eff} = 9 for GaAs, for instance), then the signal wave length, λ would be shrunk to

$$\lambda = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} = \frac{\lambda_0}{3} = 0.1\mathrm{m} \tag{4.2}$$

The higher the frequency the shorter the signal wave length and when the signal wave length gets closer to the physical size of the interconnect line in dimension, the

interconnect line starts showing transmission line properties. Transmission line theory has to be used to analyze the interconnect-line effect.

On medium radio frequency (<1 GHz) integrated circuits, interconnect lines of the circuit are modeled as discrete resistor-inductor-capacitor RLC networks in the circuits. On higher RF integrated circuits however the simple RLC network model is inadequate to account for interconnect line effects for circuit performance. The silicon substrate can no longer be treated as ideal ground. Loss introduced by the substrate needs to be included in the interconnect line circuit model. Effect of MOS single microstrip line, the simplest and most frequently used form of interconnect line, on the circuit performance will be analyzed. Circuit models for an MOS microstrip line at different frequency ranges will be discussed.

4.1 Medium frequency model

The microstrip line in Fig. 4.1 has been extensively used in CMOS integrated circuits. The substrate is made of silicon. A metallization layer is generally sputtered on the bottom of the substrate to form an electrical ground and heat transfer media. Its thickness and conductivity (or resistivity) is determined by the component requirements. The oxide layer insulates the substrate from the microstrip line conductor. Both metal and poly-silicon material could be used for the line conductor, however a metal conductor has a much higher electrical conductivity than does poly-silicon material, and therefore suffers less loss.

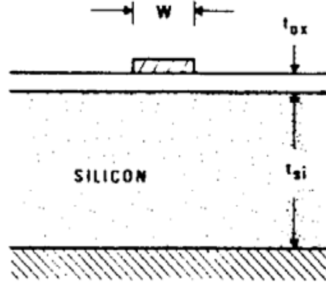


Fig. 4.1 Microstrip cross section (® 1982 IEEE) [27].

The effect of a microstrip line on the circuit performance is due to the line conductor finite resistance, inductance and parasitic conductance, and capacitance from the line to ground. These distributed series line resistance (R), inductance (L), shunt parasitic conductance (G), capacitance (C) form a transmission line (Fig. 4.2).

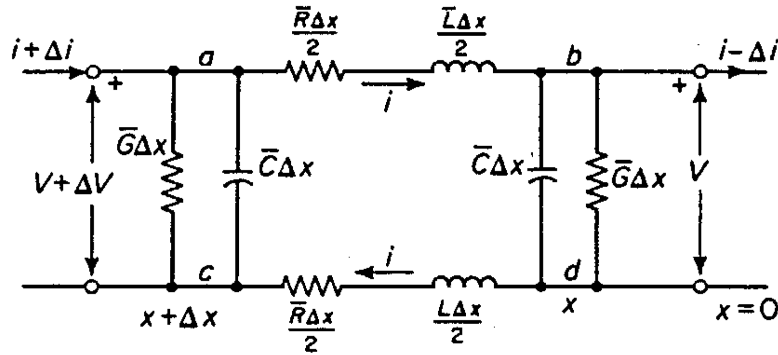


Fig. 4.2 Incremental length of a transmission line with losses.

The voltage and current at terminals of a microstrip line could be described by a transmission line equation,

$$V(l) = V_2 \cosh(\gamma l) + I_2 Z_0 \sinh(\gamma l) \tag{4.3}$$

$$I(l) = I_2 \cosh(\gamma l) + \frac{V_2}{Z_0} \sinh(\gamma l) \tag{4.4}$$

where $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$ (4.5)

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}\,. \tag{4.6}$$

Here γ is transmission line propagation coefficient, α and β is the attenuation coefficient and phase coefficient respectively. Z_0 is the transmission line characteristic impedance. R, L, G, C are distributed line parameters for the transmission line. R and L are resistance and inductance per unit length in series. G and C are shunt conductance and capacitance per unit length for the microstrip transmission line. At medium frequency range (<1 GHz), the conductance from the conductor line to the ground is negligible. Therefore at this frequency range the microstrip can be treated as a transmission line formed by distributed resistance R, inductance L, capacitance C.

In reference [27], the authors suggested that at frequency $f < 1$ GHz, the silicon substrate would behave as a perfect conductor for the electric field, the substrate loss is negligible, but is a rather poor conductor for the magnetic field [28]. Based on these assumptions, the authors [27] proposed an RLC circuit model for the subsection of an MOS micostrip transmission line (Fig. 4.3). Indeed the authors [29] study confirmed the validity of the assumptions. The circuit parameters of the model for the subsection of microstrip line could be calculated as from (4.7) to (4.10).

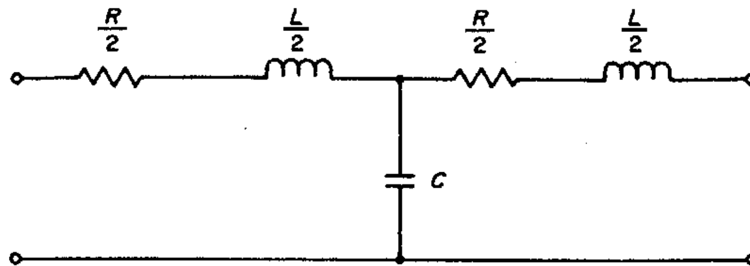


Fig. 4.3 Interconnect medium frequency circuit model.

$$R = \frac{L}{W} R_{sh} \quad , \tag{4.7}$$

$$L = \frac{\mu_0}{2\pi} \ln\left(\frac{8(t_{ox} + t_{Si})}{W} + \frac{W}{4(t_{ox} + t_{Si})} \right) \quad , \tag{4.8}$$

$$C = \frac{2\pi \varepsilon_{eff} \varepsilon_0}{\ln\left(\frac{8t_{ox}}{W} + \frac{W}{4t_{ox}} \right)} \quad , \qquad W \le t_{ox}$$

$$C = \varepsilon_r \varepsilon_0 \left[\frac{W}{t_{ox}} + 2.42 - 0.44 \frac{t_{ox}}{W} + \left(1 - \frac{t_{ox}}{W} \right)^6 \right] , \qquad W \ge t_{ox} \tag{4.9}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + \frac{10t_{ox}}{W} \right)^{-(1/2)} \quad . \tag{4.10}$$

Rsh is the DC sheet resistance of the line conductor. ε_r is relative dielectric constant of silicon oxide. ε_{eff} is effective relative dielectric constant of silicon oxide for a narrow microstrip line. ε_0, μ_0 are the permittivity and the permeability of free space. For a 250 um thick silicon substrate, 1 um thick oxide, the calculated line inductance L and line capacitance C of a single microstrip are presented (Fig. 4.4 (a), (b)) [27]. The sheet resistance Rsh of a typical aluminum metal line is 0.1 Ω/sq.

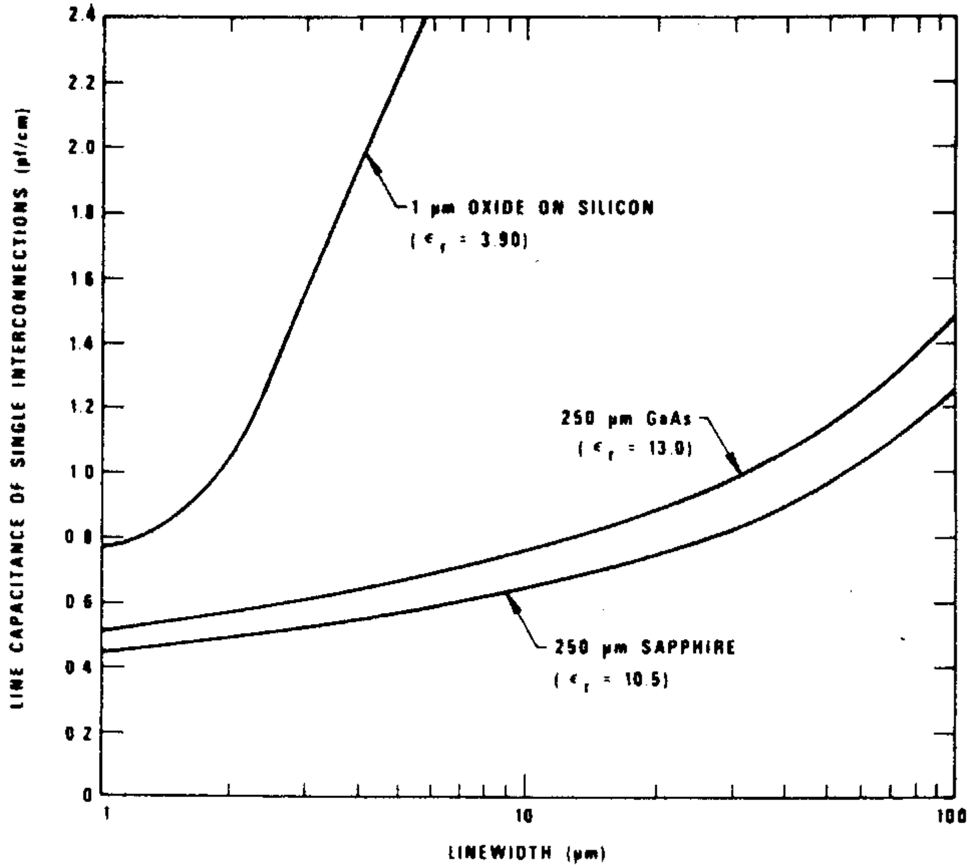


Fig. 4.4 (a) Calculated interconnection capacitance on oxide-passivated silicon, sapphire, and semi-insulating gallium arsenide substrates (® 1982 IEEE) [27].

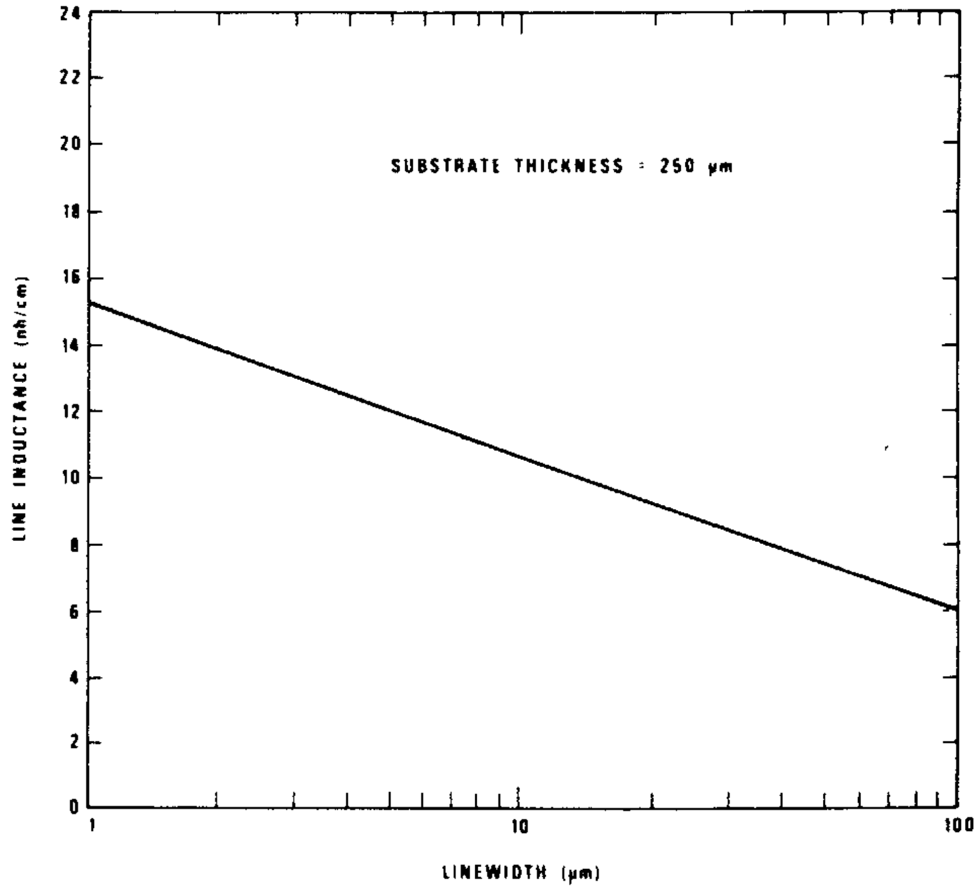


Fig. 4.4 (b) Calculated interconnection inductance on oxide-passivated silicon, sapphire, and semi-insulating gallium arsenide substrates (® 1982 IEEE) [27].

4.2 High frequency model

For CMOS integrated circuits operating beyond a 1 giga Hertz range the microstrip model mentioned above is inadequate to predict circuit performance [30]. The microstrip interconnect has greater impact on circuit performances. Microstrip line conductor skin effect and silicon substrate loss can not be ignored. Their effects need to be included into the model in order for the simulation to reflect reality. The references ([27]-[29], [31], [32]) reflect many researchers work on interconnect line phenomenon on (MIS) metal-insulator (silicon oxide)-semiconductor structure (or MOS structure) over the past forty years. The authors [31] study revealed the dispersive nature of signal propagation on a MIS microstrip line. The authors [28] further confirmed this by experiment and proposed a transmission line subsection circuit model for it. The authors [32] modified the circuit model (Fig. 4.5) to include the substrate dielectric loss. In addition [32] used a different approach to calculate series line resistance with skin effect. The equations to calculate circuit parameters are presented below.

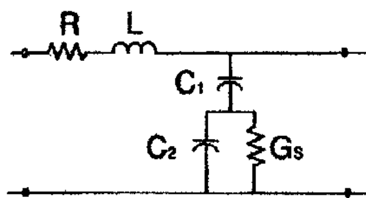


Fig. 4.5 Interconnect high frequency circuit model (® 1993 IEEE) [32].

$$R = \begin{cases} R_{DC} \quad ; \quad ------------------ \quad \text{if} \quad R(f) < R_{DC} \\ R(f) = \dfrac{\rho_m}{\delta_m \left\{1 - \exp\left(-\dfrac{t_m}{W}\right)\right\}\left(1 + \dfrac{t_m}{W}\right)}\left(\dfrac{1}{W}\right) \quad ; \quad \text{if} \quad R(f) > R_{DC} \end{cases} \tag{4.11}$$

$$L = \mu_0 \cdot F(t_{ox} + t_{Si}, W) \tag{4.12}$$

$$C_1 = \frac{\varepsilon_0 \varepsilon_{eff}(t_{ox}, \varepsilon_{SiO_2})}{F(t_{ox}, W)} \tag{4.13}$$

$$C_2 = \frac{\varepsilon_0 \varepsilon_{eff}(t_{Si}, \varepsilon_{Si})}{F(t_{Si}, W)} \tag{4.14}$$

$$G_2 = \frac{1}{2} \cdot \frac{\sigma_{Si} \cdot \left[1 + \left(1 + \dfrac{10 t_{Si}}{W}\right)^{-1/2}\right]}{F(t_{Si}, W)} \tag{4.15}$$

$$\delta_m = \frac{1}{\sqrt{\pi f \mu_0 \mu_m / \rho_m}} \tag{4.16}$$

$$\varepsilon_{eff}(t_i, \varepsilon_i) = \frac{\varepsilon_i + 1}{2} + \frac{\varepsilon_i - 1}{2}\left(1 + \frac{10 t_i}{W}\right)^{-(1/2)} \tag{4.17}$$

$$F(t_i, W) = \begin{cases} \dfrac{1}{2\pi} \ln\left(\dfrac{8 t_i}{W} + \dfrac{W}{4 t_i}\right) \quad ; ---------- \quad \dfrac{t_i}{W} > 1 \\ \left[\dfrac{W}{t_i} + 2.42 - 0.44\dfrac{t_i}{W} + \left(1 - \dfrac{t_i}{W}\right)^6\right] \quad ; \quad \dfrac{t_i}{W} \le 1 \end{cases} \tag{4.18}$$

Here ρ_m is the line conductor resistivity; δ_m is the conductor skin depth. μ_m is relative permeability of the conductor. σ_{Si} is the conductivity of silicon substrate. t_i, ε_i are thickness and relative dielectric constant respectively for either silicon dioxide or silicon

substrates. ε_{eff} is the effective relative dielectric constant for either silicon oxide or silicon substrate for a narrow microstrip line. ε_0, μ_0 are the permittivity and the permeability of free space.

By inspecting these equations, we observed that series line resistance R is frequency dependent through the skin depth δ_m. In addition to that, a frequency dependent dielectric losses of the substrate and fringing effects are introduced (by other equations not presented here) into the capacitor C_2 calculation [32]. Generally the frequency dependent parameter model is difficult to handle for circuit simulation tools. In the proposed model in reference [29], only the series line resistance R is frequency dependent. It is further suggested that the series line inductor be replaced with a series-shunt network. This is a circuit model with all frequency independent components and works well for a microstrip line up to 10 GHz.

Chapter 5 Optic Preamplifier Design with a CMOS Process

As discussed in the Introduction and in Chapter 1, when modern CMOS processing is advanced to 0.5 um and shorter feature size technologies, its transistor gain and operating frequency is high enough to be used in RF integrated circuits. To evaluate the RF performance of modern CMOS technology, we designed an optic preamplifier as a test vehicle using a 0.5 um CMOS process. A test circuit has been fabricated and tested. The measurement data confirmed the designed specifications. The circuit performance with a more advanced 0.35 um CMOS process has been evaluated by circuit simulation as well.

5.1 Transimpedance amplifier introduction

An optic preamplifier is a wide-band low-noise amplifier. It is a critical front-end building block for a fiber optic receiver in fiber optic communication systems (Fig. 5.1). Optical pulses traveling from an optic fiber link that reach photo diode (PD) in the optic receiver generate electric current (I_d) pulses. This electric current is converted to a bigger voltage signal by a wide-band low-noise amplifier. Since the amplifier converts input current to output voltage it is called a transimpedance amplifier (TIA). It is widely used

Fig. 5.1 Simplified fiber optic communication system [47].

as a core for optic preamplifier circuits. Besides transimpedance amplifiers, other circuit topologies such as a high input impedance amplifier can also be used as an optic preamplifier. In our research only the transimpedance amplifier topology is used.

The block diagram of a transimpedance amplifier is usually represented as a shunt-shunt feedback amplifier with one gain stage (Fig. 5.2). The feedback resistor (R_F) represents the gain of the transimpedance amplifier, a measure indicating how big the voltage signal the TIA can produce at the output for a given input current. The photo diode driving the transimpedance amplifier is represented by a current source I_d and the junction capacitance C_d. The input impedance of the TIA is

$$Z_{in} = \frac{R_F}{1 + A} \tag{5.1}$$

where A is the basic amplifier gain. The 3 dB bandwidth of the transimpedance amplifier is

$$BW = \frac{1 + A}{2\pi R_F C_d} \tag{5.2}$$

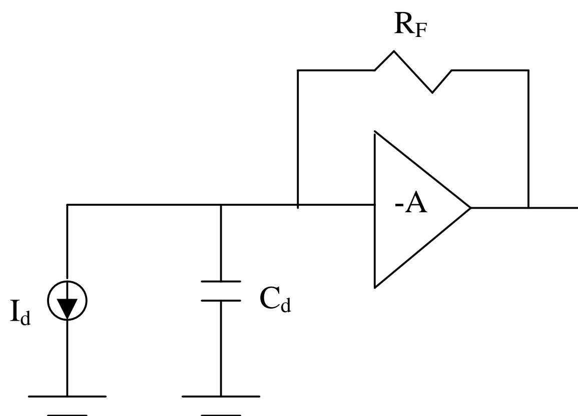


Fig. 5.2 Block diagram of a transimpedance amplifier.

As a preamplifier, the performance of the transimpedance amplifier determines to a large extent the performance of fiber optic receivers. Such an amplifier presents design challenges in the form of tradeoffs between noise, bandwidth, transimpedance gain and power consumption. The tradeoffs are discussed more in 5.3.

Traditionally, this transimpedance amplifier has been fabricated in GaAs technology [33]. Due to the progress of multimedia communication, high-speed optical communication systems are becoming increasingly important. The growing demand for increasing data transmission capacity in the commercial communication market has generated tremendous interest in low cost implementation of fiber optic receivers. This quest for low cost communication solutions and advancement of modern CMOS technologies has spurred a desire to implement transimpedance amplifiers in a standard CMOS process.

5.2 Previous works on CMOS transimpedance amplifier

There are a number of CMOS transimpedance amplifier circuit topologies reported in the past [34]-[36]. Among them, one of the earliest, an NMOS TIA circuit, was published in 1984 [34]. The author used an NMOS process with 0.45 um effective channel length for the transimpedance amplifier design (Fig. 5.3). A three-stage amplifier was chosen as the basic amplifier to get enough gain for noise and wide bandwidth purpose. A local feedback was used to maintain circuit stability. The size of the input FET of the transimpedance amplifier was optimized to minimize noise. 630 Ω transimpedance gain and 920 MHz bandwidth was reported. The circuit consumes 60 mA

from a 4.5 V power supply. By using separate (3 V) positive and (-2 V) negative power supplies, -25.4 dBm optical sensitivity with a PIN photo diode was obtained at 10^{-9} bit-error rate (B.E.R) for 1 Gbit/s operation.

Fig. 5.3 Abidi's transimpedance amplifier (® 1984 IEEE) [34].

In [35] the authors reported a transimpedance amplifier design with 0.8 um CMOS process. The transimpedance amplifier was designed with three CMOS inverters (Fig. 5.4). In order to maintain the circuit stability, high impedance nodes had to be taken care of. This was done by reducing the impedance of each high impedance nodes with loading FETs ($1/g_m$). g_m represents conductance of the loading FETs. The authors claimed that this transimpedance amplifier was tested at 240Mb/s and had a 150 KΩ transimpedance gain.

In [36] the authors designed their transimpedance amplifier with 0.6 um CMOS process. The transimpedance amplifier is preceded by a regulated cascode configuration as an input stage (Fig. 5.5). The intent is to make the input of the transimpedance

amplifier a virtual ground, so that the transimpedance amplifier bandwidth becomes less dependent on photo diode capacitance. The noise is also decreased. The amplifier was measured to have 800 Ω transimpedance gain, 950 MHz bandwidth. A 6.3 pA/$\sqrt{\text{Hz}}$ input equivalent noise current was also measured. The chip core consumes 85 mW from a 5 V supply. The drawback of regulated cascode configuration is that the input biasing resistor contributes a good portion of the noise to the total input-equivalent noise current.

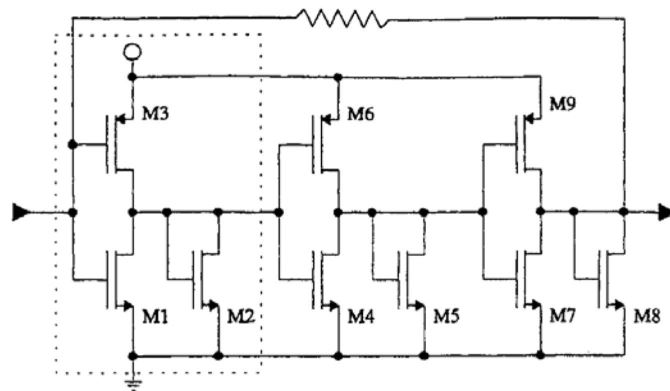


Fig. 5.4 Ingels's transimpedance amplifier (® 1994 IEEE) [35].

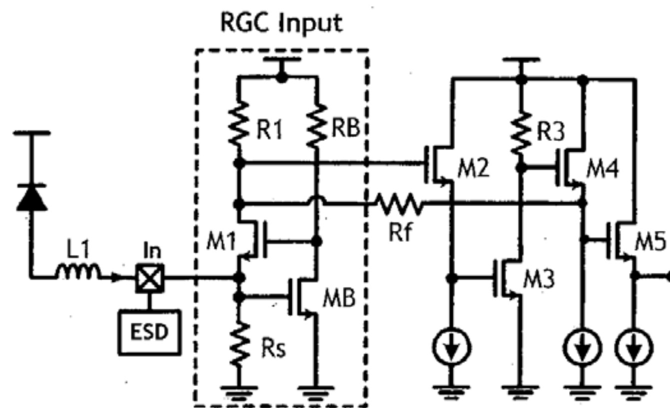


Fig. 5.5 Park's transimpedance amplifier (® 2004 IEEE) [36].

In our transimpedance amplifier design [41], a two gain-stage amplifier has been employed to get enough gain for the desired bandwidth. The choice of a lesser gain stage design compared to [34], [35] is in favor of circuit stability. The size of input FET of the transimpedance amplifier is optimized to minimize noise. The second gain stage uses a common gate configuration for its wide bandwidth characteristic. The FET gate-drain capacitance has been used for stability compensation.

5.3 Design of the Transimpedance Amplifier (TIA)

The transimpedance amplifier is the core of an optic preamplifier in the optical receiver front-end, whose main function is to provide enough gain for the subsequent stages (such as limiting amplifier). Any noise produced in this stage will be amplified and passed to the following stages. Therefore the transimpedance amplifier sets the minimum detectable signal level for the receiver. Noise analysis, noise bandwidth trade off, and a circuit description is presented first. Then the circuit simulation and measurement results follow.

5.3.1 Noise and Bandwidth

In the transimpedance amplifier block diagram shown in Fig. 5.6 (a), the transimpedance amplifier is represented by a negative feedback amplifier, which consists of one inverting amplifier stage for simplicity.

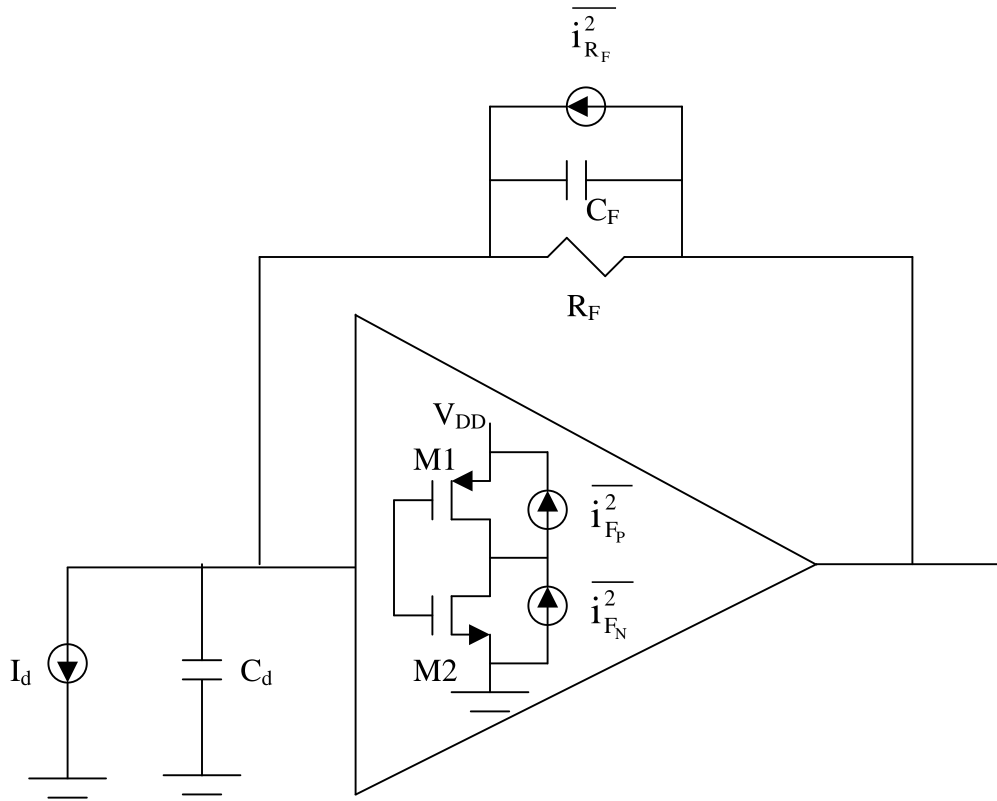


Fig. 5.6 (a) Block diagram of a CMOS transimpedance amplifier with noise sources.

It consists of active devices M1 and M2. The photo diode detector is represented by its equivalent circuit consisting of I_d and C_d. I_d is the signal current and C_d is the capacitance of the diode. There are three major noise sources represented by $\overline{i^2_{R_F}}$, $\overline{i^2_{F_N}}$ and $\overline{i^2_{F_P}}$, which are expressed as a noise spectral density. Noise $\overline{i^2_{R_F}}$ is generated by the feedback resistor R_F, $\overline{i^2_{F_N}}$ and $\overline{i^2_{F_P}}$ are generated by the input NMOS and PMOS inverter FETs. In order to indicate the equivalent amount of noise added to the signal coming to the input of the amplifier, input-referred noise current sources are usually used to

represent noise. They are $\overline{I^2_{R_F}}$, $\overline{I^2_{F_N}}$ and $\overline{I^2_{F_P}}$, which are expressed in terms of a noise power (Fig 5.6 (b)).

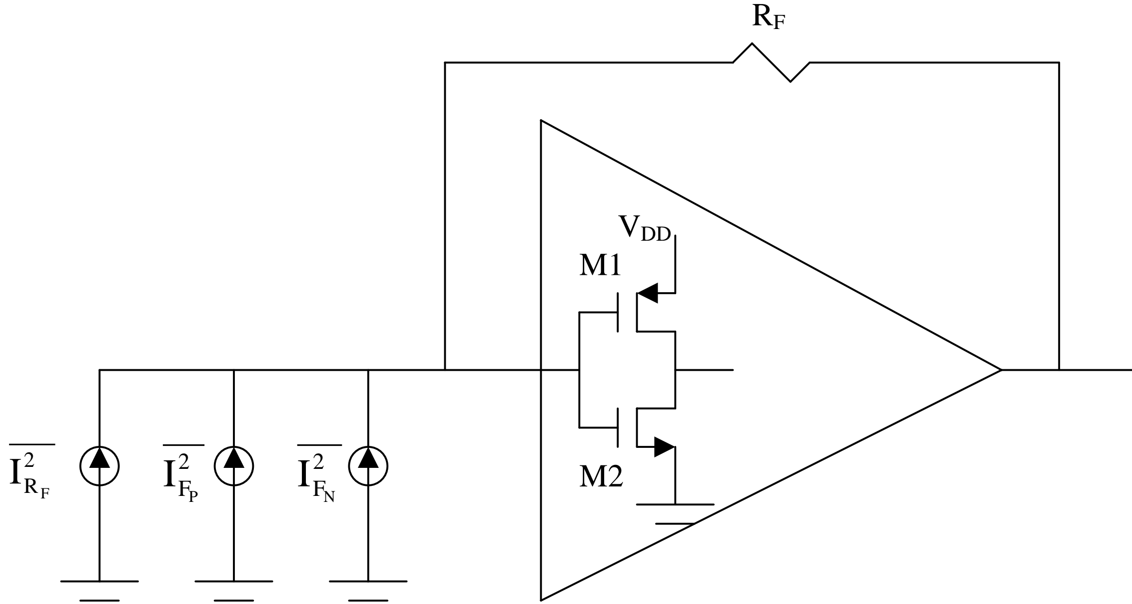


Fig. 5.6 (b) Noise sources have been reflected to the input.

$\overline{I^2_{R_F}}$ contributes same amount noise as $\overline{i^2_{R_F}}$ does at output of the amplifier. So does $\overline{I^2_{F_N}}$, $\overline{I^2_{F_P}}$ as $\overline{i^2_{F_N}}$ and $\overline{i^2_{F_P}}$. The input-referred noise source originating from the feedback resistor is given by

$$\overline{I^2_{R_F}} = \frac{4kTB}{R_F} \tag{5.3}$$

Where k is Boltzmann's constant. T is temperature in Kelvin. B is the bandwidth of interest. The input-referred noise sources originating from the input FETs are given by [34]

$$\overline{I_{F_N}^2} = \overline{i_{F_N}^2}\frac{(2\pi)^2 B^3 (C_{gs_1} + C_{gs_2} + C_d + C_{gd_1} + C_{gd_2} + C_F)^2}{3(g_{m_1} + g_{m_2})^2} \quad (5.4)$$

$$\overline{I_{F_P}^2} = \overline{i_{F_P}^2}\frac{(2\pi)^2 B^3 (C_{gs_1} + C_{gs_2} + C_d + C_{gd_1} + C_{gd_2} + C_F)^2}{3(g_{m_1} + g_{m_2})^2} \quad (5.5)$$

$\overline{i_{F_P}^2} = 4kT\Gamma_P g_{m_1}$, $\overline{i_{F_N}^2} = 4kT\Gamma_N g_{m_2}$. Γ_P, Γ_N are noise constant. g_{m_1}, g_{m2} are the M1 and M2 transconductances. C_{gs_1}, C_{gs_2}, C_{gd_1}, C_{gd_2} are the M1 and M2 gate-source capacitances and gate-drain capacitances. C_F is the parasitic capacitance of feedback resistor R_F. It is interesting to note that the Miller effect of capacitor C_{gd_1}, C_{gd_2} does not appear in the noise source terms.

From the above three equations we observe:

1) For given bandwidth B, low noise performance requires a large g_m and a small capacitance in the active devices.
2) From (5.3), a large value of R_F is desired to reduce the noise contribution from the feedback resistor.
3) Input-referred noise power due to resistor R_F increases linearly with bandwidth while input-referred noise due to FETs increases with the 3rd power of the bandwidth. It means that the R_F portion of the noise is more important for a low bit rate TIA, and becomes less important for higher bit rate TIA. Since the first TIA presented here works at 622 Mbit/s, a relatively low bit rate, choosing a large resistance value for feedback resistor R_F, to reduce its noise contribution, is very important. But another circuit requirement, bandwidth B, puts a constraint on the maximum value of R_F.

$$B = \frac{A}{2\pi R_F (C_{gs_1} + C_{gs_2} + C_d + A(C_{gd_1} + C_{gd_2} + C_F))} \quad (5.6)$$

This equation is essentially the same as (5.2). The $A(C_{gd_1} + C_{gd_2} + C_F)$ term comes from Miller effects. A is voltage gain of the basic amplifier. From the equation above, if we can have arbitrary large A, then we could choose arbitrary large resistance value of R_F to make its noise component negligible. A high voltage gain amplifier usually is a multiple stage amplifier which consists of multiple poles. If the transimpedance amplifier consists of such a multiple stage amplifier, stability is a serious issue. Excess phase shift caused by multiple poles around the loop would likely cause the transimpedance amplifier to oscillate. For this reason, the basic amplifier for the transimpedance amplifier should have few stages, so that stability can be assured. The amplifier with few stages can only have limited voltage gain (A). Consequently, the feedback resistor, R_F, can only be made so large that bandwidth B can be satisfied.

5.3.2 622 Mbit/s Fiber Optic Preamplifier Design

A 622 Mbit/s fiber optic preamplifier is designed [41] by using the HP 0.5 um triple metal CMOS process. The transimpedance amplifier approach is adopted for this design. To properly transmit a 622 Mbit/s NRZ (Not Return to Zero) signal, the bandwidth required has to be equal to or larger than seven-tenth's of the bit rate, that is $B=0.7\times622$ MHz = 435 MHz. To minimize R_F noise with achievable gain of the basic amplifier in mind, the design goal for the transimpedance gain is set at 4 KΩ. This fiber optic preamplifier includes a transimpedance amplifier, a gain boost stage, output stage and an AGC circuit. The photo diode at the input of the transimpedance amplifier is assumed to have 0.6 pF junction capacitance. Magnitude of input current from photo

diode to the transimpedance amplifier could vary from 1.0 uA to 1 mA - a 60 dB dynamic range. The AGC (Automatic Gain Control) circuit is designed to handle this dynamic range.

5.3.2.1 Brief Circuit Description (Circuit Topology)

In the block diagram (Fig. 5.7), the core of the fiber optic preamplifier is a transimpedance amplifier. The transimpedance amplifier consists of an inverting amplifier and a common gate amplifier. The transimpedance amplifier is followed by the gain boost stage and the output stage. An AGC circuit is used to prevent overloading the transimpedance amplifier.

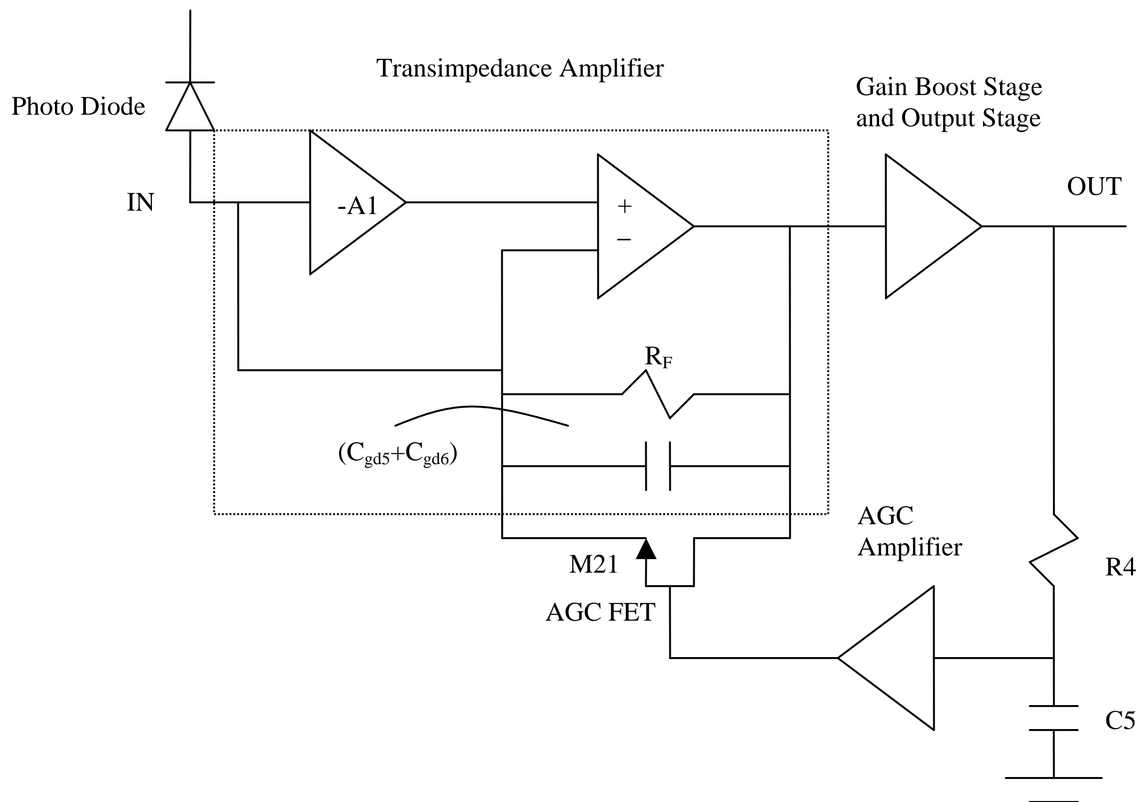


Fig. 5.7 Block diagram of the fiber optic preamplifier.

The circuit topology in Fig. 5.8 similar to the published GaAs transimpedance amplifier approach [33] has been adopted for our design.

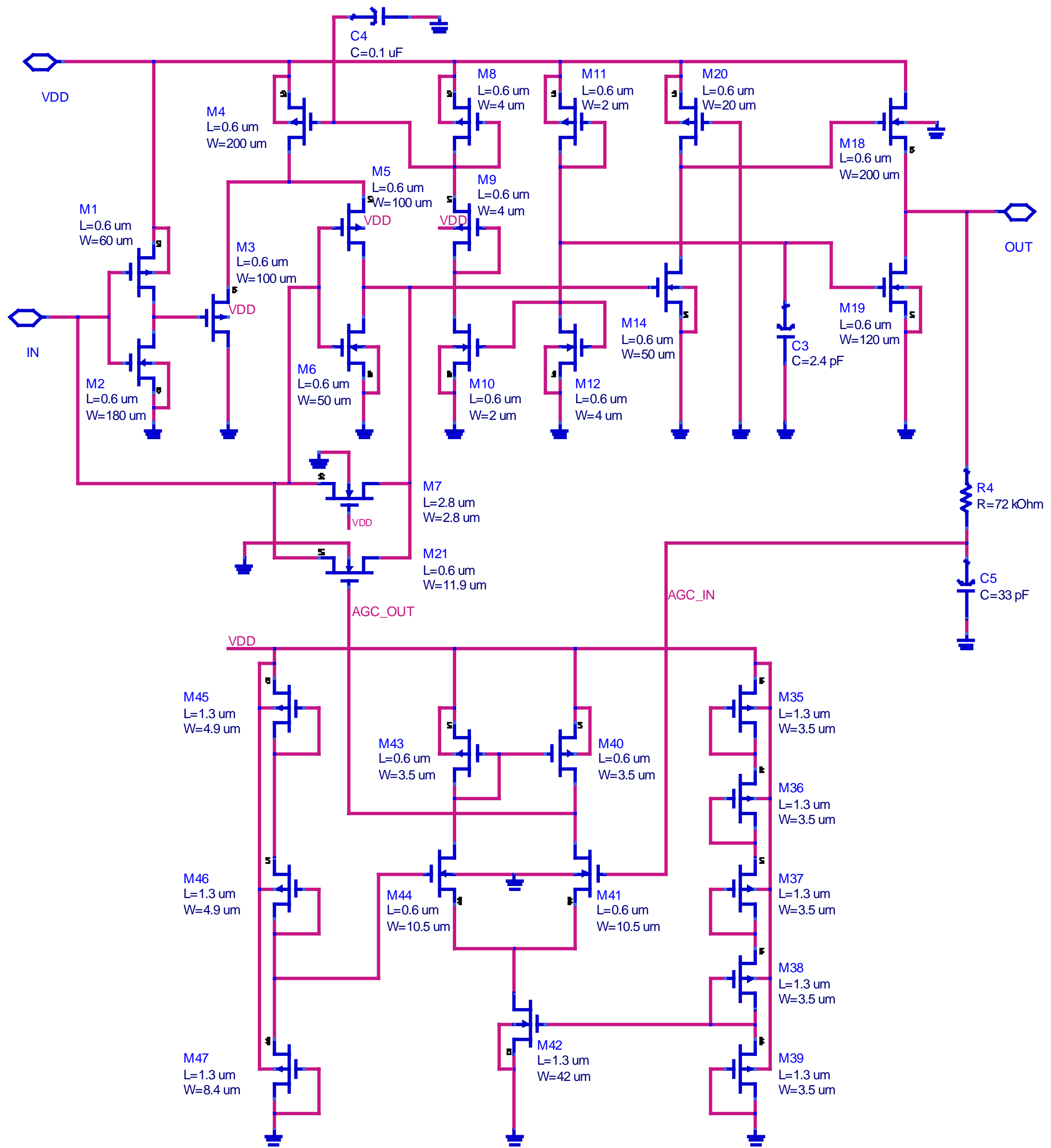


Fig. 5.8 The complete circuit of the fiber optic preamplifier.

The top part of the schematic is the RF signal path and DC bias circuit. The bottom part is the low frequency AGC circuit. This RF signal path consists of a transimpedance amplifier (shunt-shunt feedback amplifier), a gain boosting amplifier and an output driver. There are two forward RF signal paths from input to output inside the feedback amplifier - main signal path and secondary signal path. In the main signal path there are two amplifier stages. RF input is amplified by a CMOS inverting amplifier, M1 and M2, and further amplified by a source follower-common gate amplifier M3, M5, M6. The total voltage gain of this path is $A=A_1 \cdot A_2$. It is interesting to note that M3, M5, M6 can be viewed in another way as a single input-single output differential amplifier. The secondary RF path is a signal directly fed to the input of inverting amplifier M5, M6 and amplified with voltage gain A_3. This will be discussed again later.

The feedback resistor of the feedback amplifier is realized by M7. M13, M14, M20 form an additional gain stage in order to further boost the signal level. M18, M19 form an output stage to drive a 50-ohm load impedance. The AGC circuit, M35 to M47, will be discussed later.

5.3.2.2 Detailed Circuit Description and Circuit Simulation

The schematic of the 622 Mbit/s fiber optic preamplifier RF signal path is depicted in Fig. 5.9 for the purpose of discussion. AGC feedback is not included here.

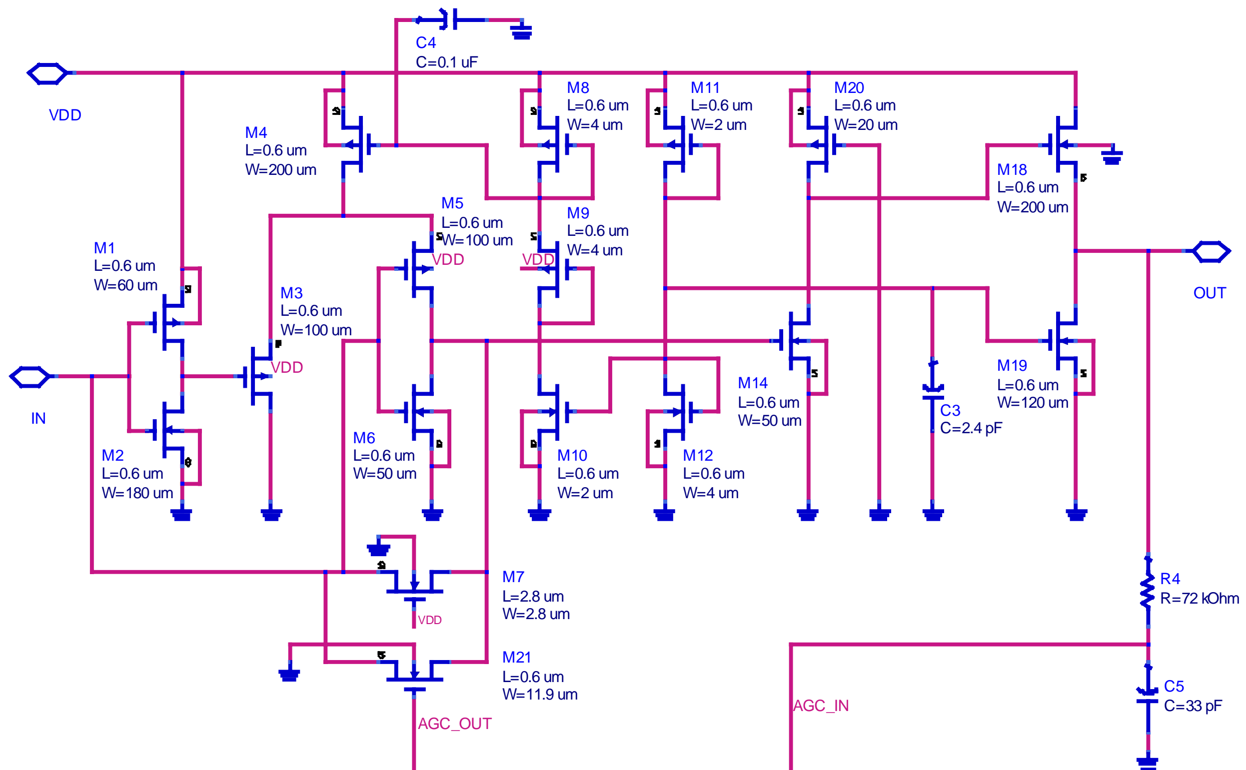


Fig. 5.9 The fiber optic preamplifier RF signal path.

This amplifier includes a two-stage transimpedance amplifier followed by an additional gain stage and an output stage. The simple DC bias circuit (M8~M12) provides bias for current source M4, M19 for the transimpedance amplifier and output stage. The transimpedance amplifier (M1~M7, M21) is self biased through feedback resistor M7 (M21 is off before AGC kicks in.) All RF path devices (except M7, M21, M20) of the optic preamplifier are biased in the saturation region. The output DC is biased at 2 volts. As mentioned earlier, in order to obtain the required bandwidth for minimum noise, a two-stage transimpedance amplifier is designed for getting enough gain to accommodate the bandwidth.

1) Transimpedance amplifier design

The transimpedance amplifier is a shunt-shunt feedback amplifier. There are two forward RF signal paths from input to output of the basic amplifier inside the feedback amplifier - main signal path and secondary signal path. The main forward path plays a major role for the frequency response and noise performance for the feedback amplifier. The secondary forward path is introduced by the connection of gate of M5, M6 to the input of the feedback amplifier for M5, M6 DC biasing. Its contribution to the gain of the basic amplifier is small compared to the main forward path. Gates of M5 and M6 are grounded when we do the first order analysis to the main forward path in Fig. 5.10.

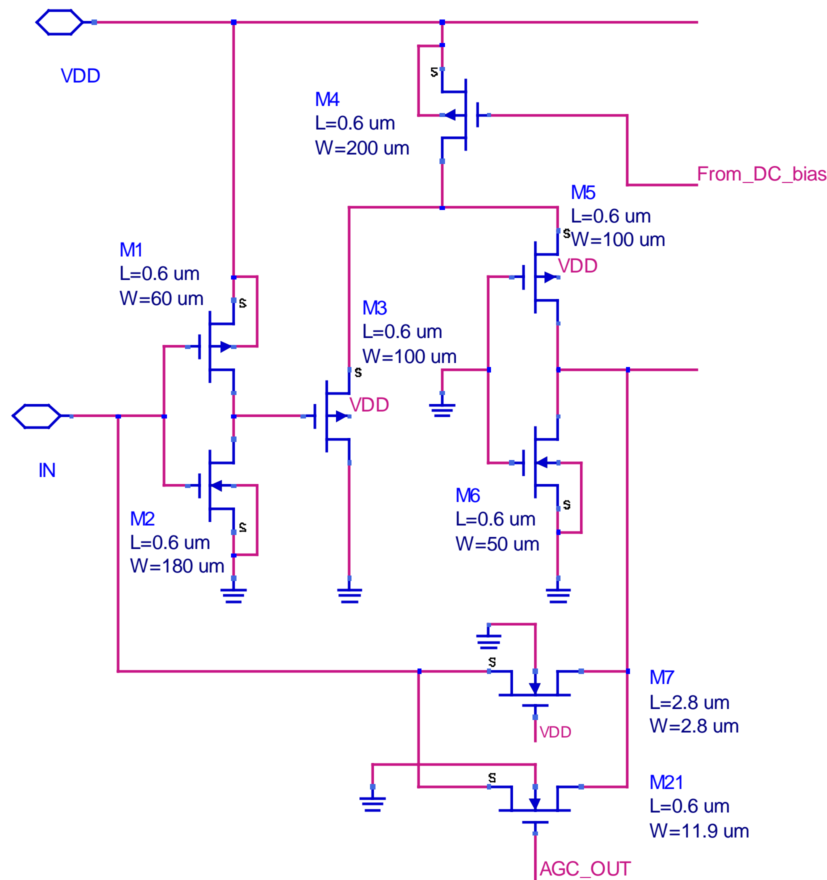


Fig. 5.10 Main forward path.

Main forward path:

As mentioned in 5.3.1, for given bandwidth, minimizing R_F noise (therefore increasing the basic amplifier A) conflicts with the stability of a transimpedance amplifier. The basic amplifier with fewer stages is preferred for stability reason. In order to form negative feedback, the basic amplifier usually consists of odd number of inverting gain stages. A transimpedance amplifier with one inverting gain stage within the feedback loop is most stable, but the gain is too low to support the bandwidth. Three inverting gain stages can provide very large gain, but it would make oscillation of the transimpedance amplifier likely. Therefore a one inverting but two gain stage amplifier, in the main forward path, is chosen for getting enough gain to accommodate the bandwidth. The first stage amplifier is the most important stage. The noise generated from the first stage usually dominates the noise generated by the following stages. The following stages of the amplifier have a negligible contribution to the overall noise performance. The noise generated from the first stage depends on physical size of the first stage FETs. To minimize FET noise contribution to the transimpedance amplifier the FET size of the first stage is chosen so that

$$C_{gs_1} + C_{gs_2} + C_{gd_1} + C_{gd_2} = C_d \tag{5.7}$$

Under this condition, an early study ([34], [37]) shows that M1, M2 noise contribution to the amplifier is minimum. So using equation (5.7) as a guideline the active devices M1, M2 of the first inverting amplifier is chosen for noise minimization. The second amplifier stage is a wide-band source follower-common gate amplifier. The dominant pole of this transimpedance amplifier is determined by the equivalent parallel

R_i-C_i circuit seen at the input by the current source i_d. Unlike the simplified transimpedance amplifier block diagram in Fig. 5.6, the basic amplifier within the feedback loop has two stages rather than one. Therefore bandwidth B, equation (5.6), for this particular amplifier is derived.

$$B = \frac{A}{2\pi R_F (C_{gs_1} + C_{gs_2} + C_d + A_1 (C_{gd_1} + C_{gd_2}) + A(C_{gd_5} + C_{gd_6}))} \quad (5.8)$$

$A = A_1 \times A_2$, where A_1 is low frequency gain of the first inverting amplifier stage, A_2 is low frequency gain of the source follower-common gate amplifier stage. The feedback resistor is realized by a small FET, M7, so the parasitic capacitance C_F associated with M7 is negligible.

$$A_1 = \frac{g_{m_1} + g_{m_2}}{g_{ds_1} + g_{ds_2}} \quad (5.9)$$

$$A_2 = \frac{g_{m_3} g_{m_5} r_{ds_5} r_{ds_6}}{g_{m_3}(r_{ds_5} + r_{ds_6}) + g_{m_5} r_{ds_5}} \quad (5.10)$$

Secondary forward path:

The secondary AC equivalent circuit is drawn in Fig. 5.11 assuming the main forward path is AC shorted.

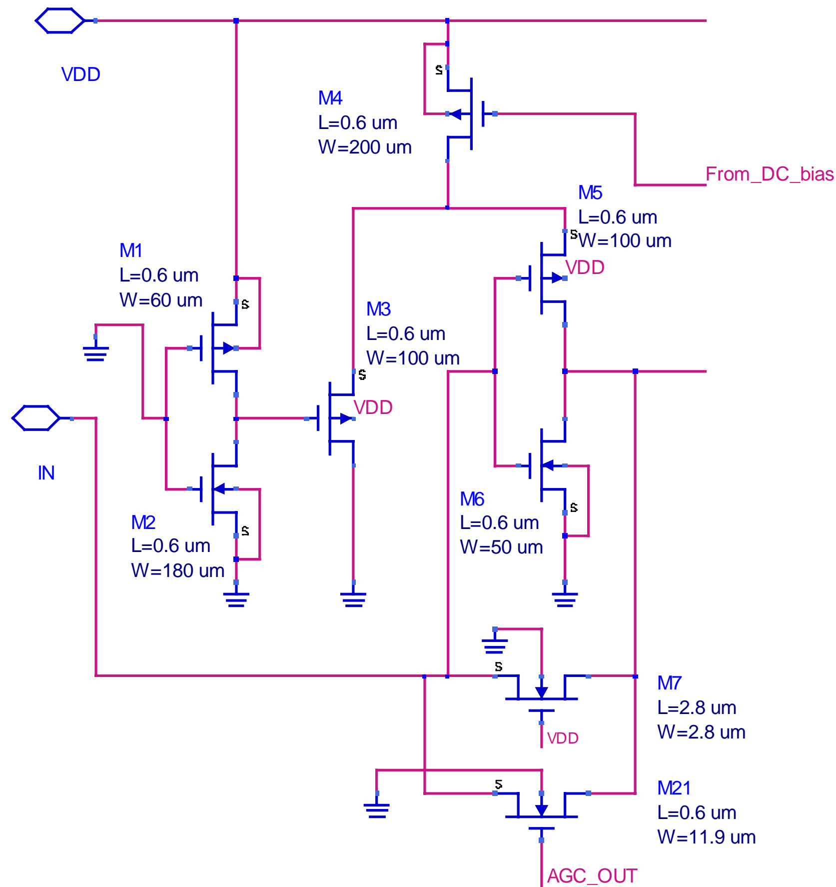


Fig. 5.11 Secondary forward path.

This signal path has one inverting amplifier M5, M6 with gain of A_3.

$$A_3 = \frac{g_{m_5} + g_{m_6}}{g_{ds_5} + g_{ds_6}} \tag{5.11}$$

We will see A_3 is much less than A. As mentioned before, while the secondary forward path is introduced by DC biasing connection for the M5, M6 common gate amplifier, the FET gate-drain capacitors C_{gd_5}, C_{gd_6} are in parallel with the feedback resistor M7 (R_F). This generates a zero at $1/(R_F(C_{gd_5} + C_{gd_6}))$ in the feedback path (Fig. 5.12), enhancing the feedback amplifier stability.

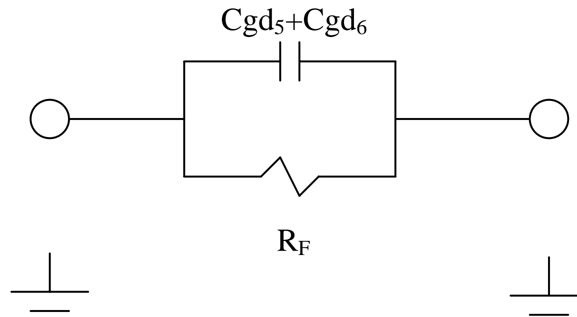


Fig. 5.12 Feedback path.

The first order analysis:

The circuit design has been carried out by PSPICE simulation. Given the bias condition $I_{ds_1} = I_{ds_2} = 13$ mA, $I_{ds_3} = 4.5$ mA, $I_{ds_5} = I_{ds_6} = 3.5$ mA, then the small signal parameters of the devices, from device measurement, are:

$g_{m_1} = 5.76 \times 10^{-3}$, $g_{m_2} = 2.5 \times 10^{-2}$, $g_{ds_1} = 7.33 \times 10^{-4}$, $g_{ds_2} = 6.74 \times 10^{-4}$

$g_{m_5} = 6.74 \times 10^{-3}$, $g_{m_6} = 6.88 \times 10^{-3}$, $g_{ds_5} = 4.64 \times 10^{-4}$, $g_{ds_6} = 1.74 \times 10^{-4}$

$g_{m_3} = 7.74 \times 10^{-3}$ $g_{ds_3} = 3.96 \times 10^{-4}$

This results in A_1=22, A_2=8.5, A=22×8.5=187. A_3 = 21.3. Including the R_F (4 KΩ) loading effect on the output of the source follower-common gate amplifier (M3, M5, M6) and on the output of the inverting amplifier (M5, M6) respectively, A_2 is reduced to A_2=6.4, A is reduced to A=140.8, and A_3 is reduced to A_3 =16.3. Further, including degeneration effect of M3 at the source of M5 will yield an even smaller value of A_3.

Since A_3<16.3<<A=140.8, the validity of Fig. 5.10 to estimate gain A and bandwidth B is assured. The capacitance parameters of the devices are:

C_{gs_1} =0.08 pF, C_{gs_2} =0.3 pF, C_{gd_1} =0.02 pF, C_{gd_2} =0.09 pF

C_{gs_5} =0.13 pF, C_{gs_6} =0.083 pF, C_{gd_5} =0.03 pF, C_{gd_6} =0.025 pF

For R_F=4 KΩ, C_d=0.6 pF, and substituting the above values into the equation (5.8) gives

$$B = \frac{140.8}{2\pi \cdot 4 \times 10^3 (0.08 + 0.3 + 0.6 + 22(0.02 + 0.09) + 140.8(0.03 + 0.025)) \cdot 10^{-12}}$$

$$= 503 \text{ MHz}$$

2) Additional gain stage and output stage

Gain stage:

M13, M14, M20 form an additional gain stage with low frequency voltage gain

$$A_4 = \frac{g_{m_{14}}}{g_{ds_{13}} + g_{ds_{14}} + g_{ds_{20}}} \tag{5.12}$$

where $g_{m_{14}} = 7.16 \times 10^{-3}$, $g_{ds_{13}} = 9.86 \times 10^{-6}$, $g_{ds_{14}} = 4.14 \times 10^{-4}$,

$g_{ds_{20}} = 2.25 \times 10^{-3}$.

This results in A_4 =2.7.

Output stage:

A wide band source follower M18, M19 forms the output stage. The output impedance of this stage is $1/g_{m_{18}}$ =34 Ω and this drives an external 50 Ω load-impedance. The low-pass filter $(r_{ds_{11}} \| r_{ds_{12}})C_3$ at the gate of M19 filters out noise above 2.7 MHz. The simulation result of the complete circuit analysis is shown in Fig. 13. Total transimpedance gain of the optical preamplifier is 5.5 KΩ. The 3 dB bandwidth is 518 MHz. The total transimpedance gain is reduced by the fact that body effect in M18 lowered it's transconductance.

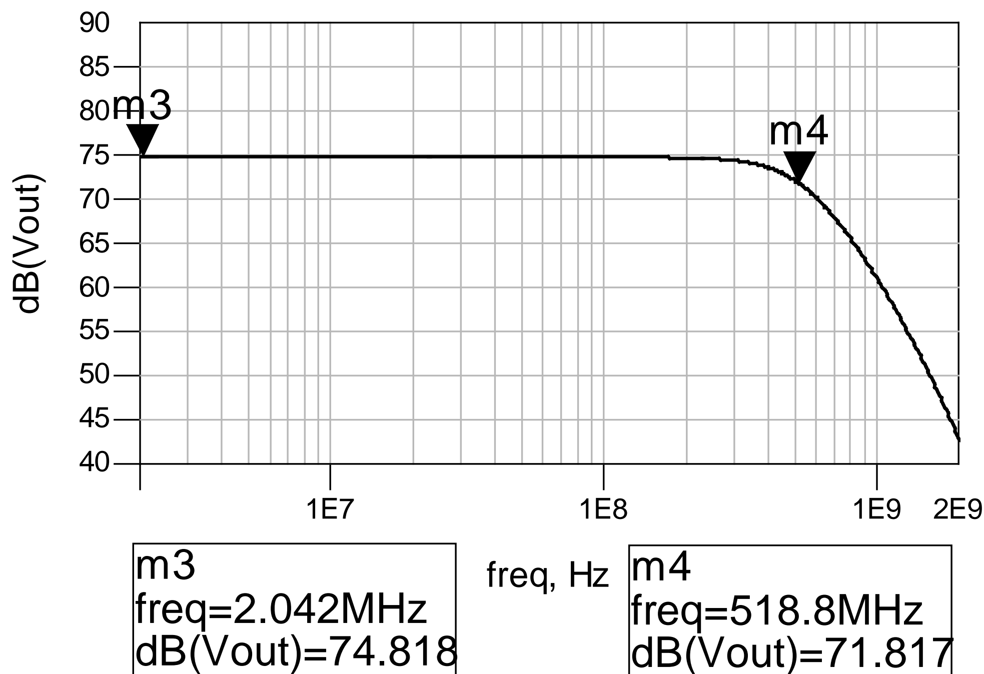


Fig. 5.13 Frequency response.

3) AGC loop

An AGC circuit (Fig. 5.14) is designed for the fiber optic preamplifier to accommodate a large variation of the photo current input. When more light falls on the photo diode it produces more photo current in the diode. The photo diode sinks more current from the optical preamplifier causing the average voltage level of the output of the amplifier to drop. Eventually a large enough photo diode current will cause the output voltage to saturate.

Fig. 5.14 AGC circuit.

To prevent this overloading of the amplifier, the DC voltage component of the optical preamplifier's output is sampled by a RC low pass filter, R_4, C_5 to provide AGC

control. Since the optical pulses coming into the optical preamplifier are allowed to have long runs, as long as 30 consecutive “0’s” or “1’s”, the time constant of the low pass filter has to be long enough to hold the correct DC voltage level despite of the existence of these long runs. For a 622 Mbit/s NRZ optical signal the fundamental frequency is 311 MHz. A long run of 30 “0’s” or “1’s” at such a data rate would last about 0.1 microseconds. Therefore a time constant for the low pass filter $R_4C_5 = 1.4us$ is selected. The sampled DC component is fed to the differential input, single output OP amp and compared with a reference voltage. The output of this OP amp controls the gate of variable drain-source resistor M21. When the DC voltage to the input of the OP amp is lower than the reference voltage, the output voltage of the OP amp rises (Fig. 5.15). This would turn on M21. The M21 drain-source resistor shunts the M7 drain source resistor,

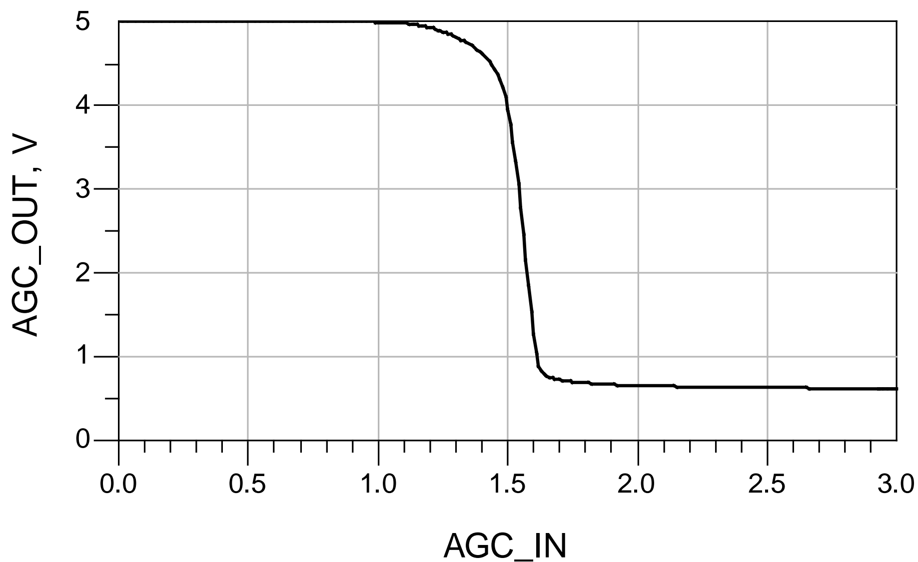


Fig. 5.15 Input-output transfer characteristic of AGC circuit.

R_F, resulting in reduced total transimpedance gain. The reference voltage to the OP amp is set so that the output voltage of the optical preamplifier will not exceed 0.6 volts peak to peak.

5.4 Layout and Packaging

1) Layout

The 622 Mbit/s optical preamplifier circuit chip is carefully laid out to reduce parasitics (Fig. 5.16).

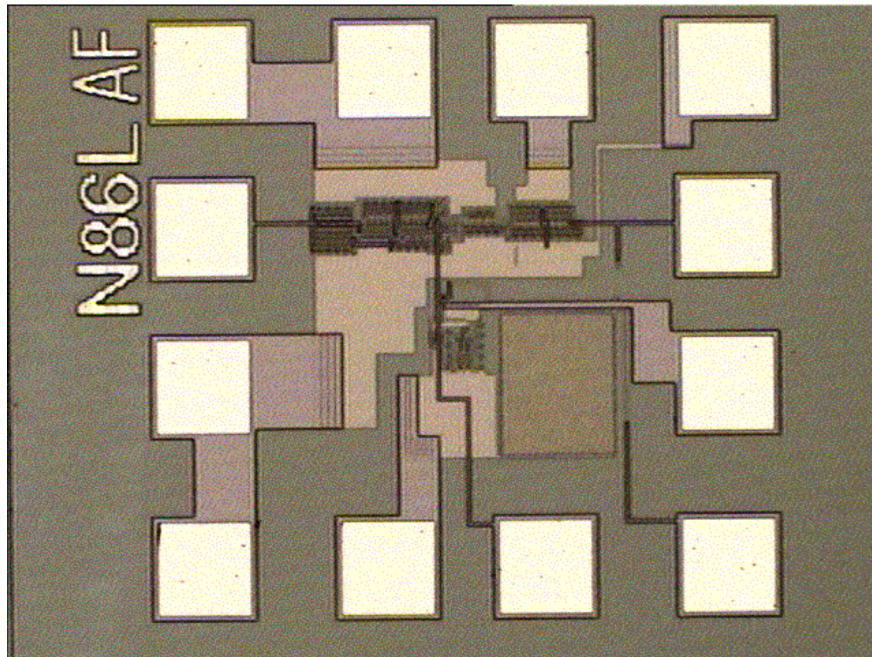


Fig. 5.16 Chip photograph of the 622 Mbit/s optical preamplifier circuit.

Special attention is made to reduce source resistance by making multiple via contacts between metal layers and metal layers to the substrate. A poly capacitor and N-well resistor is used to form the AGC low-pass filter. Input bonding pad (0,2) connects to

a photo diode. Output bonding pad (3,2) connects to an output load. The DC voltage-supply bonding pads are split to VDD1, VDD2, VDD3 (0,3~2,3 and 3,1) to avoid cross talk and feedback oscillation due to finite bonding wire inductance. VDD1 supplies the transimpedance amplifier and additional gain stage. VDD2 supplies the output stage and VDD3 the AGC stage. Ground bonding pads (bottom left corner and 3,3) have also been split to two separate groups for the same reason. Multiple bonding pads are laid out for the VDD1 and GND1 lines to reduce bonding wire inductance. A bonding pad, CAP (2,3), connects a 0.1 uF external capacitor from the gate of DC current source M4 to ground to filter out noise. An AGC bonding pad (1,4) is used to monitor the AGC DC voltage.

2) Packaging

A 10 lead flat package is used to assemble the 622 Mbit/s optical preamplifier testing circuit (Fig. 5.17). Two RC series de-Qing circuits are placed on the VDD1 and VDD2 lines and one 220 pF chip capacitor is placed on the VDD3 line to isolate and absorb undesired high frequency signal feedback due to bonding wire inductance. Circuit simulation shows that these VDD bypassing circuits are very effective in reducing high frequency signal feedback through DC supply line. The wire from pad, CAP, is bonded to package lead 5 which is used to connect a 0.1 uF external bypassing capacitor on the PCB board (not shown). The wire from pad AGC is bonded to lead 7. The output is wired to lead 8. The input is wire bonded in two different ways depending on whether an electrical testing setup or an optical testing setup is used. In an electrical testing setup,

using RF 50 Ω testing equipment, a photo diode equivalent circuit is placed in front of the preamplifier chip (Fig. 5.17) to mimic the usual photo diode source.

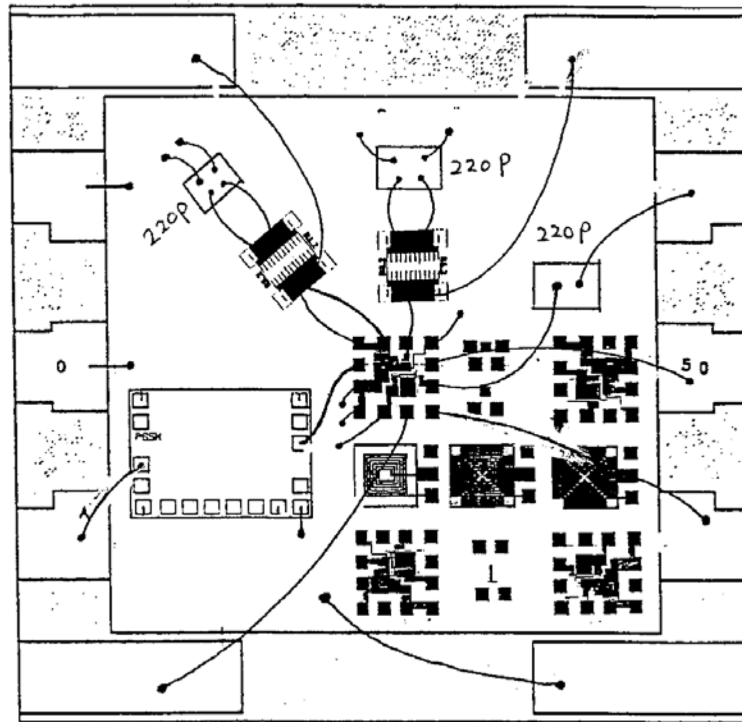


Fig. 5.17 Diagram of the packaged 622 Mbit/s optical preamplifier testing circuit.

The electrical input signal is connected to the package lead 4 where it is connected to the input of the photo diode equivalent circuit. The output of photo diode equivalent circuit is then wire bond to the input pad (Fig. 5.16 above). In the optical testing setup, a photo diode on the PCB board is connected to package lead 4. Then lead 4 is directly connected to the input pad. More noise bypassing capacitors and ESD protection diodes are placed on the PCB board around the packaged chip to further filter low frequency noise from the DC voltage supply line and to provide ESD protection for some critical leads such as the AGC monitoring lead number 7.

5.5 Measurement Result

Both electrical and optical measurements have been performed for the 622 Mbit/s optical preamplifier circuit packaged devices. The device drew 33 mA from a 5 V power supply. The electrical measurement results in a 644 MHz 3 dB bandwidth and a 7.6 KΩ transimpedance gain. A 2.42 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ input equivalent noise current density, up to 500 MHz, has been achieved. The optical measurement shows a –29 dBm optical sensitivity at a 10^{-9} bit error rate.

1) Electrical measurement

The diagram of the packaged device for electrical testing is shown in Fig. 5.18. A photo diode equivalent circuit chip is wire bonded in front of the preamplifier chip inside the package.

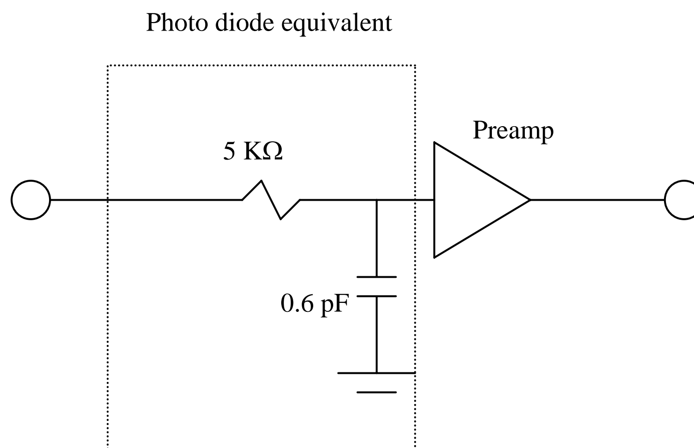


Fig. 5.18 A photo diode equivalent circuit chip connected to input of the preamplifier.

As discussed earlier, a photo diode can be electrically modeled as a current source i_d with shunt capacitor C_d [37]. In order for the amplifier to see a high impedance current source, a 5 KΩ resistor, r_d is inserted between the 50 Ohm RF source and the amplifier input. Now the source seen by the amplifier is a 5 KΩ high impedance in parallel with the diode capacitor C_d. So the amplifier sees a current source driving its input, because in contrast to the 5 KΩ source resistance the input resistance of the amplifier is about 30 Ω. An HP 8753C Vector Network Analyzer is used to perform the test (Fig. 5.19).

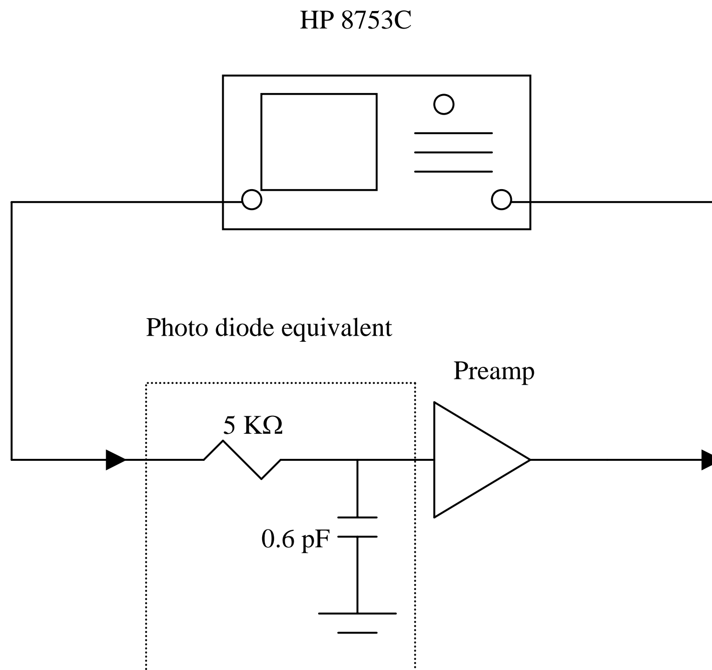


Fig. 5.19 Electrical testing set up for 622 Mbit/s optical preamplifier.

The amplifier is biased by a 5 V DC power supply and draws 33 mA current. The measurement result is presented as the S parameter forward gain, S_{21}, in Fig. 5.20. It

shows the amplifier has a 9.7 dB S_{21} gain and 644 MHz bandwidth. The relationship between S_{21} and R_{total} can be approximately expressed as

$$S_{21} = 2 \cdot \frac{R_{Total}}{r_d} \tag{5.13}$$

R_{total} is total transimpedance of the preamplifier, including gain boost stage and output loaded with 50 Ω. If S_{21} is measured in dB, then equation (5.13) becomes

$$10^{\frac{S_{21}}{20}} = 2 \cdot \frac{R_{Total}}{r_d} \tag{5.14}$$

Therefore total transimpedance of the amplifier, R_{total} , =7.6 KΩ. These measured results are higher than the calculated total impedance (5.5 KΩ) and bandwidth (518 MHz) which can be attributed to a combination of model inaccuracy and process spread.

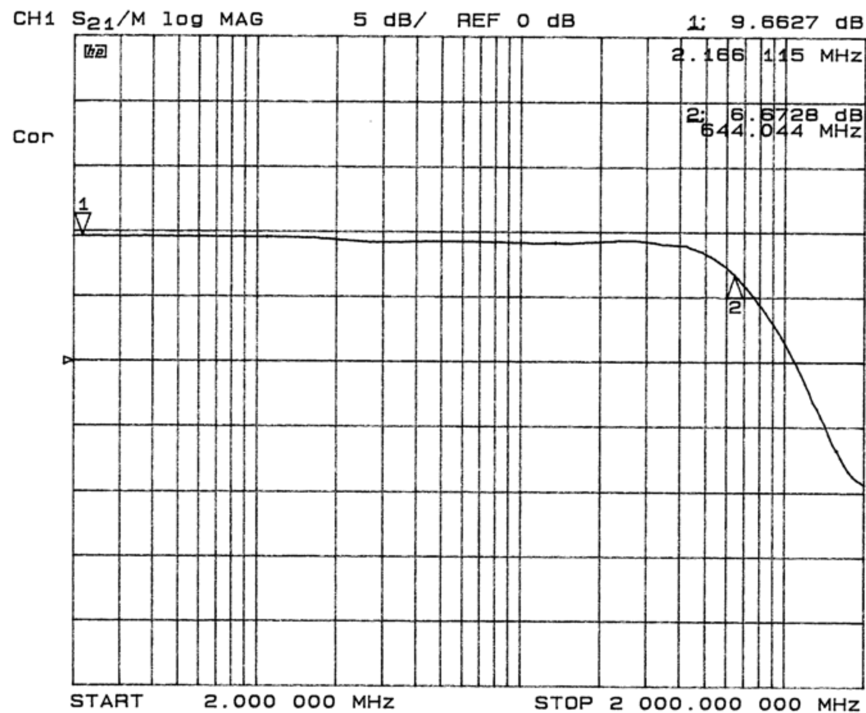


Fig. 5.20 Frequency response of 622 Mbit/s optical preamplifier.

The output noise of the amplifier is measured by an HP Spectrum Analyzer. Since we only want the noise produced by the amplifier to be measured, only C_d is connected to the input of the amplifier to mimic the photo diode loading effect (Fig. 5.21). A wide band low noise amplifier with 46 dB gain is placed after the optic preamplifier to raise the noise level for an adequate measurement, but then this level is reduced by a 23 dB attenuator to avoid overloading the spectrum analyzer.

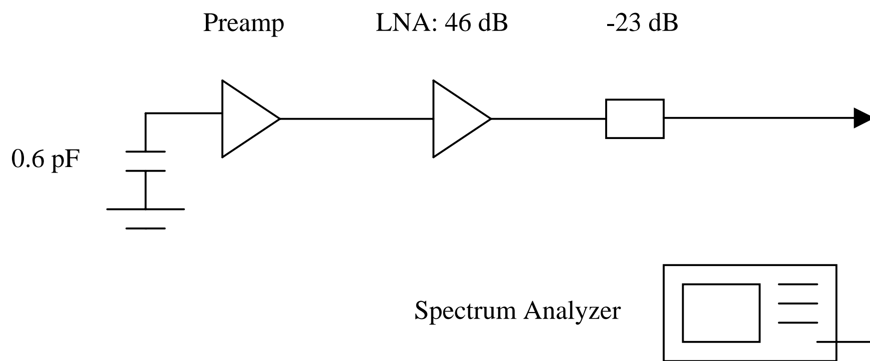


Fig. 5.21 Measure output noise of the preamplifier.

From the measured data (Fig. 5.22) the square root of equivalent input noise current density can be calculated, $i_n = 2.42_pA/\sqrt{Hz}$. According to our best knowledge this represents the best noise performance for a 0.5 um CMOS transimpedance amplifier.

2) Optical measurement

A diagram of the optical testing setup for a packaged optic preamplifier is shown in Fig. 5.23. The optic preamplifier is connected with a photo diode only at input.

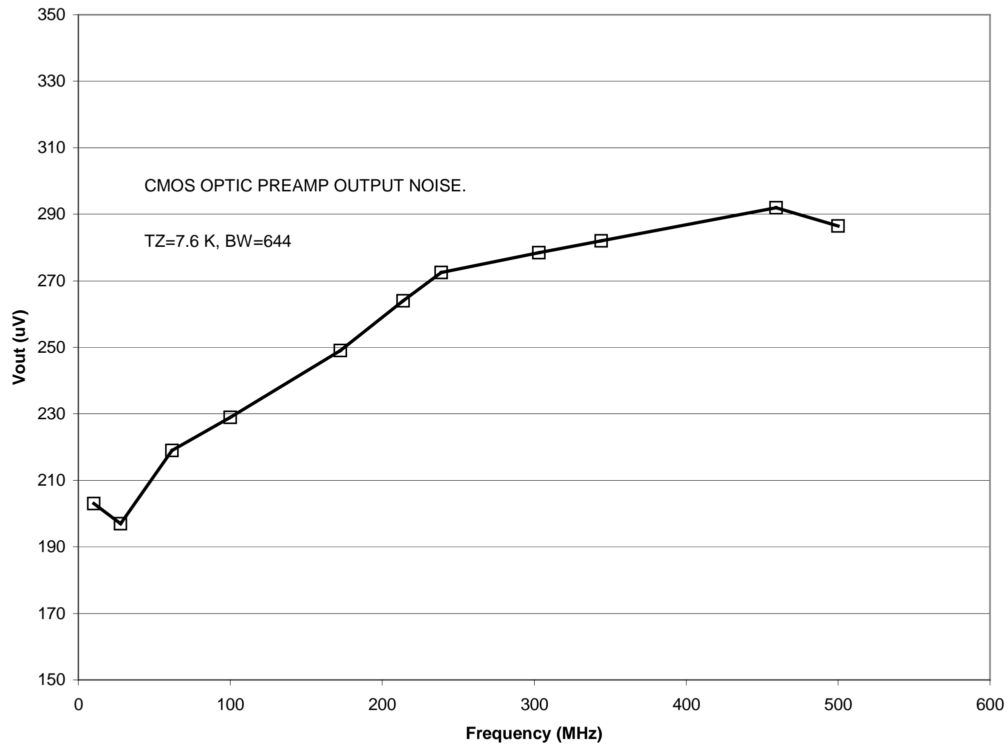


Fig. 5.22 Output noise of the preamplifier (RBW=1 MHz).

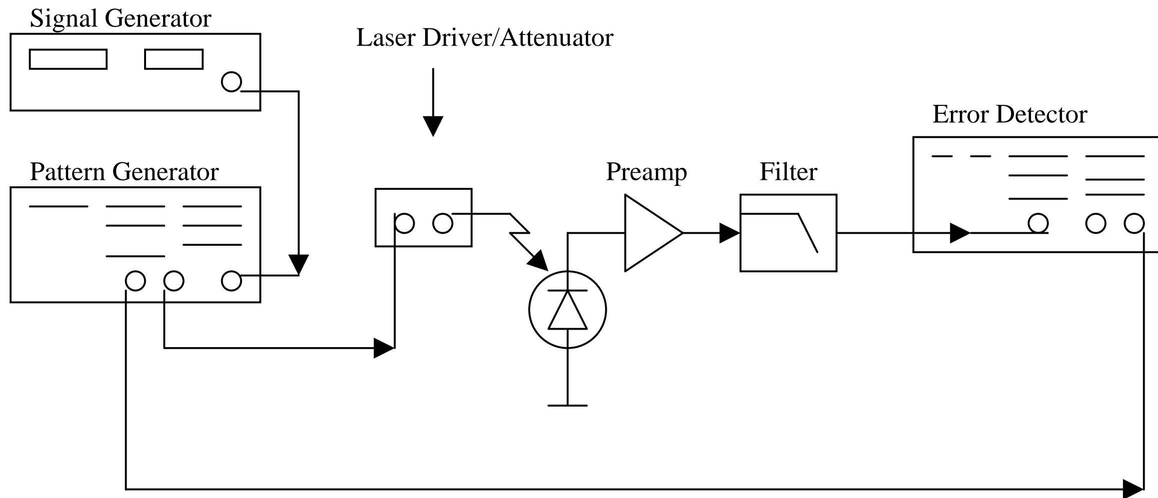


Fig. 5.23 Optical testing setup for the optic preamplifier.

A 1310 nm Siemens InGaAs/InP PIN photo diode, SRD 00214, is used as the input source for the optic preamplifier and a 622 Mbit/s 2^{23}-1 pseudo random bit sequence (PRBS) signal is chosen to drive the laser source. The amplifier sensitivity is measured at a 10^{-9} bit error rate. A 400 MHz Bessel low-pass filter is placed after output of the amplifier to eliminate out of band noise. Measurements indicated a –29 dBm optical sensitivity and a -3 dBm overload power. Eye diagrams at those conditions are shown in Fig. 5.24 (a) and 5.24 (b).

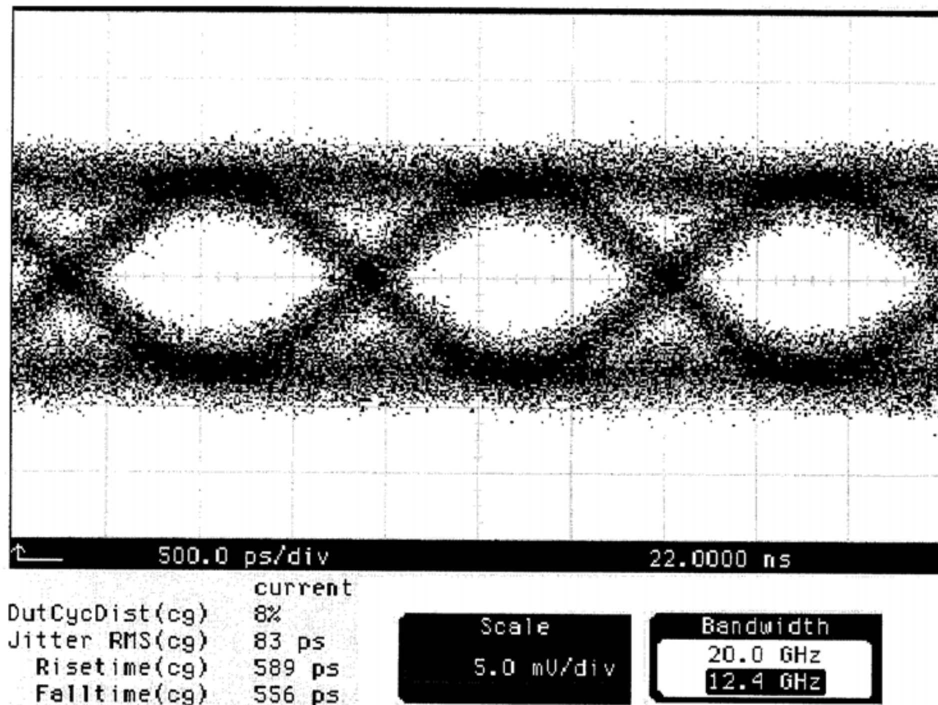


Fig. 5.24 (a) Preamplifier sensitivity eye diagram.

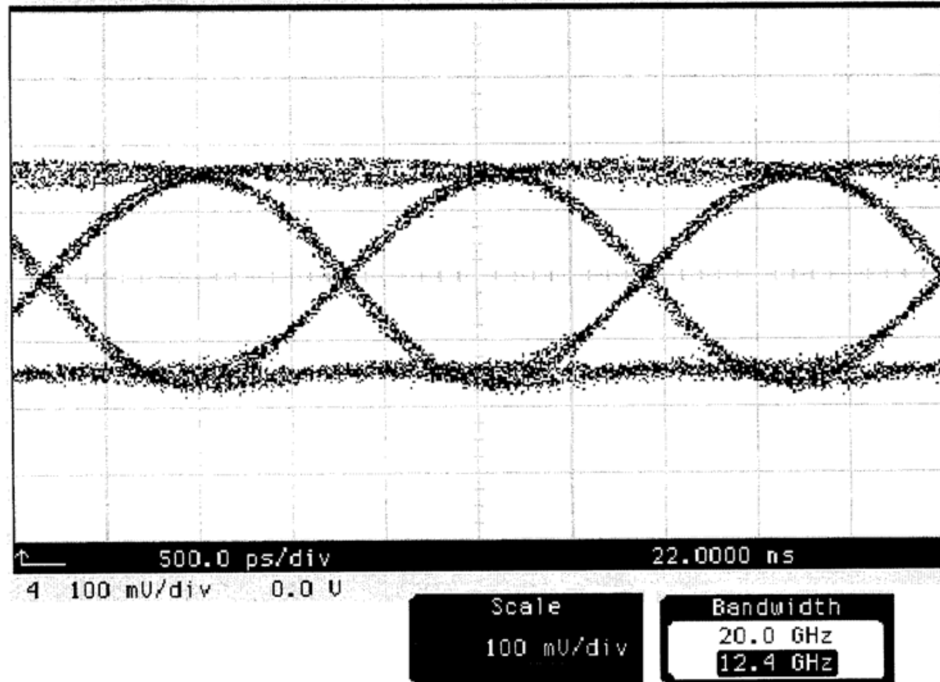


Fig. 5.24 (b) Preamplifier overload eye diagram.

5.6 The preamplifier in a 0.35 um CMOS process.

The preamplifier topology above is simulated in a 0.35 um CMOS process. The intention is to explore the circuit performance improvement with this process. The photo diode capacitor at the input and the feedback resistor are kept 0.6 pF and 4 KΩ as before. It is seen from simulation that the f_T of a 0.35 um CMOS FET is doubled compared to the 0.5 um process. This is attributed to the increased transconductance g_m and a reduced parasitic capacitance by about 0.7. The size of devices of the original amplifier is re-optimized for 0.35 um process operation (Fig. 5.25). An extra local feedback is added to the first stage to reduce high frequency peaking. A 3.3 V supply is used for the new preamplifier to reduce the power consumption. Simulation (Fig. 5.26) shows that the

Fig. 5.25 Tansimpedance amplifier with 0.35 um CMOS process.

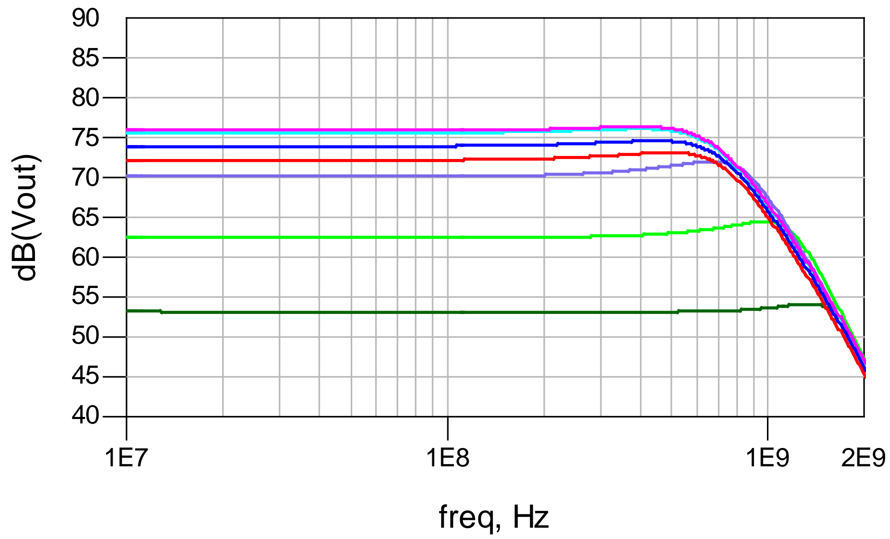


Fig. 5.26 Frequency response for 0.35 um process transimpedance amplifier.

preamplifier bandwidth with 0.35 um process is increased to 800 MHz compared to 518 MHz with 0.5 um process circuit. The total DC current is decreased to 17 mA with the 0.35 um process compared to 33 mA with a 0.5 um process.

Chapter 6 Conclusions

6.1 Summary

A 0.5 um CMOS FET has been studied in comparison with the GaAs FET. The characterization results show that an NMOS FET has similar RF characteristics in terms of g_m, f_T. However, the thermal noise for an NMOS FET is 1 dB higher than for the GaAs FET.

Inductor Q on a silicon substrate has been studied. Inductor Q depends on both metal strip thickness and substrate resistivity. The inductor Q is limited by the metal strip DC resistance at low frequencies. At higher frequencies, substrate resistivity affects the inductor Q. The test result shows that both increasing the metal thickness and increasing the substrate resistivity can improve the inductor Q. But the substrate effect on the inductor Q improvement is more prominent for the thicker metal inductor. Therefore a higher resistivity substrate could be used more effectively to improve the thicker metal inductor Q.

A 622 Mbit/s CMOS optic preamplifier has been designed in a 0.5 um process. The design features a two-stage amplifier made up of a common source stage followed by a common gate stage. Parasitic capacitance has been used for Miller compensation to assure circuit stability. This circuit shows very low noise compared to the published results on other transimpedance amplifiers using similar gate length CMOS processes. Further study should be focused on reducing the circuit power while maintaining the circuit performance. The same circuit topology of the optic preamplifier has been simulated with 0.35 um CMOS process. The simulation shows that channel length scaling

from 0.5 um to 0.35 um increases the preamplifier bandwidth from 518 MHz to 800 MHz and cuts power consumption by two thirds.

6.2 Future Work

The transimpedance amplifier we have presented could be further optimized by incorporating some design changes. First the PMOS differential pair in Fig. 5.8 could be replaced with a NMOS differential pair along with its bias circuitry. Also the M1, M2 width ratio could be adjusted to allow the bias voltage of the feedback amplifier to be closer to VDD. This arrangement would move the bias voltage of the feedback amplifier to a higher value and thus provide more options for the photo diode biasing. More importantly, it would be interesting to see if there is an advantage in term of bandwidth of the new transimpedance amplifier compared to the one we have already presented. The input capacitance of the gain boost stage at the output of the feedback amplifier causes extra phase shift. A buffer stage could be inserted before the gain boost stage at the cost of more current and some gain loss. As an alternative to adding a buffer stage, a wide band common gate amplifier can be designed for the gain boost stage.

A new heterojunction BiCMOS technology, silicon germanium BiCMOS (SiGe BiCMOS), has emerged in the last ten years [42]. It combines the high operating frequency heterojunction BJT (HBT) and CMOS FETs into a single process. It has proven to be a viable process for RF integrated circuits. Within the SiGe BiCMOS process, the SiGe NPN HBT has a much higher f_T than the NMOS FET. Its noise figure is about the same as a comparable MESFET, and much lower than an NMOS FET. By adding SiGe HBTs to the digital CMOS process, the analog, RF and digital

functionalities can be realized on one chip. Some research has already been published on SiGe BiCMOS transimpedance amplifiers [43], [44]. A 7.4 GHz and 10 GHz SiGe BiCMOS transimpedance amplifier was reported. Above 1 GHz, a SiGe BiCMOS transimpedance amplifier design usually adopts a single stage amplifier approach. The two stage amplifier approach reported in this study could be explored. Needless to say, other low noise wideband circuit design approaches should also be explored. Since SiGe NPN HBT's have higher g_m than NMOS FET's under the same bias condition, a SiGe BiCMOS transimpedance amplifier is expected to consume less power than a CMOS transimpedance amplifier. Better noise performance is also expected.

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