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BASIC ISSUES IN SYNCHRONOUS DIGITAL HIERARCHY NETWORKS

by

JUN TENG

A dissertation submitted to the Graduate Faculty in Engineering in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York

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ABSTRACT

BASIC ISSUES IN SYNCHRONOUS DIGITAL HIERARCHY NETWORKS

by

Jun Teng

Advisor: Professor M. S. Obaidat

Frame synchronization, multiplexing and error detection are three basic issues in Synchronous Digital Hierarchy (SDH) transmission networks. The relative techniques are required for meeting efficient and correct digital signal transmission in high speed digital communication networks. According to a group of ITU-T recommendations G.707, G.708 and G.709, this dissertation deals with research on the basic issues of frame synchronization, multiplexing and estimation of errored block detection for STM-1 system with a rate of 155.520 Mbits/s in SDH networks. In this framework, first, we present an entirely novel parallel processing-based frame synchronization system and analyze its performance. By using a parallel approach, we are able to process in SDH system at a rate of 19.44 MHZ. This means that all functions, such as descramble, section overhead monitoring, pointer processing, etc., are operated at byte rate after the framer. All of these functions must be done on a byte wide basis. Thus all operations are performed in parallel in an SDH processor. The scheme is expected to relax operating speed requirements and simplify complexity of the

circuits used in the system. The proposed methodology can be implemented using off-the-shelf low-rate integrated circuits (ICs) without sacrificing performance. In the second part of this dissertation, we present a method for multiplexing C-3 payload in the STM-1 structure. Our technique eliminates signal rate variations, which occur in various multiplexing structures in the SDH networks, by using a buffer. Calculations related to the buffer capacity for C-3 payload are also presented. In the third part of the dissertation, we study bit interleave parity(BIP) code performance, find a close form to solve the probability of undetected error, and give a group of curves for estimating errored block rate. This work is based on the features of BIP code.

Although our study is based on the STM-1 frame structure, the proposed methodologies are expected to be efficient solutions for implementing other STM-N systems.

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This dissertation is dedicated to my parents with respect and love, to my two sisters with sincere gratitude for bearing the responsibility of taking care of my parents during my Ph.D. study.

Also this dissertation is dedicated to my wife. With her great love and unselfish support I could continue my Ph.D. study.

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Chapter 1

INTRODUCTION

1.1 Motivation

Since the Plenary Assembly of the ITU-T[1] adopted the I series of recommendations dealing with the Integrated Services Digital Network (ISDN) matters in 1984, both demand for a flexible network and progress in technology and system design have led to the definition of the Asynchronous Transfer Mode(ATM) principle [1]. ATM is a wide-bandwidth, low delay, packet-like switching and multiplexing technique. Its concept is now accepted as the ultimate solution for the Broadband Integrated Service Digital Network (B-ISDN) by ITU-T in which benefits to users and network providers include: common user-network interface for accommodating various types of traffic including voice, video and real-time data, signaling capabilities, service

[1] ITU-T is the new name for the well-known International Consultative Committee for Telephone and Telegraph(CCITT) from 1993. Now it is a sector of the International Telecommunications Union(ITU), which is in charge of setting network standards for public telecommunication.

integration, and provision of new and improved services [2]-[5].

Proposed as the B-ISDN interface structure, Synchronous Digital Hierarchy (SDH) was adopted by ITU-T as a group of recommendations in 1993 [6]-[8]. It has the inherent flexibility to transport quite different types of signals like those through ISDN channels. ATM cells can also be carried in SDH frames as the SDH payload [3]. Since a basic frame of SDH is able to carry $261 \times 9 = 2349$ payload bytes, while each ATM cell contains 53 bytes, SDH provides some overhead bytes for pointing out the location of the first complete ATM cell in a SDH frame. All of the features in SDH construct a base for realizing information super-highway [9]. Such a user-network interface implementation would have the advantage of full compatibility with the network-node interface. This avoids the unnecessary conversion of signals that are sent from a user to others through the network. This property is extremely useful at the introductory phase of B-ISDN when a complete network infrastructure does not yet exist. Customers may easily be provided with access to a broadband network node(a cross-connect or a switch).

1.2 Development From PDH To SDH

Digital transmission networks in the public switched telephone network are designed in hierarchies of transmission rates, corresponding to increasing numbers of channels conveyed on a single multiplexed link. These hierarchies are defined in international

Table 1.1: Plesiochronous Digital Hierarchy(PDH, in kbits/s)

Level	US hierarchy	European hierarchy
1	1,544	2,048
2	6,312	8,448
3	44,736	34,368
4		139,264

standards. They have experienced evolution from plesiochronous hierarchies to synchronous ones.

The first hierarchies standardized were those for plesiochronous multiplexing [10]-[15]. Several distinct plesiochronous hierarchies simultaneously exist in different locations around the world. In Europe, the hierarchy is based on the 30-channel 2.048 Mbits/s primary rate, while in the USA and Japan, it is based on the 24-channel 1.544 Mbits/s primary rate. Some successive levels of multiplexing recommended by ITU-T are listed in Table 1.1.

PDH network gave its contribution to enhancing channel capacity, however, it has some limitations due to the fact that it is plesiochronous.

One of the limitations in PDH is its multiplexing method. In European hierarchy, for example, primary multiplexing to form the 2.048 Mbits/s signal is operated by interleaving 8-bit bytes from each of the 30 channels, and putting one byte from

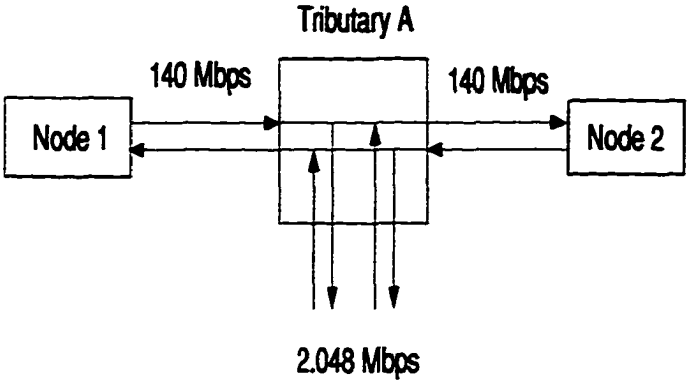

Figure 1.1: Add-Drop Application

each channel in a frame. The frame structure is identifiable within the bit stream with the presence of the frame synchronization code. Higher order multiplexing also uses single frame structure where bounded byte structure of the primary multiplexed signal is not retained at higher levels. Higher levels merely treat the signal to be an unstructured 2.048 Mbits/s bit stream. This multiplexing method has disadvantages in the PDH. For example, if we want to add or drop a channel on the half way from a 140 Mbits/s multiplexed signal between two major centers as shown in Figure 1.1, the only way to get access to the required channel is to completely demultiplex down to a primary rate signal and then re-multiplex to re-construct the higher signal as shown in Figure 1.2. This would significantly increase the cost of equipment at the relay stations.

Other limitations are (1) both ends of a link must be from the same supplier preventing possibilities of re-configuring networks and interchanging links externally, and (2) there are too few overheads for supervisory and management.

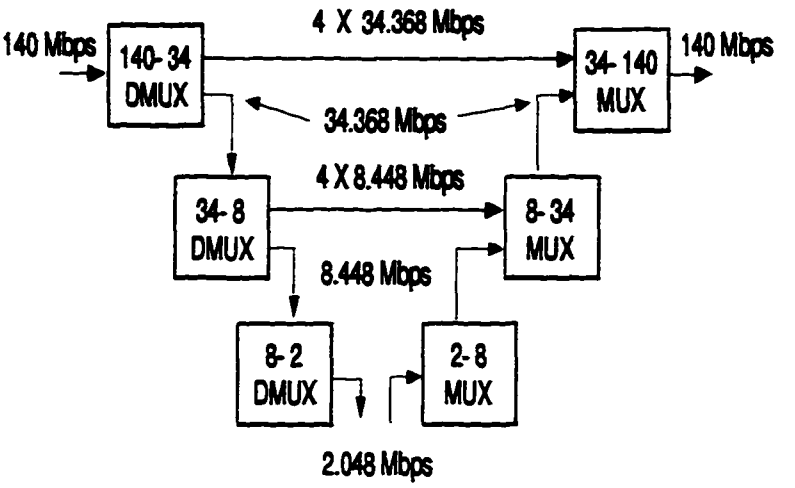

Figure 1.2: Add-Drop in Tributary A

As a result, the synchronous transmission has been introduced to lift the limitations of the PDH, and to extract individual circuits from high capacity systems without having to demultiplex the whole system. In 1984, Bell Communication Research (Bellcore) introduced the concept of Synchronous Optical Networks [16], SONET that was adopted by American National Standards Institute(ANSI) as the first standard for a synchronous hierarchy with many developments in the digital communication networks [3] [13] [17]. Based on the North American synchronous optical network and proposal devised by the International Telecommunications Union, ITU-T proposed in 1988 a draft known as Synchronous Digital Hierarchy(SDH) for worldwide digital communication networks that became in 1993 a group of three recommendations G.707, G.708 and G.709 [6]-[8]. These recommendations define a number of basic transmission rates within the SDH. The first of these is the 155.520 Mbits/s, usually called Synchronous Transport Module Level 1(STM-1). Higher synchronous

Table 1.2: Synchronous Digital Hierarchy(SDH, in kbits/s)

Level	Hierarchical bit rate
1	155,520
4	622,080
16	2,488,320

digital hierarchy bit rates shall be obtained by byte-interleaving N frame-aligned STM-1s to form STM-N signals so that the higher rate is exactly $N \times 155.520$ Mbits/s. At present ITU-T recommends STM capacities for N=4 and N=16, see Table 1.2. Performance with higher N values is to be investigated. The recommendations also define a multiplexing structure whereby an STM-1 signal can carry a number of lower signals as payload, including existing PDH signals.

Synchronous digital multiplexing and related synchronous digital hierarchy offer many advantages, such as:

- simplified multiplexing/demultiplexing techniques;

- direct access to lower speed tributaries, without multiplexing /demultiplexing the entire high speed signal;

- enhanced Operations Administration and Maintenance(OAM) capabilities;

- easy upgrade to higher bit rates in step with evolution of transmission technology;

- allow the transportation of digital signals at hierarchical bit rates as specified in Recommendation G.702 and at broadband channel bit rates.

Because it is easy and flexible to handle various services in different bandwidths from 64 Kbits/s to 150 Mbits/s or higher, the establishment of SDH gives a tremendous activation for wider researches and applications of the synchronous optical network technology worldwide [18]-[30]. Reference [31] discusses a ring architecture which uses the ATM virtual path concept to reduce the SONET ring cost in terms of bandwidth management. In [32], two methods which are used for automatically tracing a network connection and gathering network configuration data in an SDH network are proposed. Liu et al [33] described some basic criteria for the type of Synchronization Status Message within a SONET network. References [34]-[41] introduced a lot of applications of SDH network in Europe. At the same time, global undersea communication networks, with high rate based on SDH broadband transport technologies, are currently under construction. The Transatlantic Telephone Cable Network (TAT-12 / 13) will connect North America and Europe [42]. The Fiberoptic Link Around the Globe Cable System (FLAG) will link 12 countries with over 120,000 voice channels via 27,000 km [43]. The TPC-5 Cable Network (TPC-5 CN) will be the first self-healing trans-Pacific ring network which consists of a ring of undersea cables connecting six network nodes at six cable landing sites [44]. The Asia Pacific Cable Network (APCN) will interconnect 9 Asia countries and areas. It is a regional undersea telecommunications network with an 11,500 km trunk and branch

[45]. Using a combination of wavelength-division multiplexing (WDM) and SDH multiplex and cross-connect equipment, the Africa Optical Network will encircle the entire continent of Africa with an undersea fiber optic ring network [46]. Future satellite communication is also required to carry the ITU-T synchronous signal, either STM-1 or its integer multiples SDH signals. Such a digital satellite communication system with the ITU-T standardized interface will be feasible [47].

1.3 Interface Structure

1.3.1 Network Node Interface

Network node interface(NNI) specifications defined in Recommendation G.708 enable interconnection of synchronous digital network elements to transport payloads, including digital signals of the PDH defined in Recommendation G.702. Figure 1.3 gives a possible network configuration to illustrate the location of NNI [7].

NNI introduces a new concept of Virtual Container(VC). It refers to a limited set of payload structures that have specific size and structural relationship with each other and have the ability to carry several tributaries having different capacities and formats. This method makes it possible to multiplex, cross-connect, and switch various tributaries without their knowledge and contents. Furthermore, the VC "floats" within the NNI frame, so that the virtual container frame alignment is not required at a transit node. Hence, time delay at transit nodes could be minimized.

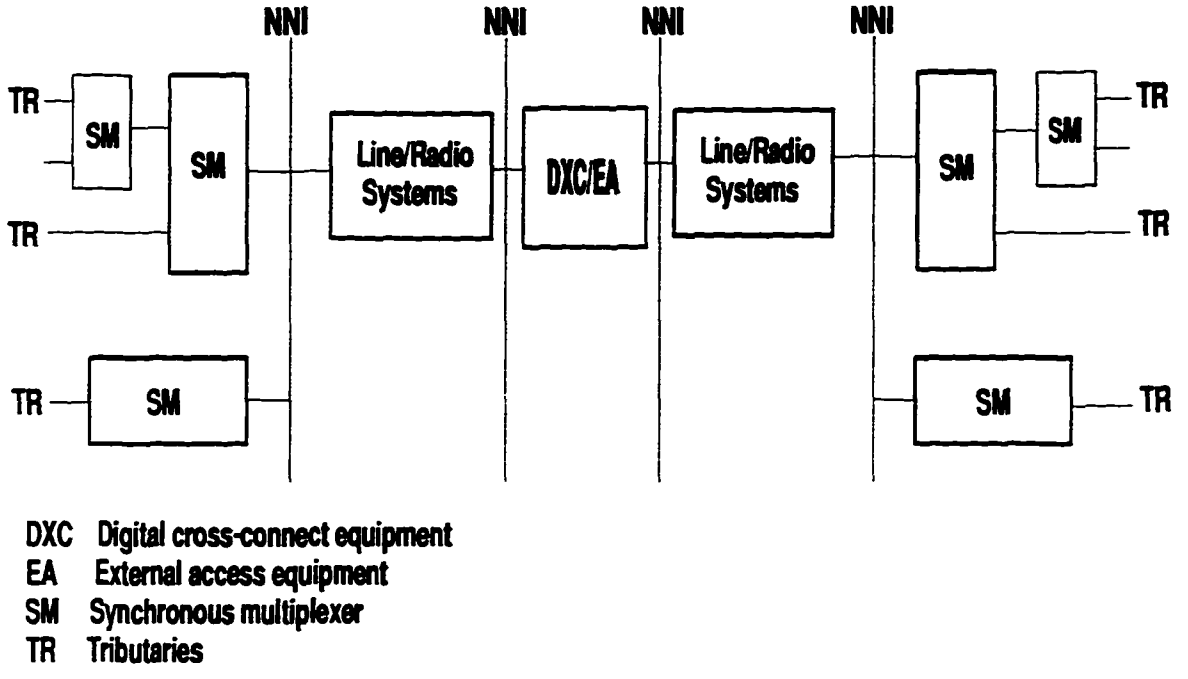

Figure 1.3: NNI Locations in SDH Networks

1.3.2 User-Network Interface

The User-Network Interface (UNI) is the mean by which subscriber terminal equipment, i.e., telephone, data terminal equipment, video coder, etc., access a higher serial bit stream. Such a user-network interface implementation can be fully compatible with the NNI. This compatibility avoids signal concersion which has to occur when user's signals are transmitted via the network. In this application a framing chip and byte-wide first-in/first-out (FIFO) buffers provide the interface between transmission and reception equipment and the network. At the transmission end, the chip generates strobes to read data and control bytes from the FIFO to its parallel data input port and produces a properly framed data stream at its serial data

output port. At the receiving end, the chip detects a framed data stream applied to its serial data input port and presents the data bytes on its parallel data output port to the FIFO along with the appropriate write strobes.

1.3.3 Plan of Work

According to the interface features above three aspects will be studied to develop SDH transmission network framework. The major objective is to propose a new SDH frame synchronization scheme. Buffer capacity will be determined for SDH payloads multiplexing. Block errors in payload transmission will also be estimated.

1.4 Features

The advantages of the proposed frame synchronization approach, determination of buffer capacity and estimation of errored blocks are listed in the following.

- Optimize the SDH frame synchronization scheme for high speed operation, provide the natural integration of demultiplexing and SDH frame synchronization detection functions, improve the receiving system performance, and reduce the system cost.
- Avoid losing data within the gaped duration by using buffer. Calculation of the buffer capacity is simple.

- Simplify the estimation of errored blocks in transmission of different virtual containers.

1.5 Outline of the Dissertation

In Chapter 2, after reviewing two traditional frame synchronization techniques-serial and parallel modes, we will propose a new parallel frame synchronization scheme for SDH network according to the byte-interleaving feature in SDH payload transmission. Performance with respect to parameters will be analyzed.

In Chapter 3, based on discussing SDH payload multiplexing features, we will present a buffer method to avoid information loss within the gapped duration and determine buffer capacity of SDH payload multiplexing. Buffer capacity table for multiplexing three C-3 payloads will be given.

Chapter 4 systematically describes Bit Interleaved Parity (BIP) code used for monitoring errored blocks. In order to relieve the shortage of BIP which does not detect even numbers of errors, we need to consider the case where the error bits are distributed as even numbers. We will find a closed form for solving probability of undetected errors, estimate errored block rate of each virtual container in STM-1 structure, and give a group of curves.

Finally, Chapter 5 will give conclusions to the dissertation and outline potential extensions and directions for further research.

Chapter 2

PARALLEL FRAME SYNCHRONIZATION SYSTEM

2.1 The Need For Synchronization

SDH transmission network uses synchronous time division multiplexing technique. It involves thousands of communication public and private system switches, and requires that all the transmission paths, which are connected to each of the digital switching nodes, must occur in intervals which start at the same moment. Each node must be able to reconstruct and reroute frames received in a reliable manner, and have access to sources that can report time in accurate 125 microsecond period, a basic time unit formed by the sampling rate of digital voice. To ensure that each multiplexing equipment is synchronized with other equipment in the network, synchronization must exist at three levels(i.e., bit, frame, and time slot) of transmission system. A brief explanation of each level is presented below.

1. Bit synchronization is required for a receiver exactly to restore the same bit sequence as the transmitter sent. It deals with physical layer and involves timing issues, such as: clock insertion and recovery, transmission line jitter, sampling windows in eye patterns, and intersymbol interference. These issues are addressed by placing requirements on the clock and the transport system, and by adhering to engineering rules such as maximum repeater spacing and number of repeater spans.

2. The frame timing level of synchronization refers to the need of the transmitter and receiver to achieve proper phase alignment so that the beginning and end of a group of bits can be identified. The frame, as in STM-1 signal of SDH, is a group of bits (19,440 bits) consisting of information data and overheads bytes. The STM-1 bit rate is 155.52 Mbits/s, the frame period is 125 μsec. The time slots are distributed to particular circuit users. The frame synchronization signal, which is encoded in the digital system and normally formed by a means of a specific combination of symbols, accomplishes the function of identifying the time slots so that they can be processed separately. Once frame synchronization state is determined, each time slot is identified and stored for processing. Loss of frame synchronization clearly renders the whole information stream undecodable, and is therefore much more serious than the loss of the same proportion of information bits. The main issues at the frame synchronization are synchronization incoming, reframe and frame synchronization

holding [48] [49].

3. The network timing level deals with processing of time slots. The time slots are time-division multiplexed into an STM-1 frame by a digital system located at a source node and transported by a digital transmission system.

In this dissertation, we are only concerned about frame synchronization. References [50]-[54] have more details dealing with bit synchronization and network timing. After reviewing conventional frame synchronization approaches in the subsections below we will introduce the strategy of frame synchronization system in SDH transmission network. Then based on the analysis of the frame synchronization code recommended by ITU-T, we will present our new parallel frame synchronization scheme.

2.2 Reviews of Existing Frame Synchronization Systems

There are two basic traditional frame synchronization methods to be available for SDH transmission systems, namely, the high speed frame synchronization approach and the low speed frame synchronization approach [55]-[58]. Figures 2.1 and 2.2 illustrate the principles of the two approaches, respectively.

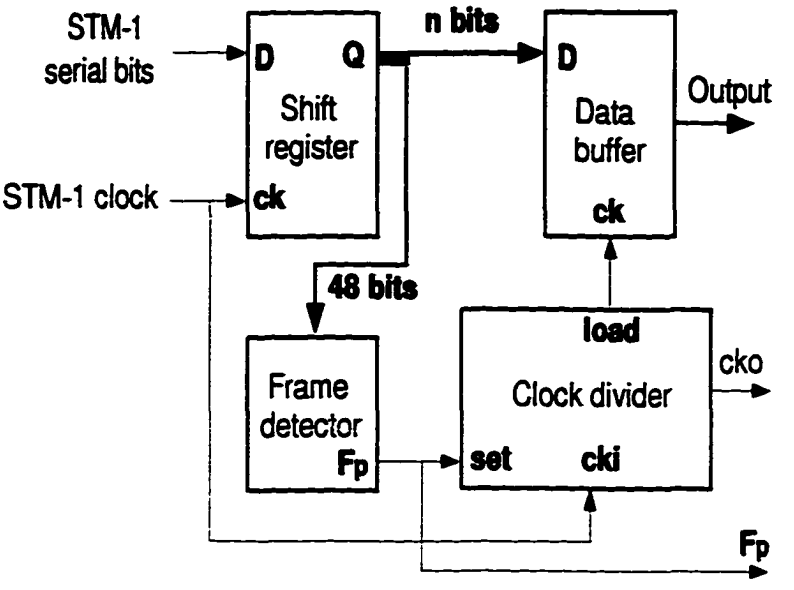

Figure 2.1: High Speed Framing Approach

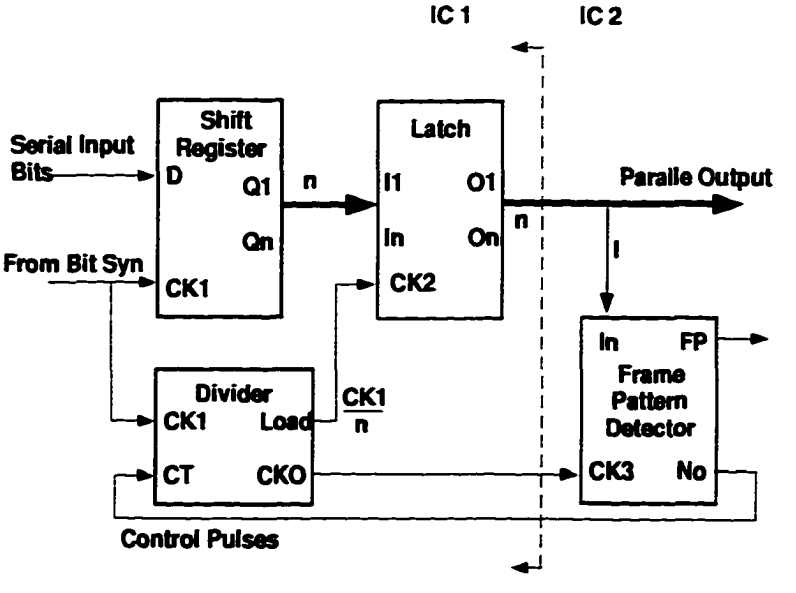

Figure 2.2: Low Speed Framing Approach

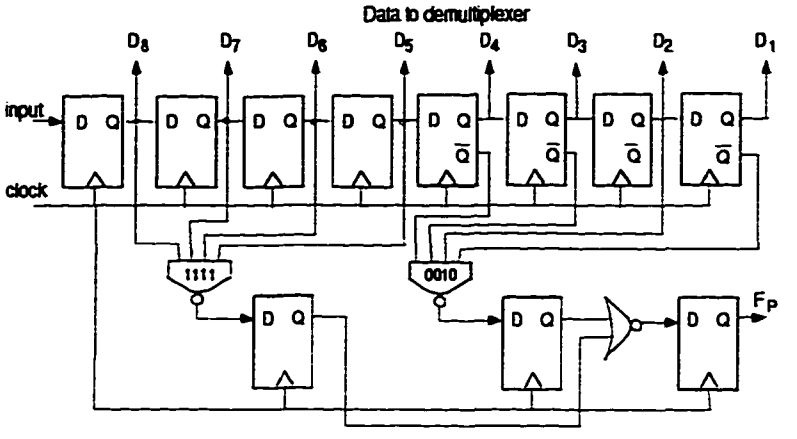

Figure 2.3: High Speed Frame Synchronization Detector

2.2.1 High Speed Frame Synchronization Approach

For searching frame synchronization code, the high speed approach shown in Figure 2.1 uses detector which is made up of high speed circuit. A logic diagram of the detector is illustrated in Figure 2.3 [55].

In Figure 2.3, Data flow is input in series by clock into a shift register with eight bits wide and then data with byte wide becomes visible at the output. If the shifted bits match a predetermined frame synchronization code, a detecting pulse F_P with a bit wide will be produced and used for setting the clock divider circuit to a state decided in advance so that the outputs of the data buffer are properly synchronized and demultiplexed. As shown in Figure 2.3, the input bit to the detector is changed once every bit, so the detector is operated at the line rate. This approach is

suited for detecting bunched frame synchronization sequences. Its synchronization incoming time is fast and design is conceptually simple since the approach searches frame synchronization code in bit by bit way. However, just because the detector recognizes frame synchronization code from a high speed bit stream, the width of its frame synchronization pulse is too narrow. This means that all circuits of the frame synchronization system have to operate at the line rate and probably add stringent limitation on timing delay of demultiplexer operation. For the case of STM-1, the width T_b of each bit has only 6.4 ns. In order to complete a frame synchronization process within 6.4 ns, it is difficult to design frame synchronization system. We have to use high speed integrated circuits for the complete frame detection circuit in STM-1. It is more difficult to design the frame synchronization system of STM-N. Therefore the traditional high speed frame synchronization approach is not well adaptable for the SDH transmission networks with the rate of Gbits/s.

2.2.2 Low Speed Frame Synchronization Approach

In order to improve the performance of the line interface demultiplexer, frame synchronization code detector could be implemented at low speed. An illustration of the low speed frame synchronization approach for SONET STS-N receiver is shown in Figure 2.2. In Figure 2.2, unlike the high speed frame synchronization approach in which output of the shift register is directly connected to the frame synchronization code detector, instead output of the shift register is indirectly connected to the frame

synchronization code detector via a latch. The latch transfers its data bits to the detector in parallel. This makes the detector output change one time every m bits, where m may be equal to the length of the frame synchronization code. Clearly, it could generate a wider frame detecting pulse than one in the low speed approach and allow to become less tight on timing delay requirement for successive circuits. Such an approach usually performs functions of both the high speed demultiplexing and low speed frame synchronization detection using two or more separate integrated circuit chips resulting in extra stiff timing requirement on the integrated circuits, their interfaces from different points. And it also increases in synchronization incoming time for the reasons described later in the next section.

2.2.3 Improved Low Speed Frame Synchronization Approach

Reference [56] presents an improved approach for SONET frame synchronization system. Figure 2.4 shows a diagram of the system. In this approach, SONET frame synchronization is completed in two steps: the first step is byte alignment, and the second step is frame detection. A byte aligner is added to perform the byte alignment function by identifying the first byte of STS-N frame synchronization code. And a traditional parallel detector is used to perform frame synchronization detection function by identifying frame synchronization code. The advantage of the approach is that it gives the natural integration between SONET frame synchronization detection and demultiplexing. However, the addition of the byte aligner and its operation

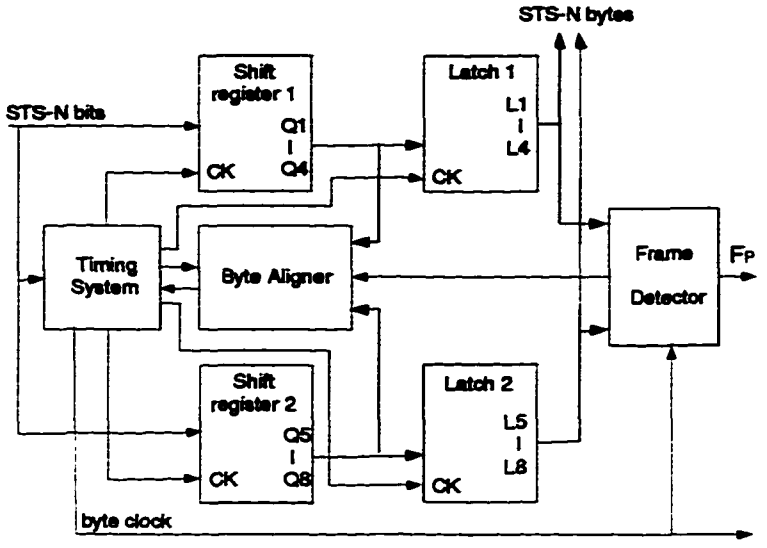

Figure 2.4: SONET Demultiplexer with Byte Aligner and Frame Detector

results in the probability, that any random data mimic the first byte of the frame synchronization code in the input data bit stream, increasing to 2^{-8} but not 2^{-24} as described in [56]. Secondly, two 4-bit latches, which use respectively the different edges of the clock signal, introduce design complexity of the approach. Finally, the approach still does not overcome the shortage of long synchronization incoming time, and it can cause bigger loss in the information bits [57].

The traditional frame synchronization approach in a serial manner provides only a very narrow pulse as the frame synchronization signal for the successive circuits. This strategy imposes strict timing constraint on the related circuits which, in turn, leads to substantial increment in the frame system design complexity. On the other hand, the traditional parallel approach causes longer synchronization incoming time. According to the feature of byte-interleaving in SDH networks we propose a new SDH

frame synchronization scheme which combines the advantages from the traditional approaches. It provides a wider frame detection pulse for consecutive circuits, has a shorter synchronization incoming time than that of the traditional approach, and provides the natural integration of demultiplexing and SDH frame synchronization detection functions. It can improve integral performance of the frame synchronization system.

In the sections below we will describe strategy and implementation scheme for frame synchronization in SDH transmission networks.

2.3 SDH Frame Synchronization Strategy

2.3.1 Two States in Frame Synchronization System

If there are not certain identifying patterns, a sequence of digital bits bearing information is not decodable. Most digital transmission systems count on the use of a specified digital sequence to correctly identify the information bits. The sequence is inserted at regular interval and generates temporal frame with fixed length for simple decoding at the destination. Such sequence is called a frame synchronization code or flag. A process of getting the frame synchronization code at the destination is called frame synchronization or frame alignment. The frame synchronization code can be inserted into a frame using one of the following two methods,

1. Bunched method: in which the frame synchronization code occupies consecutive digit time slots;

2. Distributed method: in which the frame synchronization code occupies non-consecutive digit time slots.

SDH uses the bunched method and arranges a group of six bytes [7] described in formula (2.1), in the STM-1 frame. These bytes are used for identifying the beginning and end of each transmitted frame and for the purpose of frame synchronization in the receiving system.

$$FSC = A_1 A_1 A_1 A_2 A_2 A_2 \tag{2.1}$$

For convenience, we first introduce two basic operating states which are used in the proposed parallel frame synchronization system: the in-frame state, and the detecting state.

Assume that the frame synchronization system is initially correct. That is, n bits of the received bit stream can be shifted into receiver register in which the first N bits are the frame synchronization code. A detector device is used to detect the frame synchronization code by checking whether there is a match between the preset frame synchronization code in the detector and the received N bits. If the match is correct, the next n-N bits are information data which will be transferred to a demultiplexer

for further processing. Then the next n bits are shifted into the register and the process above is repeated. We call this operation, an in-frame state.

If the frame synchronization is lost because of some reasons that will be studied below, the frame synchronization code will not appear in the expected location, and the information data will not be decoded correctly and transferred to the demultiplexer for processing. This causes the frame synchronization system to detect synchronization code again. We define this operation a detecting state. Later we will analyze the performance of proposed parallel frame synchronization system using these two states.

2.3.2 Strategy of SDH Frame Synchronization

Like other ones, frame synchronization system of the SDH should be designed to deal with three major problems. They are as follows:

1. Channel errors may corrupt the received frame synchronization code. If the frame synchronization system is in the in-frame state, these errors may cause a transition to the detecting state.

2. Slips may result in a loss of bits or the addition of bits to the sequence. If the system is in the in-frame state, slips will result in repetitive errors in the frame synchronization code detector tests, and thus necessitate a transition to the detecting state.

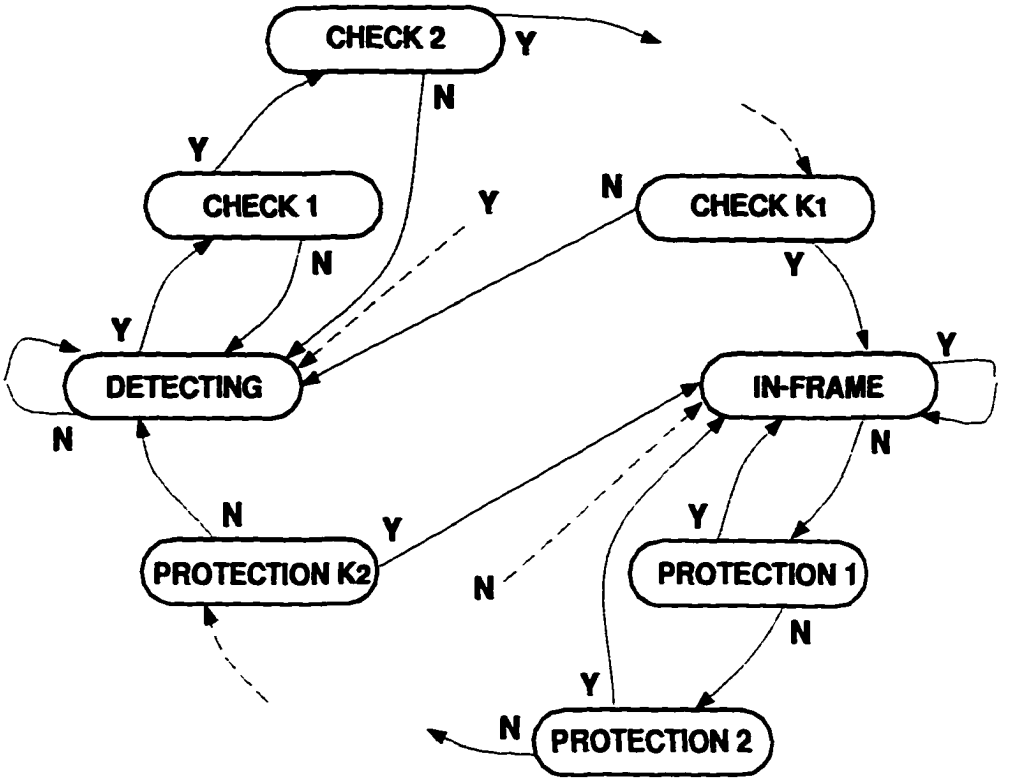

Figure 2.5: State Transfer Diagram

3. Information data may happen to simulate the frame synchronization code. These will have no effect if the system is in the in-frame state. However, if it is in the detecting state, it may be caused to go into the in-frame state but, in fact, still remain out of synchronization.

Considering the states and problems above we use the frame synchronization strategy shown in Figure 2.5 for the SDH transmission system. If valid frame synchronization code are detected in K_1 consecutive STM-1 frames, the system will declare itself "in-frame" which indicates that the system is in frame synchronization state. Once the system is in the normal in-frame state, it will have to detect at least K_2 consec-

utive invalid frame synchronization codes before it can declare itself "out of frame". This is to ensure that the system will not experience frequent "misframes", i.e., false out of frame due to the presence of line errors. Once in the out of frame state, a signal will start detecting new STM-1 frames. In the subsections below, after reviewing conventional frame synchronization approaches we will analyze characteristics of the frame synchronization code in the STM-1 frame. Based on the aforementioned strategy, we will present our new parallel frame synchronization scheme.

2.4 Proposed Parallel Frame Synchronous System

Although there are many traditional methods which can be used to design frame synchronization system of STM-1, we find that there are problems in these methods. The primary one is that the width of frame synchronization detection pulse is too narrow since frame synchronization system recognizes frame synchronization code from a high speed bit stream, which means that all circuits of frame synchronization system have to operate at the line rate. For the case of STM-1, the width T of each code bit has only 6.4 ns. In order to finish a process of frame alignment within 6.4 ns it is difficult to design a frame synchronization system. We are required to use high speed integrated circuits (ICs) for each part, such as ECL ICs, for implementing a synchronous recognizer, a synchronous check counter and a synchronous protection counter in STM-1. It is even more difficult to design the frame synchronization system of STM-N.

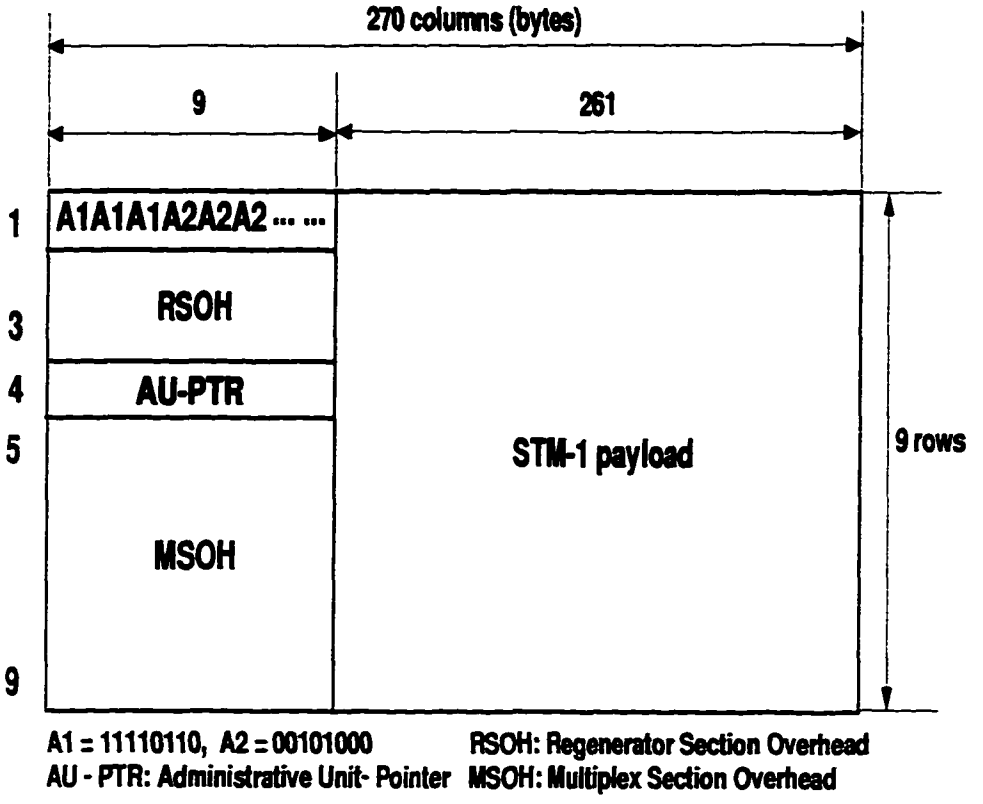

Figure 2.6: STM-1 Frame Structure

In this section, we first analyze the features of the STM-1 frame structure and frame synchronization code, then present our scheme based on them.

2.4.1 STM-1 Frame Structure

STM-1 frame structure in SDH systems is shown in Figure 2.6. The frame has a byte-structure containing 9 rows × 270 columns byte size. The frame period equals 125μsec. The first 9 columns comprise the section overhead (SOH) and administrative pointer(AU-PTR), the rest of the bytes are dedicated to path overhead(POH)

and payload. SOH is used to realize main functions such as frame synchronization, error checking, data communication, protection switch control and maintenance. AU-PTR gives not only the offset in bytes between the pointer position and the first byte of the payloads but also the means of frequency justification. Payload area provides flexible size containers to carry payloads and virtual containers for various services. For example, it can perform payload mapping of ATM cells, each of which is a block with 53-byte fixed length. The frame is transmitted first from left to right, and then row by row. Various types of digital traffic are multiplexed to the frame in terms of byte size. In order to demultiplex correctly, each received frame must synchronize with frame boundaries.

2.4.2 Frame Synchronization Code Characteristics

As we know, a combination of random data may be the same as the required frame synchronization code and channel interference may distort the frame synchronization code. The former will lead to false synchronization, and the later will cause a leaky synchronization. The computing formulae for the false synchronization probability of P_{FS} and the probability of leaky synchronization P_{LS} are given below:

$$P_{FS} = \frac{1}{2^n} \tag{2.2}$$

$$P_{LS} = 1 - \sum_{i=0}^{k} \binom{n}{i} \cdot P_e^i \cdot (1 - P_e)^{n-i}. \tag{2.3}$$

where P_e is the probability of channel bit error, n is the length of frame synchronization code in unit bit, and we assume that the number of permissible errors in n-bit frame synchronization code transmitted through a channel is k.

When the number of permissible errors equals zero, i.e., $k = 0$, then

$$P_{LS} = 1 - (1 - P_e)^n \tag{2.4}$$

Table 2.1 provides the values of P_{LS} and P_{FS} for $P_e = 10^{-7}$ and n=0,8, ... ,48 respectively. From Table 2.1 we learn that the value of n should be selected large, making the probability of any random data mimicking this 48 bit pattern equal 2^{-48}, and ensuring short average reframe time and infrequent false frame synchronization for a Gbits/s SDH system. Table 2.1 also indicates that as n increases P_{LS} increases and P_{FS} decreases. One of the ways to solve this contradiction is to improve bit error rate of the transmission channels, which can be achieved by using optical fiber as the transmission medium. Since the optical fiber has many advantages such as large bandwidth, low loss, high transmission security, and vulnerability to electromagnetic interference, it has become one of the most important and attractive media for telecommunication networks. In fact, SDH is the standard for transmission over optical fiber medium.

Table 2.1: Values of P_{LS} and P_{FS} for n under $P_e = 10^{-7}$

n	P_{LS}	P_{FS}
0	0	1
8	9.537×10^{-7}	3.906×10^{-3}
16	1.901×10^{-6}	1.526×10^{-5}
24	2.861×10^{-6}	5.961×10^{-8}
32	3.815×10^{-6}	2.328×10^{-10}
40	4.768×10^{-6}	9.095×10^{-13}
48	5.722×10^{-6}	3.553×10^{-15}

Another way is to select the pattern and length of FSC suitable for both, P_{FS} and P_{LS}.

Let us consider an overlap region where the system has slipped out of synchronization by only a small number of bits less than the frame synchronization code length n, i.e., part of the received bit stream contains both data and the frame synchronization code bits. For example, assume that synchronization is lost for the case where an 8-bit pattern is being used by one bit slip. This is illustrated in Figure 2.7 for the case where the frame synchronization code is 11111111. In this case, it is easy for false synchronization to occur when the adjacent data bit x_1 or y_1(followed by the first or last 7 bits of the frame synchronization code) is equal to 1. The related

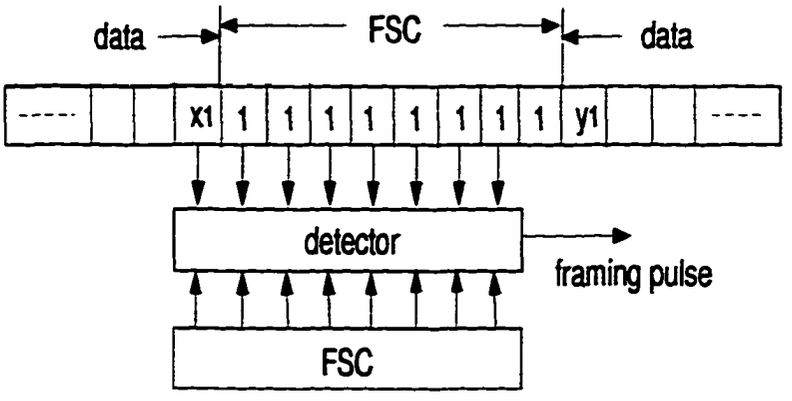

Figure 2.7: False Synchronization caused by Random Data

probability of y_1 or $x_1 = 1$, is 0.5. Clearly it is important to choose an optimal frame synchronization code in digital transmission system, especially in high speed system. References [59]-[61] give a detail discussion about how to choose a frame synchronization code. Here, we emphasize one of the most important rules, that the choice of frame synchronization code pattern should minimize the probability that the random data simulates a false frame synchronization code.

Formula (2.1) was used so that the probability of false frame synchronization by random data in the overlap region is zero for up to (n-1) time slips. In the design and performance analysis of the proposed parallel frame synchronization scheme we will use this feature.

As for the length of FSC it can be seen from Table 2.1 that reducing n will decrease P_{LS} and increase P_{FS}. This means that synchronous state can not be established very quickly. It is important to consider the effects of P_{FS} and increase the values of n first in a way that it may not make channels efficiency too low. After considering

the factors above, the n value of STM-1 is selected and it is equal to 48. Now the ratio of occupied channels related to n is:

$$\eta = \frac{n}{B} \tag{2.5}$$

where B represents the number of bits in an STM-1 frame. When $n = 48$ and $B = 19440$, $\eta = 0.25\%$. The value of η here is smaller than that for a rate of 139.264 Mbits/s, a rate in ITU-T recommendation G. 751. It is clear that a larger n makes P_{FS} diminish and the time of incoming synchronous state shorter.

2.4.3 General Principle of PFSS

Once a group of frame synchronization code is selected and its arrangement is located in the frame structure, the performance of a frame synchronization system will be determined by a method of implementing frame synchronization.

Parallel processing has emerged as a key enabling technology not only in modern computers, but also in other fields [62]. In order to relax operating speed requirement for some circuits in the frame synchronization system and implement frame synchronization system of STM-1 using low rate integrated circuits, we devise a new parallel frame synchronization system. The concept of parallelism in a computer system has been exploited to design a scheme of parallel frame synchronization system for STM-1 transmission structure as shown in Figure 2.8. It is based on the byte

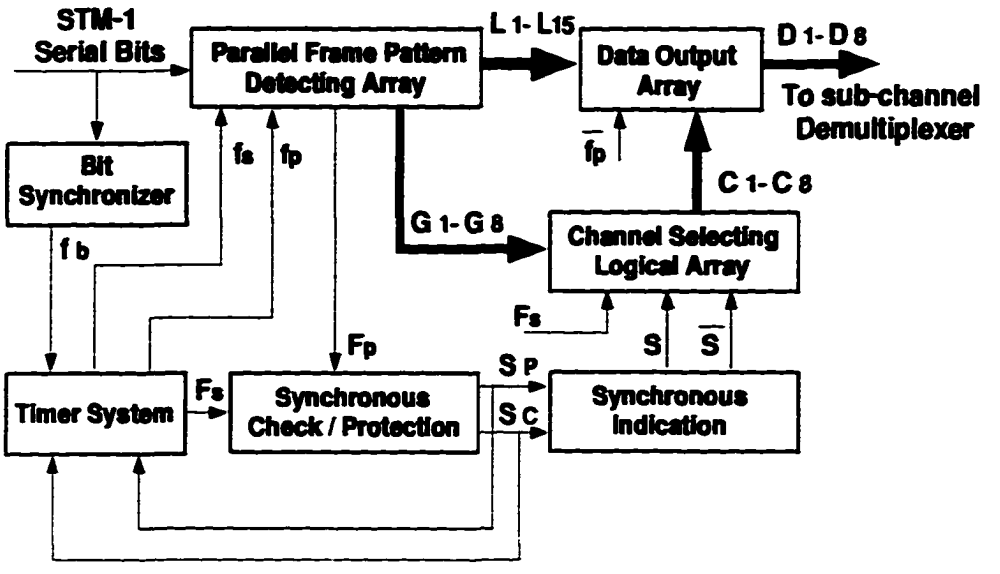

Figure 2.8: Diagram of Parallel Frame Synchronization System

multiplexing feature of ITU-T Recommendation G. 708.

In Figure 2.8, the bit synchronizer uses digital phase locked loop. It extracts clock signal $f_b(f_b = 155.520MHz)$ from 155.520 Mbits/s serial input bit stream. By using f_b, the timer system generates bit clock pulse f_s with a frequency of 155.520 MHz, byte clock pulse f_p with a frequency of 19.44MHz, and frame clock pulse F_s with frame repetition frequency of 8KHz. Once an identical frame synchronization code with formula (2.1) is detected, Parallel Frame Pattern Detecting Array(PFPDA) of FSC in PFSS will produce a frame synchronization pulse F_p with the width of 8T(to be discussed below) making the rest of the circuits operate at a rate of $\frac{1}{8}f_s$. Synchronous check counter in the Synchronous Check and Protection unit(SCP) begins to record the number of F_p pulses, if it gets K_1 times in succession which is referred to as synchronous checking parameter and set to avoid the false synchronous phe-

nomenon to a certain extent. Then the counter in the Synchronization Check and Protection unit sends a signal S_c to the Synchronous Indication unit(SI), and the frame synchronization system enters frame synchronization state. The synchronization indication signal, together with the output from G_j which is generated by frame synchronization code, enables Channel Selecting Logical Array(CSLA) to produce C_j(j from 1 to 8). C_j opens a proper data output channel of Data Output Array(DOA) and allows data in byte between L_1 and L_{15} of the parallel frame pattern detecting array to be demultiplexed correctly. If the frame synchronization system worked in synchronization state fails to get a F_p pulse on the location of the frame synchronization code, the synchronous protection counter in the Synchronous Check and Protection unit starts counting instantly. When the counted number of the counter exceeds K_2, which is referred to as synchronous protection threshold and set to avoid the leaky synchronous phenomenon, frame synchronization system begins the reframe process.

Our scheme differs significantly from the traditional approaches in detecting frame synchronization code, channel controlling unit, and data output unit. We will explain their main concepts in the following subsections.

2.4.4 Parallel Frame Pattern Detecting Array

A block diagram of the Parallel Frame Pattern Detecting Array is shown in Figure 2.9. Input bits at rate of 155.520 Mbits/s are shifted by f_s bit by bit to a Serial-In,

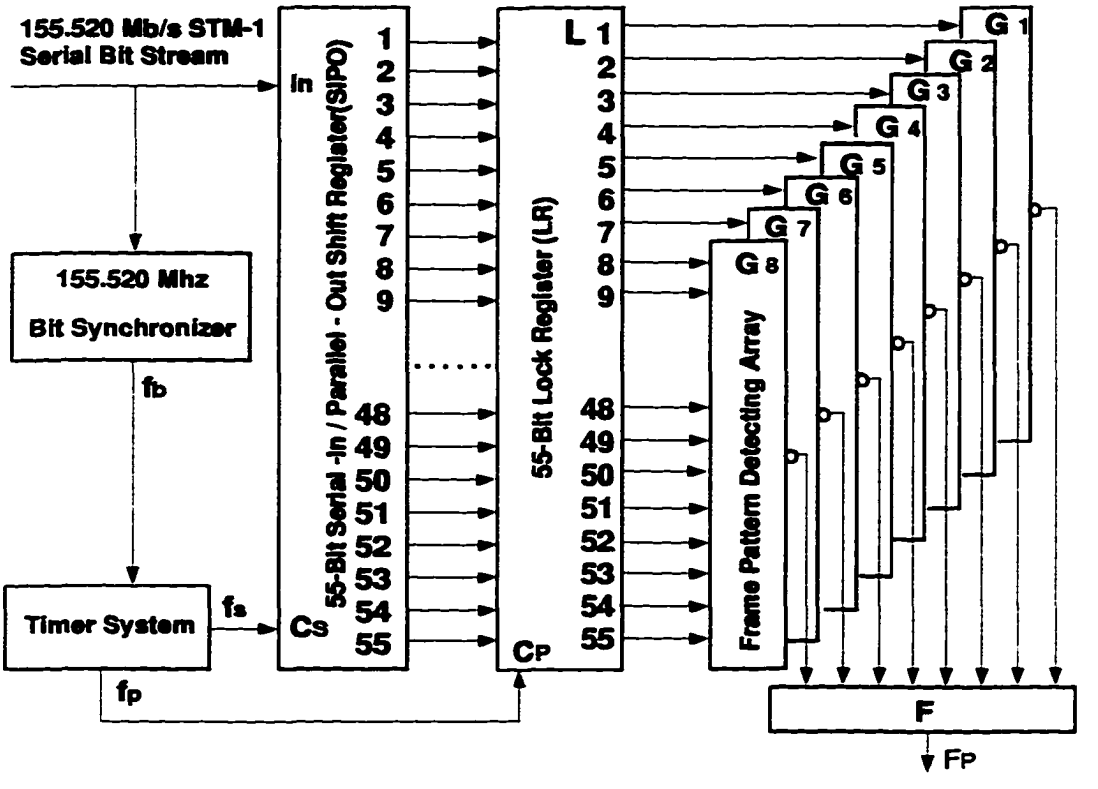

Figure 2.9: Parallel Frame Pattern Detecting Array

Parallel-Out(SIPO) shift register. Fifty five output lines of the SIPO are connected to a 55-bit Lock Register(LR) in parallel. When byte clock signal $f_p(f_p = \frac{f_s}{8})$ enables LR, the data from Serial/Parallel Shift Register are fed in parallel to the lock register once every eight times of T($T = \frac{1}{f_s}$). Fifty five output lines of the lock register are connected to a group of detectors (Frame Pattern Detecting Array) of frame synchronization code every one bit, i.e., the detecting array G. There are eight detectors in G (G_j as shown in Figure 2.9, where j=1,2,...,8) because one byte consists of 8 bits. Each detector contains 48 inputs. Their connections with the Lock Register are shown in Table 2.2. In each detector a comparator is built in to check the frame synchronization code in formula (2.1). The comparator accepts 48 bits in parallel from the lock register that are compared with the pattern in formula (2.1) and produces an output signal, G_j. Connections of the detecting array to the fifty five-bit register are to ensure that the detecting array can detect the frame synchronization code in the worst case when the code slips the register up to seven-bit positions.

In consideration of selecting the pattern in formula (2.1), it is known that when the frame synchronization code is in the mid of an area of (3n-2) bits long, it is not possible for the frame synchronization code to present twice or more within the area. Thus, if a frame synchronization code included in the 55 bit codes is shifted every time, there is only one detector of the array which can respond to input and there are no outputs in the rest. If all outputs in G_j are equal to '1' then F_p ='1'

Table 2.2: Connections between PFPDA and LR

G_j	Bits from Lock Register
G_1	$L_1 - L_{48}$
G_2	$L_2 - L_{49}$
G_3	$L_3 - L_{50}$
G_4	$L_4 - L_{51}$
G_5	$L_5 - L_{52}$
G_6	$L_6 - L_{53}$
G_7	$L_7 - L_{54}$
G_8	$L_8 - L_{55}$

which represents that no frame synchronization code is detected by the parallel frame detecting array and no negative pulse is generated in F. The frame synchronization system will continue searching for frame synchronization code. If one of the G_j's detects frame synchronization code, G_6 for example, then G_6 ='0', G_j ='1'($j \neq 6$), output of F equals to zero represented by a negative pulse F_p. This pulse is delivered to the synchronous check counter in the synchronization checking and protection unit for further processing. Because the data in the lock register change once every byte, the width of F_p in the output of F will hold for $8 \times T$, eight times longer than that of conventional methods. F_p makes the synchronization checking and protection unit enter checking mode. When the value of the counter in the synchronization checking and protection unit equals K_1, the check parameter being preset according to the design requirement, synchronization checking and protection unit sends a signal to synchronization indication, thus frame synchronization system enters the synchronous state.

The system realizes a trade-off between time and space by increasing the number of the detecting channels of the frame synchronization code. Comparing to the improved approach our scheme has two advantages. One of them is that the speed of incoming frame synchronization code (we will analyze it in coming section) in the new parallel frame synchronization system is higher than the traditional parallel mode in [56]. In [56] one byte is checked by detector at a time. If one bit position in frame synchronization code is slipped by the detector, it has to wait

one frame time for next checking. This process will be repeated until the byte of the frame synchronization code exactly occurs in the detector. However, the new scheme could not miss the frame synchronization code even under the condition that up to seven-bit positions are slipped by the detecting array since the scheme uses fifty five-bit wide register in the detecting array. The other one is that the parallel frame pattern detecting array generates wider frame synchronization pulse than the conventional approach. It reduces the requirement of the rate of the successive circuits to one-eighth of the traditional method, and creates possibility for using lower speed integrated circuits in order to demultiplex the information data bits from high speed bit stream.

2.4.5 Channel Selecting Logical Array (CSLA)

The G_j signals in the Parallel Frame Pattern Detecting Array are used to generate both F_p signal (see Figure 2.8) and C_j channel selecting signals in the Channel Selecting Logical Array (see Figure 2.10). Channel Selecting Logical Array consists of 8 units with identical structure. The structures of the channel selecting logical array and subunit are shown in Figures 2.10 (a) and 2.10 (b), respectively.

Let's take $j = 6$ as an example, as shown in Figure 2.10 (b), to explain the basic operation of the channel selecting logical array. From the Detector, G_6 is connected to an input of a D flip-flop. If G_6 ='0' and the clock input F_S is enabled, Q_6 ='0' and forces the NAND gate Y_6 to be '1'. When S ='1', meaning that the frame

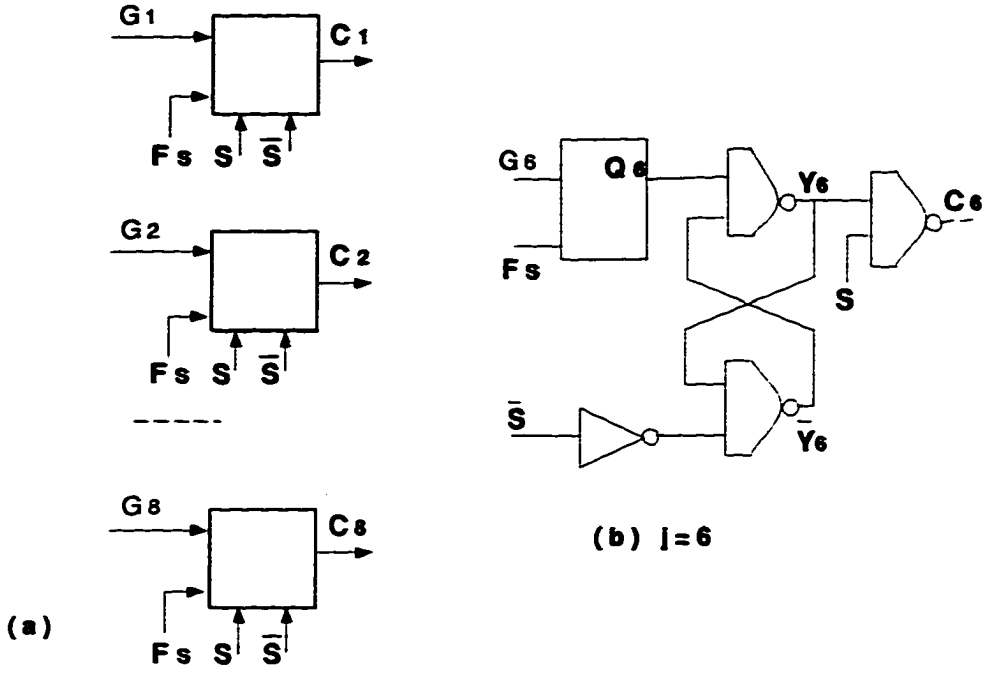

Figure 2.10: Diagram of Channel Selecting Logical Array

synchronization system is in the synchronization state, then C_6 ='0' which in turn enables the 6^{th} data register of the Data Output Array. If G_6 is asserted(G_6 ='1') K_2 times and S signal is deactivated($S = 0$) then C_6 ='0', the 6^{th} data register of the Data Output Array will be blocked and the frame synchronization system will leave the synchronization state.

2.4.6 Data Output Array (DOA)

The structure of the data output array is shown in Figure 2.11. Eight tri-state data registers D_j(j from 1 to 8), each one contains 8 bit inputs and 8 bit outputs, are connected to the outputs of the lock register from the 1^{st} bit to the 15^{th}. We still

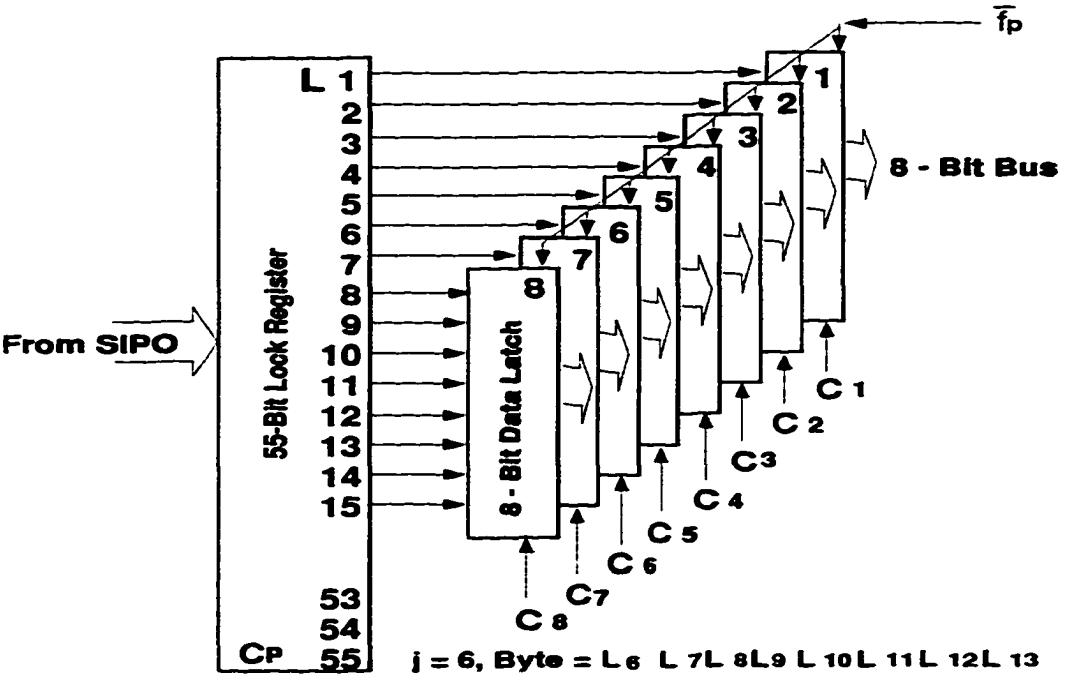

Figure 2.11: Diagram of Data Output Array

take $j = 6$ as an example to describe the operating principle of the data output array. As we know, if G_6 ='0' and S ='1', the output of C_6 equals '0'. When G_6 ='0', after shifting 8 bits the first data byte is shifted in the position between the 6^{th} to the 13^{rd} bits of serial/parallel shift register and sent to lock register by f_p. Therefore one data byte consisting of $L_6 - L_{13}$ is connected to eight inputs of the 6^{th} data register of the data output array. When C_6 is asserted contents of the 6^{th} data register are sent through $\bar{f}_p$ to the data bus for further demultiplexing, where $\bar{f}_p$ is the complement of f_p.

We have basically described the main features of the parallel frame synchronization system above. In comparison with the conventional methods, the scheme improves the conventional detector of frame synchronization code. It makes the processing in SDH systems performed at 19.44 MHz. This ensures that all operations are byte operation after the framer. Functions that follow the framer include desrcamble, section overhead monitoring, pointer processing, etc. At the same time, it has the advantage quickly to income frame synchronization. In addition, it gets the wider frame synchronous detective pulse, provides consequent circuits with sufficient processing time and accesses data bytes directly from the detector.

The improvement in channel detection is obtained here at the expense of slightly higher circuit complexity. However, it is worth as the integrated circuits cost is remarkably decreased.

2.5 Performance Analysis

Different techniques and metrics are used to analyze and measure performance of frame synchronization system [60]-[71]. As we discussed in the previous section, however, the main issues at the frame synchronization level are synchronization incoming, reframe and frame synchronization loss detection. The performance of the frame synchronization system can be measured by these three important synchronization parameters: the average synchronization incoming time T_{ASI}, the average synchronization catching time T_{ASC} and the average synchronization holding time T_{ASH}. Next, we will find the expressions for these metrics using probability theory [72].

2.5.1 Definitions of Performance Parameters

We first introduce some notations in order to conveniently perform the analysis.

- M: The length of each frame in bytes.
- N_f: The length of the frame synchronization code in bytes.
- T_F: The interval of one frame.
- T_W: The interval of one byte.
- T: The interval of one bit.
- p_e: The bit error probability, $q = 1 - p_e$.

- P_{FS}: The probability of the false frame synchronization.

- P_{LS}: The probability of the leak frame synchronization.

- K_1: The number of consecutive frames before entering in-frame state, which is used for avoiding the false synchronous phenomenon to a certain extent.

- K_2: The number of consecutive missing frame synchronization code before quitting in-frame state, which is used for avoiding the leaky synchronous phenomenon.

- T_{ASC}: The time between the moment the frame synchronization system begins to catch frame synchronization code when it finds a loss of the frame synchronous signal, to the moment frame synchronization system confirms it entered the synchronous state.

- T_{ASH}: In the lock mode, the interval during which the frame synchronization system keeps itself operating at synchronous state is called average synchronization holding period, the time corresponding to it is called average synchronization holding time.

2.5.2 K_1 and K_2 Parameters in the Synchronization Check and Protection Unit

A transmission channel error may corrupt a frame synchronization code so that it will be misidentified. Also, during a search operation a random combination of

information bits may corrupt the required frame synchronization code. Thus we need to consider strategies of frame synchronization check and protection. They will be implemented by the Synchronization Check and Protection(SCP) unit. K_1 and K_2 defined above are two parameters in SCP unit.

K_1 is set to avoid the false synchronous phenomenon to a certain extent. If valid framing patterns are detected in K_1 consecutive STM-1 frames by the synchronization checking counter in the SCP unit, the frame synchronization system will declare itself in synchronization and enters frame synchronization state. The receiver does not proceed before the K_1 consecutive frame synchronization codes are checked. This means that the larger K_1 is, the more the information lose since the receiver can not enter synchronization state sooner. Considering the analysis to the features in length and pattern of the frame synchronization code, we could choose $K_1 = 0$ for the frame synchronization system of SDH transmission network since the P_{FS} is very low (see Table 2.1). Thus performance analysis in the following section will not include the effect of K_1.

K_2 is set to avoid the leaky synchronous phenomenon. If invalid frame synchronization codes are counted at least K_2 consecutive STM-1 frames by the synchronization protection counter in the SCP unit, frame synchronization system will declare itself out of frame synchronization and begin the reframe process. T_{ASH} is closely related to the parameter K_2. We will analyze its effects in the subsections below.

2.5.3 Average Synchronous Catching Time T_{ASC}

2.5.3.1 Average Synchronous Incoming time T_{ASI}

We first consider a special case. In the process of searching frame synchronization, if the first byte of frame synchronization code being input exactly matches the position which is preset in detector to conform with the frame synchronization code, we say the detector enters incoming state of the frame synchronization process. The time arrived at this state is called synchronization incoming time T_{SI}. Since position of frame synchronization code input to the detector is random, T_{SI} is a random variable. We need to find its average value T_{ASI}.

In designing detector of traditional parallel mode, only when the first bit of frame synchronization code exactly occurs on the first bit position of the detector, the detector can match the frame synchronization code and indicate it to admit synchronization incoming state. However, input bit stream enters the detector randomly when the detector initializes searching frame synchronization code. This means that the first bit of frame synchronization code may occur on any bit position of the byte (8-bit) in the detector. Then, the probability that the first bit of the frame synchronization code takes up on the first bit of the first byte in the detector is $\frac{1}{8}$. It is also the probability that the detector could generate frame detection pulse. Otherwise the detector has to repeat searching frame synchronization code after approximate one frame time until the first bit of frame synchronization code exactly occurs on the

first bit position of the detector.

Thus, the average number of frames for which the detector has to wait after missing a frame synchronization code $\bar{n}$ is equal to

$$\begin{aligned} \bar{n} &= \sum_{l=0}^{8-1} l\frac{1}{8} \\ &= 3\frac{1}{2} \end{aligned} \tag{2.6}$$

The average synchronization incoming time of the traditional parallel mode T_{asi} is equal to three and a half frames.

In the proposed scheme, since we design a detecting array with 55-bit register and eight detectors, and use different connections from the traditional mode, after every byte is shifted into the register, the connections shown in Table 2.2 ensure that one of the eight detectors can detect frame synchronization code wherever its first bit falls during the 1^{st}-8^{th} bit position in the detector. This means that the probability that generates frame detection pulse is p_d, and $p_d = 1$ within the first byte of the detector. So the average number of frames that the detector has to wait after missing a frame synchronization code $\bar{N}$ equals

$$\begin{aligned} \bar{N} &= \sum_{l=0}^{1} lp_d \\ &= 1 \end{aligned} \tag{2.7}$$

The average synchronization incoming time of the proposed scheme T_{ASI} is equal to one frame of time. It is clear that our scheme to get into synchronization mode is faster than the traditional one.

2.5.3.2 T_{ASC}

Here we analyze the average synchronous catching time(T_{ASC}) of the parallel frame synchronization system. T_{ASC} is defined as the time between the moment frame synchronization system begins to catch frame synchronization code when it finds a loss of the frame synchronous signal, and the moment frame synchronization system confirms it entered the synchronous state.

As described in the previous sections, our catching process of frame synchronous signal is that once frame synchronization system finds one frame synchronization code it continues detecting others after waiting one frame time T_F. If the frame synchronization system fails to find the frame synchronization code during this period of time it will start the detection process once again after taking $T_W = 8 \times T$, where T_W is the width of one byte($T_W = \frac{1}{f_p}$). In one frame that contains M bytes, there are $M - N_f$ non-synchronous bytes where false synchronous possibility may occur. Here N_f represents the byte number of one frame synchronization code. Since there are eight detectors in the array and the maximum number of false synchronous codes is eight appeared in 2^{8N_f} combinations, the false synchronous probability P_{FS} is :

$$P_{FS} = \frac{8}{2^{8N_f}} \tag{2.8}$$

The average time $\bar{t}_1$ of shifting one byte after the synchronization is given by:

$$\begin{aligned} \bar{t}_1 &= (1 - P_{FS})T_W + P_{FS}(1 - P_{FS})(T_W + T_F) \\ &< +P_{ffs}^2(1 - P_{FS})(T_W + 2T_F) + \ldots\ldots \\ &= \sum_{i=0}^{\infty}(1 - P_{FS})T_W P_{FS}^i + \sum_{j=1}^{\infty}(1 - P_{FS})P_{FS}^j j T_F \end{aligned} \tag{2.9}$$

In (2.9) we neglected the delay caused by devices for the sake of simplicity. By using series summing method and the fact that $P_{FS} < 1$, we can rewrite equation (2.9) as below:

$$\bar{t}_1 = T_W + \frac{P_{FS}}{(1 - P_{FS})} T_F \tag{2.10}$$

Because of the feature of the frame synchronization code, no false synchronization code exits in $(N_f - 1)$ non-synchronous bytes. Detector recognizes frame synchronization pattern again after one byte time, i.e., the frame synchronization system stays for one byte time. We refer to this amount of time as average stay time $\bar{t}_2$, where,

$$\bar{t}_2 = T_W \tag{2.11}$$

Let t_3 represent the time for transferring from non-synchronous bytes to synchronous bytes. The worst case occurs when the beginning of the catching process exceeds seven bits or recedes one byte from FSC in bit stream, where the parallel frame synchronization system spends time of $(M - N_f)$ non-synchronous bytes. False synchronous phenomenon takes place and also spends time of $(N_f - 1)$ non-synchronous bytes in which no false synchronous code exits. In this case $t_3 = t_{3MAX}$. For non-synchronous bytes, in which no false synchronous code takes place, t_3 is equal to t_{3MIN}, i.e.:

$$t_{3MAX} = (M - N_f)\bar{t}_1 + (N_f - 1)\bar{t}_2 \tag{2.12}$$

$$t_{3MIN} = \bar{t}_2 \tag{2.13}$$

From formulae (2.12) and (2.13) we can get average value $\bar{t}_3$ of t_3:

$$\bar{t}_3 = \frac{t_{3MAX} + t_{3MIN}}{2} \tag{2.14}$$

thus:

$$\begin{aligned} \bar{t}_3 &= \frac{(M - N_f)(T_W + \frac{P_{FS}}{1-P_{FS}}T_F) + (N_f - 1)T_W + T_W}{2} \\ &= \frac{MT_W + \frac{P_{FS}}{1-P_{FS}}(M - N_f)T_F}{2} \end{aligned} \tag{2.15}$$

considering $MT_W = T_F$, therefore:

$$\bar{t}_3 = \frac{T_F}{2}[1 + \frac{P_{FS}}{1 - P_{FS}}(M - N_f)] \tag{2.16}$$

In fact, bit error in the channel causes FSC to change leading to the leaky synchronous phenomenon and prolonging catching time. FSS spends time of t_{3MAX} if the phenomenon happens with probability P_{LS}, otherwise it spends a time duration equal to $\bar{t}_3$ with $(1 - P_{LS})$. Therefore average synchronous catching time T_{ASC} is equal to:

$$\begin{aligned} T_{ASC} &= (1 - P_{LS})\bar{t}_3 + P_{LS}(1 - P_{LS})(\bar{t}_3 + t_{3MAX}) \\ &< +P_{LS}^2(1 - P_{LS})(\bar{t}_3 + 2t_{3MAX}) + \ldots\ldots \end{aligned} \tag{2.17}$$

By using the same formula of (2.10) we get:

$$T_{ASC} = \bar{t}_3 + \frac{P_{LS}}{1 - P_{LS}} t_{3MAX} \tag{2.18}$$

According to series expansion, considering $t_{3MAX} \gg t_{3MIN}$, replacing $\bar{t}_3$, t_{3MAX} by (2.15), and (2.12) respectively, T_{ASC} equals:

$$T_{ASC} \approx [1 + 2P_{LS} + (M - N_f)P_{FS}]\frac{T_F}{2} \tag{2.19}$$

In STM-1, $M = 2430$, $N_f = 6$. When $P_e = 10^{-7}$, equation (2.19) gives

$$T_{ASC} \approx \frac{125}{2} \times 10^{-6}(sec.) \tag{2.20}$$

It is observed that the frame synchronization system takes $T_{ASC} \approx \frac{125}{2} \times 10^{-6}(sec.)$ before entering the frame synchronous state. The first term in formula (2.19), $\frac{T_F}{2}$, assumes a PFSS initiates (on the average) at the mid of the frame. In fact, the false synchronous code will make T_{ASC} longer. If we compare this result of PFSS T_{ASC} to that of the conventional approaches we find that they are almost equal [55]. However, our proposed scheme, the PFSS, has an advantage that FSS can be implemented with off-the-shelf lower rate integrated circuit chips.

2.5.4 Average Synchronization Holding Time T_{ASH}

T_{ASH} is one of the most important parameters used for measuring performance of a frame synchronization system. It indicates how long the system stays in the synchronous state. It is known that only when the frame synchronization system operates in the synchronous state the receiver can correctly demultiplex payload of each user from data bit stream received. Therefore, the longer T_{ASH} is, the better the performance of the frame synchronization system.

Now we evaluate the value of T_{ASH}. Under the synchronous operation, a frame synchronization system periodly examines frame synchronization code. However, as mentioned before, a frame synchronization code may be corrupted by transmission

error so it can not be recognized on the expected position by the frame synchronization system. In the previous section, we defined the bit error probability p_e in a noisy transmission channel and the probability without bit error $1 - p_e$. Then the probability of correct transmission of the frame synchronization code of n-bit size is $(1 - p_e)^n$, and the probability that at least one error in the frame synchronization code occurs is $[1 - (1 - p_e)^n]$, the probability that the frame synchronization system fails to detect the frame synchronization code.

From the synchronization strategy of SDH system described above, frame synchronization system will declare itself out of frame synchronization state when it can not detect the frame synchronization code K_2 frames in succession. The corresponding probability is equal to $[1 - (1 - p_e)^n]^{K_2}$. The interval between two declarations of the loss frame synchronization state is the period in which the frame synchronization system operates regularly at synchronous state. The interval is also average synchronization holding time T_{ASH}. It is given as following:

$$T_{ASH} = \frac{T_F}{[1 - (1 - p_e)^n]^{K_2}} \tag{2.21}$$

When p_e is very small and n is large,

$$(1 - p_e)^n \approx 1 - np_e \tag{2.22}$$

By replacing $(1 - p_e)^n$ with $1 - np_e$, we obtain

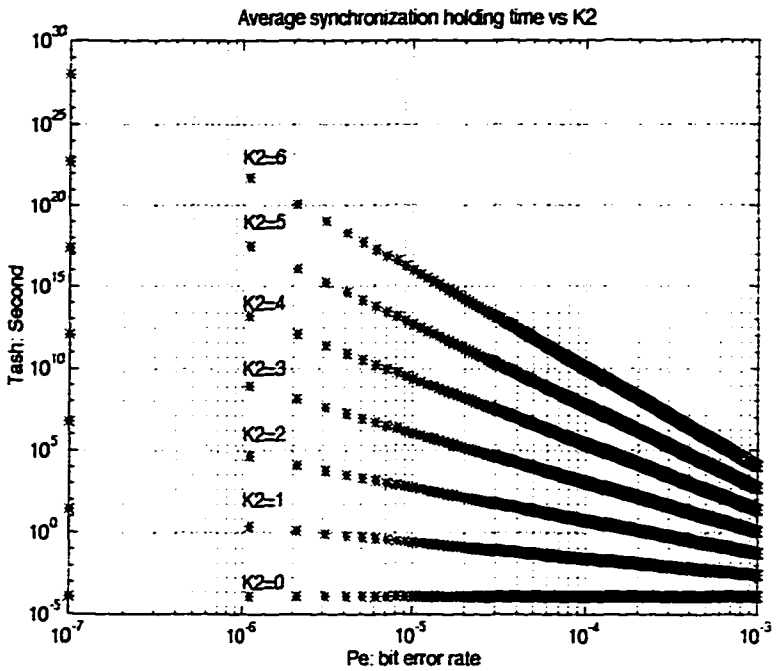

Figure 2.12: T_{ASH} curves vs K_2

$$T_{ASH} \approx \frac{T_F}{(np_e)^{K_2}} \tag{2.23}$$

A group of T_{ASH} curves corresponding to different p_e and K_2 values are shown in Figure 2.12.

From the curves we find:

1. When p_e is constant, T_{ASH} increases as K_2 increases. It is evident from the definition of K_2. However, K_2 can not be increased with no limits. A large K_2 requires increasing the capacity of counter. On the other hand, a very large K_2 may delay the start for state search when the system losts its synchronous

state due to other reasons. Selection of K_2 values for a system depends on the requirement of the telecommunication system. For example, if we require a system to keep synchronous state approximately thirty years under the condition where $p_e = 10^{-6}$, then we find that we need to choose $K_2 = 3$, see Figure 2.12

2. When K_2 is constant, T_{ASH} decreases as p_e increases.

Generally, we always decide K_2 value according to channel condition.

Chapter 3

PAYLOAD MULTIPLEXING

3.1 General Overview

Multiplexing is a popular method by which payloads from many terminals are simultaneously transmitted over the same transmission link. It can bridge the difference between terminal speed and transmission media speed. Over any given route, the most cost-effective transmission will, in general, be achieved by multiplexing as many channels together as possible. Because of the development of signal theory and the availability of efficient transmission techniques, there has been a tendency to combine different traditional multiplexing techniques with modern digital transmission techniques to gain greater multiplexing efficiency on a single transmission link.

There are two basic methods to classify multiplexing techniques. They are:

1. Frequency Division Multiplexing(FDM): In FDM a fraction of the carrier frequency is assigned to each signal so that different segments within the frequency

are occupied by the multiplexed signals at the same time. We use electrical filters to position the bands at the transmitting end and to separate the bands at the receiving end [73]. For fiber optic channels, a variation of FDM is used. It is called Wavelength Division Multiplexing, WDM.

2. Time Division Multiplexing(TDM): In TDM a fraction of the transmission time, called timeslot, is assigned to each signal so that different timeslots are occupied by the multiplexed signals. Each signal contained in each timeslot takes up the whole carrier bandwidth. We use multiplexers to position the timeslots at the transmitting end and demultiplexers to separate the signals at the receiving end [74]-[76].

We here briefly review the TDM techniques related to our research work.

3.1.1 TDM Techniques

Time division multiplexing is not limited to a fixed level. Based on the unit of the information multiplexed it is classified into three levels. A brief explanation for each level is described below.

1. Frame multiplexing: User signals are interleaved in a manner of frame by frame into time slots prearranged in the same carrier.

2. Byte multiplexing: User signals are interleaved in a manner of byte by byte into time slots prearranged in the same carrier.

3. Bit multiplexing: User signals are interleaved in a manner of bit by bit in turn in the same carrier.

Also time division multiplexing is classified as synchronous and asynchronous. Multiplexing is referred to as synchronous if the timeslots are distributed to each signal in turn in a regular sequence produced in the system, and it is referred to as asynchronous if the timeslots are distributed to each signal as demanded. Synchronous time division multiplexing combines multiple, lower speed digital signals into single, higher speed signal. It allocates a fixed timeslot to a fixed user. Even though a user has no signal to transmit his timeslot can not be used by others. This feature decides that the synchronous time division multiplexing is widely used in trunk links with heavy traffic and leads to the development of a class of multiplexing techniques called asynchronous or statistical time division multiplexing methods. The new idea is that timeslots are distributed to a user once it has data to be transmitted, otherwise no timeslot is allocated. Clearly, the multiplexer needs some overheads as identifiers in order for the receiver to restore the original data information.

3.1.2 Multiplexing Methods in PDH

The essential function of the multiplexers being recommended is to multiplex a number of lower level signals into a higher level one. In time division multiplexing system of PDH, there are two basic methods to multiplex to higher rate signals from lower rate tributary signals. They are shown in Figure 3.1 (a) and (b).

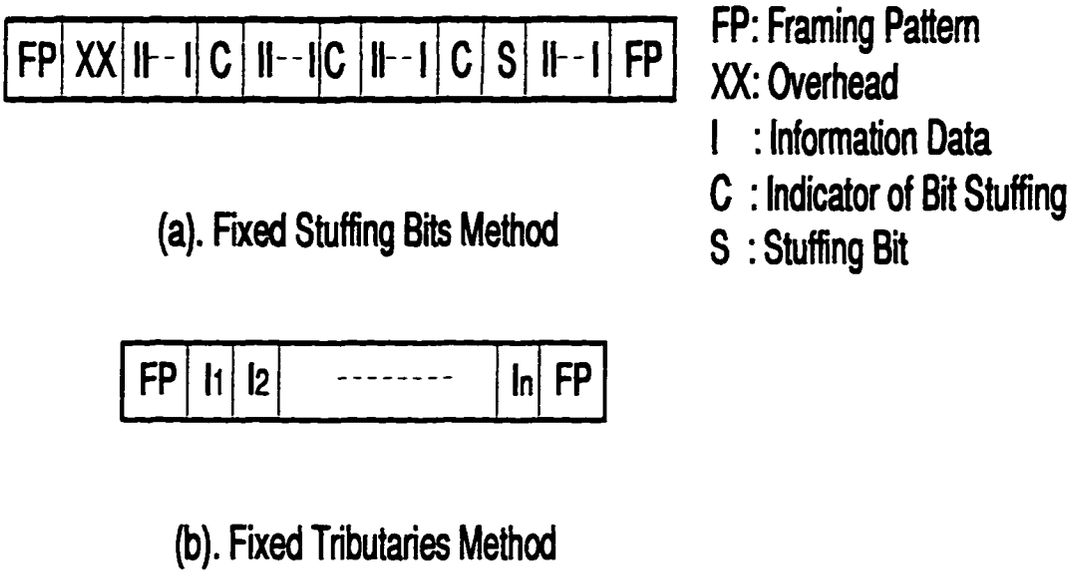

Figure 3.1: Multiplexing Methods of Payloads

Method (a) is to use stuffing bit to match the precise signaling rates of the tributaries to the signaling rate of the multiplexed signal. As bit stuffing indicators, C bits occupy fixed positions within a higher level frame and are used to indicate whether the stuffing bit S carries information data or dummy data for the tributary in the frame. Multiplexing of four DS1 signals into one DS2 signal and the multiplexing of seven DS2 signals into one DS3 are examples of method (a). Bit stuffing can accommodate large frequency variations of multiplexed payloads. However, access to those payloads from the higher level multiplexed signal is extremely difficult since before the tributary signal must first be de-stuffed, i.e., the information data bits should be separated from the dummy bits, the framing pattern of the payloads must be identified if complete payloads access is required.

In method (b) there is a fixed mapping position for each tributary when lower rate

tributaries are multiplexed into high rate signal, i.e., fixed location mapping uses specific bit positions in the higher level frame to carry lower rate synchronous signals. For example, I_1 always carries information data from one special tributary. Because de-stuffing becomes unnecessary this method is easy to access the special payloads. However, in order to repeat or delete a frame of information to correct frequency differences, multiplexing equipment interface has to place larger buffers to phase-align and slip the tributary signal since phase and frequency differences which are caused by synchronization network failure or at plesiochronous boundary. These buffers are undesirable because of the signal delay that they impose and the signal impairment that slipping causes.

3.2 Multiplexing in SDH

As mentioned at the beginning of Chapter 2, SDH transmission network uses synchronous time division multiplexing technique for transmitting payloads. It provides the most cost-effective transmission with powerful multiplexing functions. Its multiplexing hierarchy and the relationship between various containers are shown in Figure 3.2.

SDH defines a number of "containers", each corresponding to an existing plesiochronous rate and other new services. Information from a plesiochronous signal and new services is mapped into the various container. Each container has control information

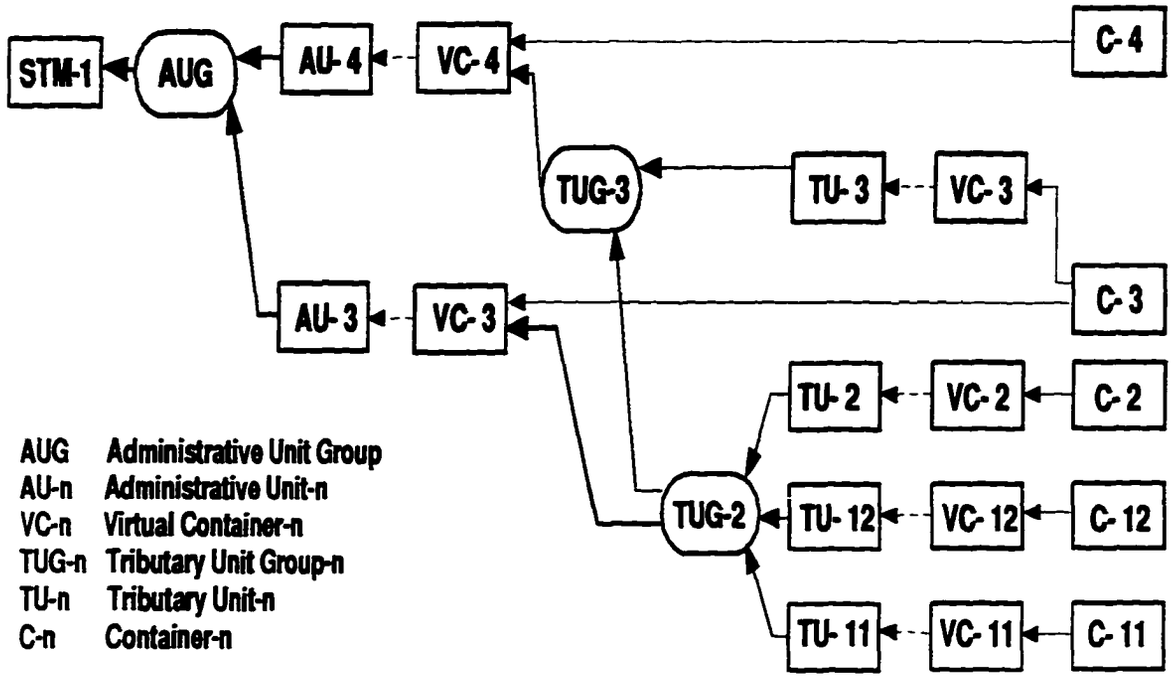

Figure 3.2: Basic Multiplexing Structure in SDH

known as the "path overhead(POH)". The POH bytes allow network operator to achieve end-path monitoring of things such as error rates. The container plus POH is called "Virtual Container(VC)". After review of some conventional multiplexing methods in the subsections below, we will introduce a concept of pointer in SDH, and then, based on the features we will present an implementation for one of the multiplexing structures in the STM-1 frame.

In order to overcome the disadvantages of the conventional multiplexing methods, SDH introduces the concept of pointer. In a synchronous network, all equipment is synchronized to an overall network clock. It should be noticed that the delay associated with a transmission link may vary slightly with time and cause a variation.

As a result, the location of virtual containers within an STM-1 frame may not be fixed, and the virtual containers are not synchronous with the STM-1 frame. These variations in frequency and phase between the payload and the STM-1 frame are accommodated by associating a pointer with VC each [77]. The position at which the virtual container starts within any one frame is given by the value of the pointer contained in the SOH of the STM-1 frame. It can be incremented or decremented as required in order to accommodate the position of the VC. The advantages of this scheme are that small variations in the data rate in the container can be accommodated by changing the pointer value, thus allowing the virtual container to move its position in the frame. For example, if the STM-1 payload data rate is high with respect to the STM-1 frame rate, the payload pointer is decremented by one and the H3 overhead byte is used to carry data for one frame. If the payload data rate is slow with respect to the STM-1 frame rate, the data byte immediately following the H3 byte is nulled for one frame and the pointer is incremented by one. Therefore, slips and their associated data loss are avoided. The phase of the STM-1 synchronous payload is known by reading the pointer value. The access to specific payloads from the higher level multiplexed signal is easy.

3.3 Multiplexing C-3 Payload

G. 709 defines different combinations of VC which can be used to fill up the payload area of the STM-1 frame. The process of loading containers and attaching overhead

is repeated at several levels in the SDH, resulting in the nesting of smaller VCs within larger ones. This process is repeated until the VC of the largest size, i.e. VC-4, is filled and eventually loaded into the payload of the STM-1. Containers of various size are used to carry payloads for extensive services. By introducing the concept of container, the frame structure becomes flexible to combine the two main current systems, i.e., 1.544 Mbits/s system and 2.048 Mbits/s system, efficient to multiplex tributaries to higher transmission levels, easy to carry ATM cells and to support a number of new services.

From among a variety of containers, one of the most frequently used containers in the STM-1 frame is the C-3 container. Each C-3 payload container can carry not just one Level 3 signal or multiple Level 2 signals of European and Northern America systems in Table 1.1, but also carry ATM cells. The basic multiplexing structure defined in SDH (Figure 3.2) allows two different methods for multiplexing C-3 payload, they are:

1. C-3 $\rightarrow VC-3 \rightarrow TU-3 \rightarrow TUG-3 \rightarrow VC-4 \rightarrow AU-4 \rightarrow AUG \rightarrow STM-1$;

2. C-3 $\rightarrow VC-3 \rightarrow AU-3 \rightarrow AUG \rightarrow STM-1$;

The direct multiplexing method, method 2, of C-3 signal is shown in Figure 3.3 and it will be the one discussed mostly through out this dissertation.

In method 2, POH is added to C-3 payload to form a virtual container VC-3. POH

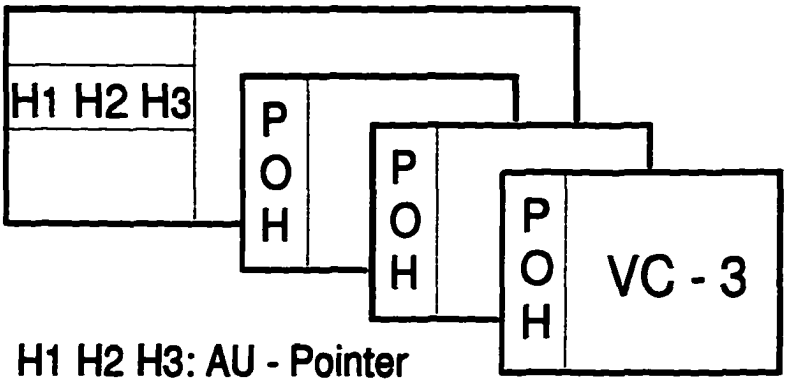

Figure 3.3: Direct Method for Multiplexing C-3

provides for integrity of communication between the point of assembly of a virtual container and its point of disassembly. An administrative unit AU-3 consists of VC-3 and an administrative unit pointer. This pointer is used to indicate the offset of the payload frame start relative to the multiplex section frame start. Three administrative units occupying fixed, defined positions in an STM-1 payload area form an administrative unit group AUG. This AUG, together with SOH, constructs an STM-1 frame.

In direct multiplexing method, three C-3 signals may be byte-interleaved and multiplexed together to form an STM-1 signal at 155.52 Mbits/s. Byte-interleaved multiplexing is accomplished by taking, in turn, one byte from the first C-3 signal for output, followed by one byte from the second C-3 signal for output, followed in turn by one byte from the third C-3 for output. At this point, the sequence is repeated by returning to the first C-3 signal to provide the next byte for output. Each row of the structure for multiplexing three C-3 signals is identical and is shown in Figure

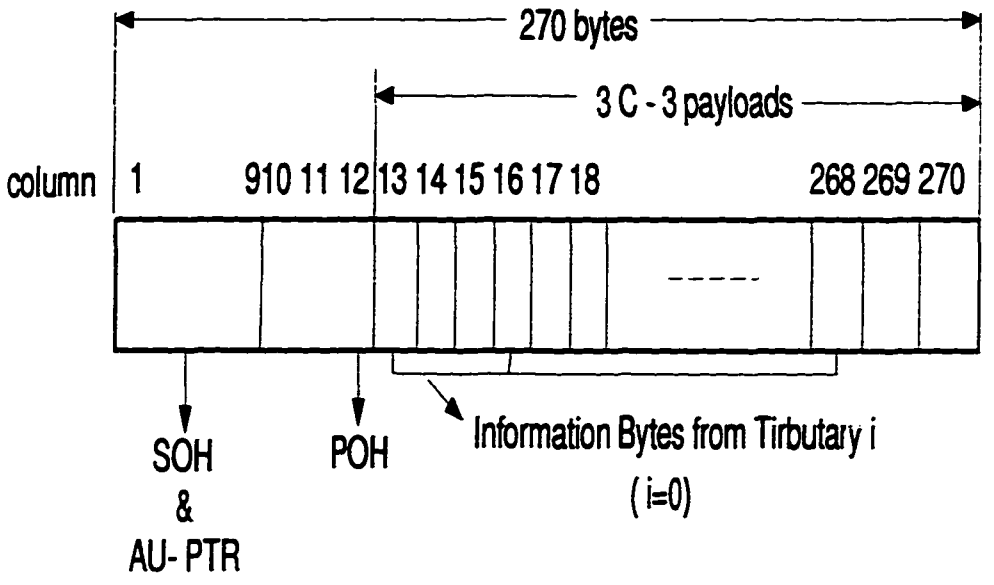

Figure 3.4: Row j in the Multiplexing Format of 3 C-3 Payloads

3.4.

Each C-3 container can carry user payload of 9 × 86 bytes in a single STM-1 frame. It operates at 49.536 Mbits/s. The multiplexed payloads can be:

1. CH1: Data from computer.

2. CH2: Voice signal, consisting of seven TUG-2 signals. Each TUG-2 signal can be used to carry three signals at rate of 2.048 Mbits/s, or one signal at 6.312 Mbits/s.

3. CH3: One 44.736 Mbits/s signal from North America Hierarchy or one 34.368 Mbits/s signal from European Hierarchy.

3.4 Buffer Multiplexing Method

In this section we present a buffer method for multiplexing three C-3 signals. Its diagram is shown in Figure 3.5. We assume that there are always user data arriving at the sender for transmission.

3.4.1 Matching Input and Output Rates

Figure 3.4 shows one row where three C-3 payloads are interleaved byte by byte, 86 bytes each. Each C-3 payload arrives at the inputs of multiplexer at 49.536 Mbits/s in serial. After conversion from serial to parallel format, the rate of the input data becomes:

$$r_{iw} = \frac{49.536}{8} = 6.192 Mbytes/s \tag{3.1}$$

Its width is $t_2 = \frac{1}{r_{iw}} \approx 161.5(nsec.)$.

The output rate r_{ow} is :

$$r_{ow} = \frac{155.52}{8} = 19.44 Mbytes/s \tag{3.2}$$

The width of each byte is approximately equal to 51.44 nsec. In order to correctly multiplex input signals what we need to do are two things. First, we should change

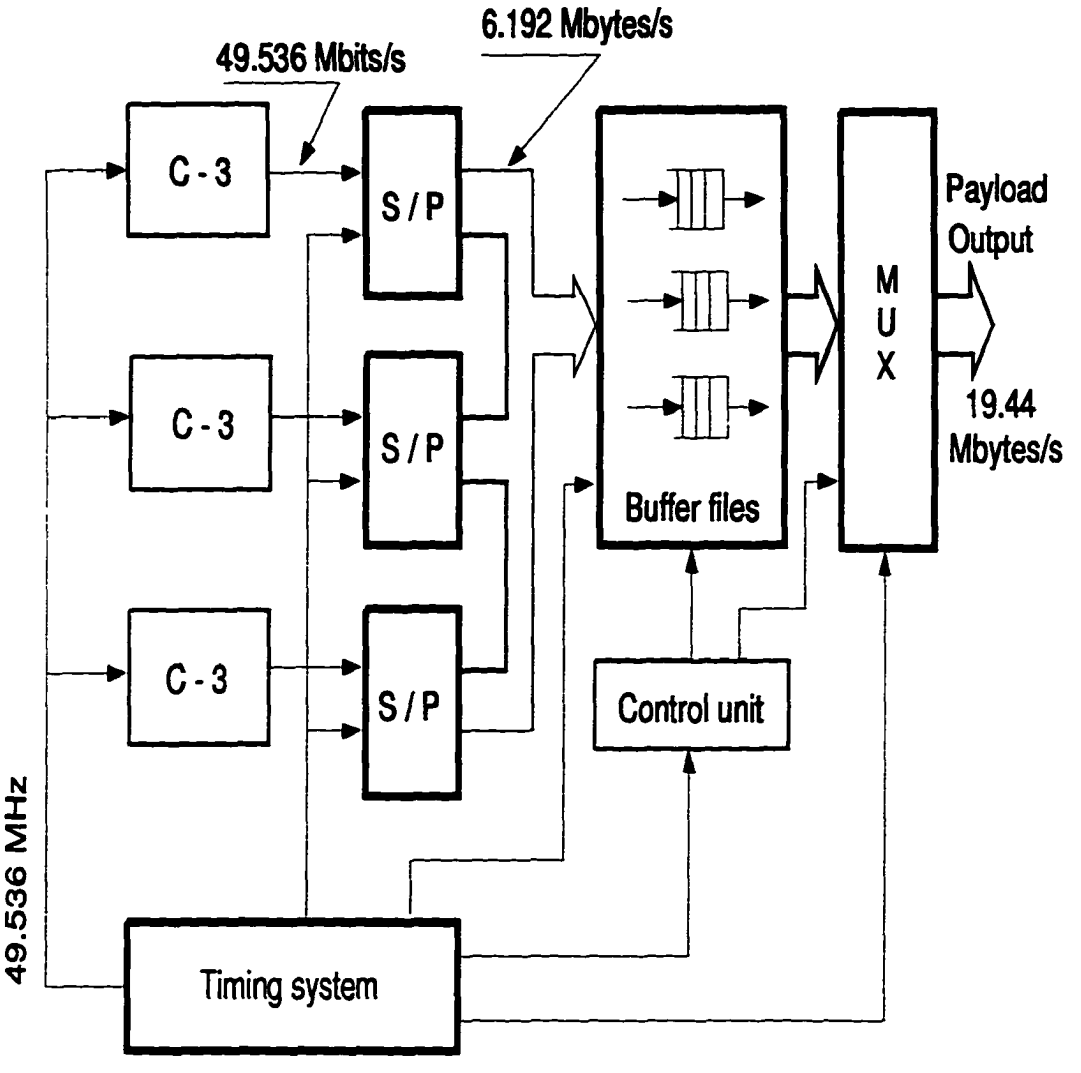

Figure 3.5: Multiplexer for 3 C-3 Payloads

information code rate from 6.192 Mbytes per second to 19.44 Mbytes per second. Second, we should avoid the phenomenon of read-empty. Since a container is mapped into a virtual container which contains overhead and stuff bytes, the read clock of payloads in the container is a gapped clock. Leaving "gaps" in the clock reduces frequency. Payloads with different rate within the SDH frame are timed using gapped clocks. In order to avoid loss of information in the gapped duration, we need to place a buffer in the multiplexer for temporary storage of each C-3 payload when overhead and stuff bytes are being read.

3.4.2 Calculation of Buffer Capacity

The key point is to evaluate the buffer capacity. We first evaluate buffer capacity for each of the C-3 channel, M. From Figure 3.4 we know that the first 12 bytes in each row of the STM-1 frame structure are used for SOH, AU-PTR, and POH. The positions of the i^{th} C-3 payload is located at $13+i$, $16+i$, ... , and $268+i$, respectively (where, i=0, 1, 2). The initial position of each C-3 channel is related to the first byte of the frame and it is nonuniform. Each C-3 signal is interleaved once every two bytes. Its interval is approximately 102.88 nsec. The maximum interval is 14 bytes which is the width from the first byte of the frame to the beginning byte of the third C-3 payload. Assume that T_{12+i} is the time at which the i^{th} payload starts to be multiplexed from the moment it arrives at the input end of the multiplexer. Then,

Table 3.1: The buffer capacity for the i^{th} C-3 signal

i	T_{12+i}	W_i	M_i
	(μsec.)	(bytes)	(bytes)
0	0.61728	3.82	$3 \prec M_1 \leq 4$
1	0.66872	4.14	$4 \prec M_2 \leq 5$
2	0.72016	4.46	$4 \prec M_3 \leq 5$

$$T_{12+i} = \frac{1}{r_{ow}} \times (12+i)\mu sec. \tag{3.3}$$

Let the number of information bytes transmitted during T_{12+i} be W_i. A user transmits its information bits at a rate r_{C-3}, where,

$$W_i = \frac{r_{C-3} \times T_{12+i}}{8} \tag{3.4}$$

It is observed that we could avoid the phenomenon of read-empty in the buffer if $M_i \geq W_i$, where M_i is the capacity of the buffer.

Using formulae (3.3) and (3.4), we have obtained Table 3.1 that contains the buffer capacity in the i^{th} C-3 channel for $r_{ow} = 19.44$ Mbytes per second and $r_{C-3} = 49.536$ Mbits/s.

In Table 3.1, W_i is a fractional number because, the ratio α of line transmission rate

$r_L = 155.520$ Mbits/s to payload input rate r_{C-3} is not equal to the whole number, where

$$\alpha = \frac{r_L}{r_{C-3}} = \frac{155.520}{49.536} \approx 3.13 \tag{3.5}$$

It is important to mention that the non-integer relationship makes it more complex to design the timing system for STM-1.

In theory, it is sufficient to make buffer capacity equal to W_i. In fact, we know that the buffer capacity should be an integer greater than W_i. This is because, the smallest unit of buffer capacity is a bit. Therefore, the buffer capacity for each C-3, denoted by M_i, is

$$M_i = \lceil W_i \rceil \tag{3.6}$$

Where $\lceil x \rceil$ means the smallest integer which is greater than or equal to x.

The selection of the buffer capacity, M_i, is related to implementation complexity of the system. For example, in order to use smallest buffer, it is sufficient to let $M_i = 5$. The buffer access could be performed by a divide-by-5 circuit. The problem with the preceding approach is that the circuit has to rotate 18 times to generate 86 byte pulses($18 \times 5 = 90$: it is not enough to rotate 17 times($17 \times 5 = 85$)). We know that the timing circuits need to generate 86 byte pulses for interlacing 86 of 3 C-3 signals

within each row of the frame. Therefore, we have to modify the divide-by-5 circuitry to eliminate 4 extra pulses.

In this chapter, we have presented a new method for multiplexing payloads in SDH networks. In particular, we have formulated and developed a multiplexing scheme for C-3 type of payload. Our scheme is based on the use of appropriate size buffers in order to avoid information loss due to gapped clock. We have also performed calculations to determine the minimal buffer size for various user transmission rates. The computations were done for C-3 type of payload, however, similar calculations could be performed to determine buffer sizes for other SDH containers. We believe that the scheme presented here is an efficient solution for multiplexing a variety of SDH containers.

Chapter 4

ERROR BLOCK ESTIMATION IN PAYLOADS

4.1 Block Error Rate (BLER)

In order to ensure the reliable and correct information transmission, a communication network generally use some techniques to detect errors which are impossible to eliminate completely in the transmission processing. The simplest detecting error method is to add an extra bit at the end of each wordcode. This extra bit is referred to as a parity-check bit and is chosen to make the number of 1's in each wordcode an even or odd number. This detecting technique is often applied for digital computer and communication systems in which the error probability of a bit is very low.

In the present SDH networks, optical fiber is used as transmission medium. However, although optical fiber has low error bit rate, errors maybe occur in equipment due to the hardware malfunction, imperfections in component design, etc. There are many techniques [50] [78] [79] that can be used to measure errors which happen in the

Table 4.1: Block size of virtual containers in STM-1 structure

VC type	No. of bits in a block	m, n
VC-11	832	m=416, n=2
VC-12	1120	m=560, n=2
VC-2	3424	m=1712, n=2
VC-3	6120	m=765, n=8
VC-4	18792	m=2349, n=8
STM-1	19224	m= 801, n=24

transmission processing. Communication networks error rates are measured with a simple formula called the bit error rate (BER). It is calculated as follows:

$$BER = \frac{errored\ bits\ received}{total\ bits\ sent}$$

Another useful statistics is called the block error rate (BLER) which defines the number of blocks sent in relation to the number of blocks received in error. The term block is generic, it has different forms corresponding to various applications. In the SDH network a block refers to a virtual container.

Table 4.1 shows block size of the different virtual containers in the STM-1 frame structure.

The formula for calculating BLER is:

$$BLER = \frac{errored\ blocks\ received}{total\ blocks\ sent}$$

An errored block is defined as a block in which at least one bit associated with the block is corrupted, therefore the block errored ratio (BLER) represents the probability of having an errored block. It is clear that the BLER is related to bit error rate. To measure the probability of errored block occurred in the SDH network ITU-T Recommendation G.826 gives an expression of BLER as follows [80]:

$$BLER = 1 - \frac{1}{e^{mnp}} \tag{4.1}$$

Where m is the number of columns in the block, n is the number of rows in the block, and p is the bit error rate, i.e., BER. BLER describes the probability that the received blocks are in error.

4.2 Bit Interleaved Parity (BIP)

The detection of errored blocks is a key point in the SDH network . Bit Interleaved Parity (BIP) code is recommended by ITU-T for error monitoring in the SDH network [80]. In the STM-1 frame structure of the SDH network, there are three types of BIP codes used for error monitoring. They are regenerator section BIP-8 code, multiplex section BIP-24 code and path BIP-8 code, respectively.

4.2.1 The Functions of BIP in STM-1 Frame

1. BIP-8

   One byte, B1, provides regenerator section error monitoring by means of a Bit Interleaved Parity code (BIP-8) using even parity in the STM-1 frame. The B1 byte is located in row 2 and column 1 of the STM-1 frame. By B1 the SDH network performs the even parity check on the previously sent STM-1 frame. The method of calculating parity is that, for the previously sent STM-1 frame after scrambling, the number of "0" or "1" located at the n^{th} bit position is evaluated using modulo 2 for each byte over the whole STM-1 frame. The calculated result, which is 0 for even number and 1 for odd, is stored in the n^{th} bit position of B1 byte in the current frame before scrambling. Therefore, 8 independent parity calculations are operated at 8 adjacent bit positions in B1 byte.

2. BIP-24

   Three bytes, B2B2B2, provide a multiplex section error monitoring function. This function is a Bit Interleaved Parity code (BIP-24) using even parity. The BIP-24 is evaluated over all bits of the MSOH and payload envelope capacity of the previous STM-1 frame except for the first three rows of SOH. The calculated result is stored in the B2B2B2 bytes before scrambling.

3. Path BIP-8

One byte, B3, provides a path error monitoring function in each VC-3 and VC-4. Its function is the same as that of the regenerator section and multiplex section, to perform a BIP-8 path parity check using even parity. The path BIP-8 is evaluated over all bits of the previous VC-3, VC-4 OR VC-4-Xc before scrambling. The calculated result is stored in the B3 byte of the current VC-3, VC-4 OR VC-4-Xc before scrambling.

4.2.2 The Algorithm of BIP in STM-1 Frame

As we see, BIP-N ($N = 8$ or $N = 24$) code is used for error monitoring. A monitored partition comprises all bits which are in the same bit position within the N-bit sequences in the covered portion of the signal. The covered portion includes the BIP-N. The matrix below represents an input sequence ($a_{ij}, i = 1, 2, \cdots, n; j = 1, 2, \cdots, m$) with BIP-N code.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & \cdots & a_{1,m} & c_1 \\ a_{2,1} & a_{2,2} & \cdots & a_{2,m} & c_2 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ a_{i,1} & a_{i,2} & \cdots & a_{i,m} & c_i \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ a_{n,1} & a_{n,2} & \cdots & a_{n,m} & c_n \end{pmatrix}$$

The algorithm is that the first bit of BIP-N code , c_1, gives even parity over the first bit of all N-bit sequences, $(a_{11}a_{12}\cdots a_{1m})$, in the covered portion of the signal. The second bit, c_2, gives even parity over the second bit of all N-bit sequences, $(a_{21}a_{22}\cdots a_{2m})$, within the specified portion, and so on. The code $(c_1c_2\cdots c_n)$ will be filled up the position of BIP-N in the next frame.

The parity bit c_i is chosen such that the total number of 1's in each transmitted code word (including the parity bit) is even. The single parity check bit c_i is given by:

$$c_i = a_{i,1} + a_{i,2} + \cdots + a_{i,m} \tag{4.2}$$

where addition is based on modulo-2.

For example, VC-3 consists of C-3 container and path overhead. Byte B3 in the path overhead performs a BIP-8 path parity check to the previous VC-3 using even parity. $N = 8$ means the VC-3 is divided into 765 sequences, each of which is 8-bit long. Then the relative matrix is

$$\begin{pmatrix} a_{1,1} & a_{1,2} & \cdots & a_{1,765} & c_1 \\ a_{2,1} & a_{2,2} & \cdots & a_{2,765} & c_2 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ a_{i,1} & a_{i,2} & \cdots & a_{i,765} & c_i \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ a_{8,1} & a_{8,2} & \cdots & a_{8,765} & c_8 \end{pmatrix}$$

At the receiver, the error detection system determines whether one or more transmission errors have occurred by counting the number of 1's received in each block and determining whether the result is odd or not. That is, the receiver will recalculate the parity bit c_i. If there exists any difference between the calculated value and the received bit the receiver declares that errors occurred. When error number is odd the received block is corrupted during the transmission. When error number is even the received block will be accepted as one valid block. However, the BIP code can not detect errors of even number. In most situations we need to know the probability of having an errored block when undetectable errors happen. In the next section below, we will estimate BIP code performance with Bernoulli error distribution in the SDH network.

4.3 Probability of Undetected Errors in BIP

In order to estimate the block errored ratio we need to find probability of undetected errors first.

Assume that a M-bit long code is transmitted over a channel in which the probability of a bit error is p and bit errors are independent, and there are k random error bits in a row of the block. Then the probability of k bits in error p(k) is:

$$p(k) = \begin{pmatrix} M \\ k \end{pmatrix} p^k (1-p)^{M-k} \tag{4.3}$$

When the number of error bits is even, the probability related to it is $P\{k = even\}$, and

$$P\{k = even\} = p(0) + p(2) + \cdots + p(2i) + \cdots \tag{4.4}$$

When the number of error bits is odd, the probability related to it is $P\{k = odd\}$, and

$$P\{k = odd\} = p(1) + p(3) + \cdots + p(2i+1) + \cdots \tag{4.5}$$

where $i = 0, 1, 2, \cdots$.

Assume that $P_{undetected}$ is the probability of undetected even errors, it is clear that $P_{undetected}$ equals

$$P_{undetected} = p(2) + p(4) + \cdots + p(2i) + \cdots \tag{4.6}$$

where $i = 1, 2, \cdots$.

On the other hand, from Binomial Theorem, we know if l is a positive integer, then

$$
\begin{aligned}
(a+b)^l &= b^l + lab^{l-1} + \frac{l(l-1)}{2!}a^2b^{l-2} + \frac{l(l-1)(l-2)}{3!}a^3b^{l-3} \\
&\quad + \cdots + a^l \\
&= \sum_{k=0}^{l} \binom{l}{k} a^k b^{l-k}
\end{aligned} \tag{4.7}
$$

$$
\begin{aligned}
(a-b)^l &= (-b)^l + la(-b)^{l-1} + \frac{l(l-1)}{2!}a^2(-b)^{l-2} + \frac{l(l-1)(l-2)}{3!}a^3(-b)^{l-3} \\
&\quad + \cdots + a^l \\
&= \sum_{k=0}^{l} \binom{l}{k} (-1)^{l-k} a^k b^{l-k}
\end{aligned} \tag{4.8}
$$

Add Equation (4.7) and (4.8) when l is equal to even number, then

$$
(a+b)^l + (a-b)^l = 2\sum_{k=0}^{\frac{l}{2}} \binom{l}{2k} a^{2k} b^{l-2k} \tag{4.9}
$$

Simplify Equation (4.9) using $a = p$, $b = 1-p$ and let $l = m$ then

$$
\begin{aligned}
1 + (2p-1)^m &= 2\sum_{k=0}^{\frac{m}{2}} \binom{m}{2k} p^{2k}(1-p)^{m-2k} \\
&= 2(1-p)^m + 2\sum_{k=1}^{\frac{m}{2}} \binom{m}{2k} p^{2k}(1-p)^{m-2k}
\end{aligned} \tag{4.10}
$$

From (4.6) we know the second term in (4.10) exactly equals $P_{undetected}$, thus we get

$$1 + (2p-1)^m = 2P_{undetected} + 2(1-p)^m \tag{4.11}$$

then

$$P_{undetected} = \frac{1 + (2p-1)^m - 2(1-p)^m}{2} \tag{4.12}$$

where $(2p-1)^m = (1-2p)^m$ since m is even number thus (4.12) can be written as

$$P_{undetected} = \frac{1 + (1-2p)^m - 2(1-p)^m}{2} \tag{4.13}$$

Subtract Equation (4.8) from (4.7) and repeat the process above when l is equal to odd number, then

$$P_{undetected} = \frac{1 - (2p-1)^m - 2(1-p)^m}{2} \tag{4.14}$$

also (4.14) can be written as

$$\begin{aligned} P_{undetected} &= \frac{1 - (-1)^m(1-2p)^m - 2(1-p)^m}{2} \\ &= \frac{1 + (1-2p)^m - 2(1-p)^m}{2} \end{aligned} \tag{4.15}$$

where $1-(-1)^m(1-2p)^m = 1+(1-2p)^m$ since m is odd number.

Equations (4.12) and (4.15) indicate $P_{undetected}$ has the fixed expression either m is even or odd number.

4.4 Estimating Errored Block

We know that errors in a channel are distributed randomly. Assume probability of detectable errors in n rows of the whole block is $P_{detected}$, then

$$P_{detected} = 1-(P_{undetected})^n \tag{4.16}$$

By amending Equation (4.1) using the probability $P_{detected}$ we get $BLER_a$, an estimation of BLER:

$$BLER_a = P_{detected}BLER = (1-P^n_{undetected})(1-\frac{1}{e^{mnp}}) \tag{4.17}$$

Substituting Equation (4.12) for $P_{undetected}$, then

$$BLER_a = \{1-[\frac{1+(2p-1)^m-2(1-p)^m}{2}]^n\}(1-\frac{1}{e^{mnp}}) \tag{4.18}$$

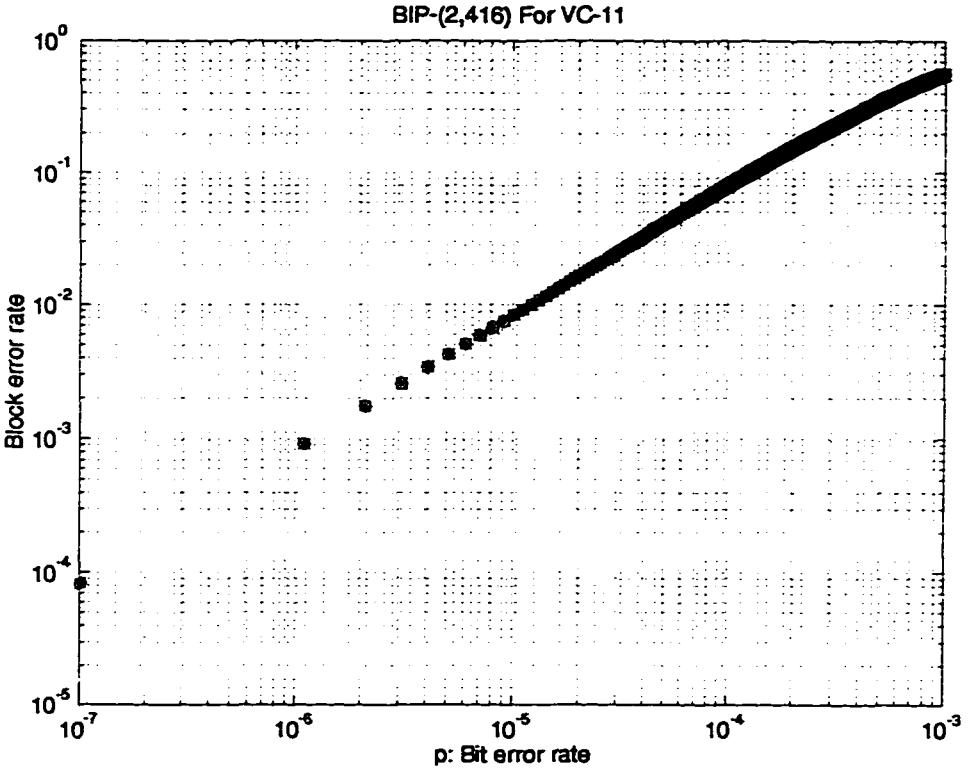

Figure 4.1: BLER of VC-11

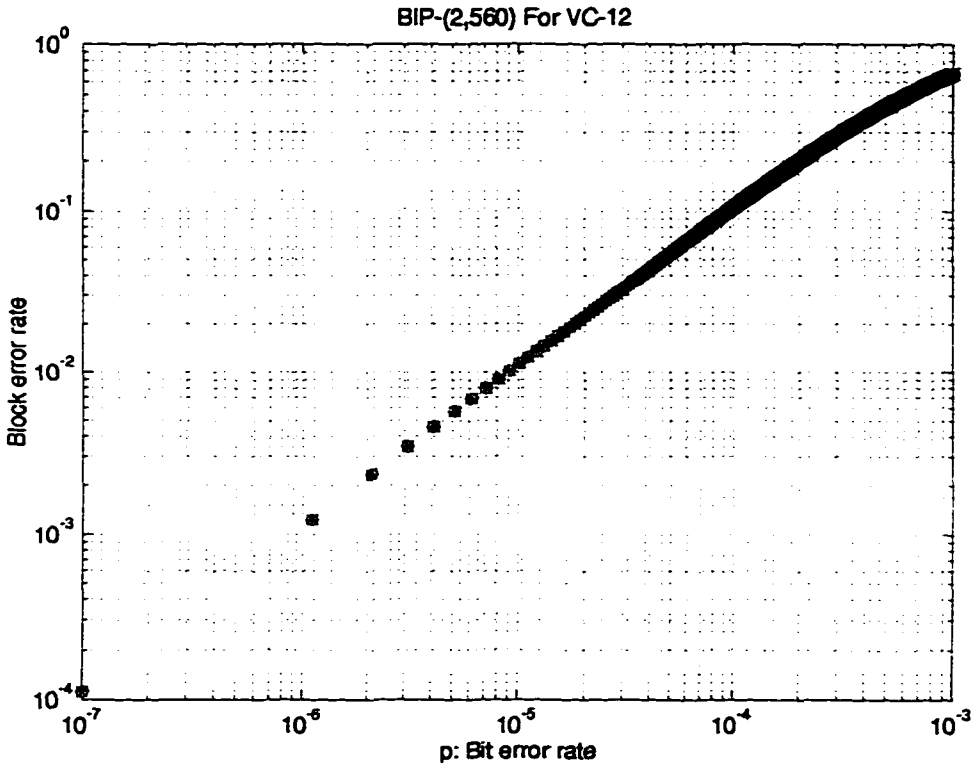

Figure 4.2: BLER of VC-12

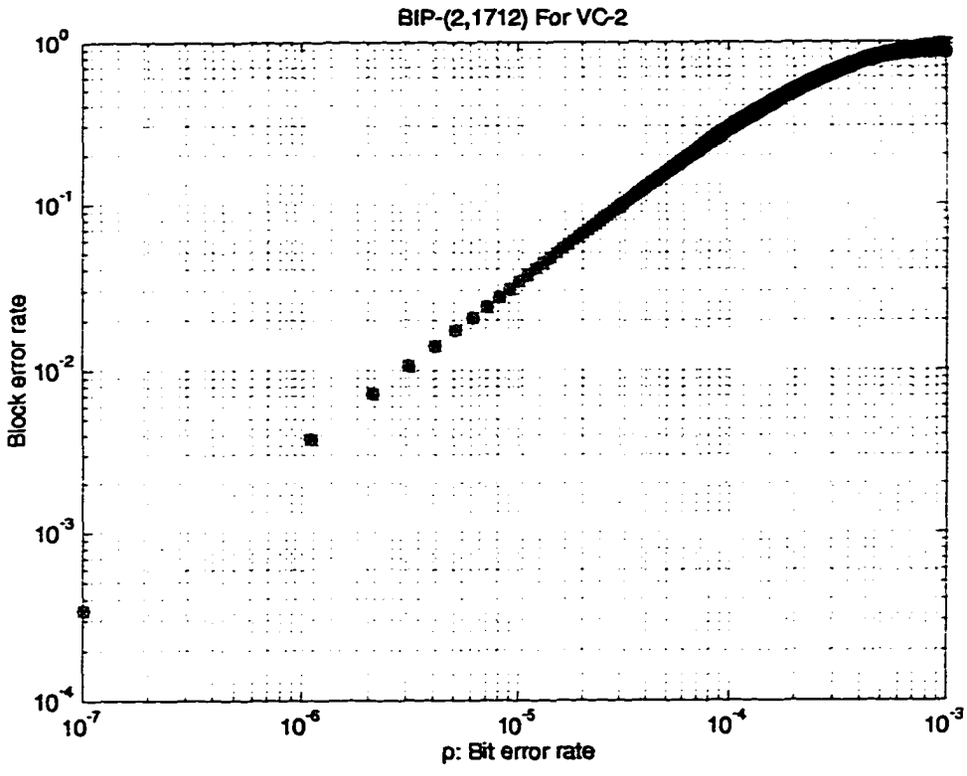

Figure 4.3: BLER of VC-2

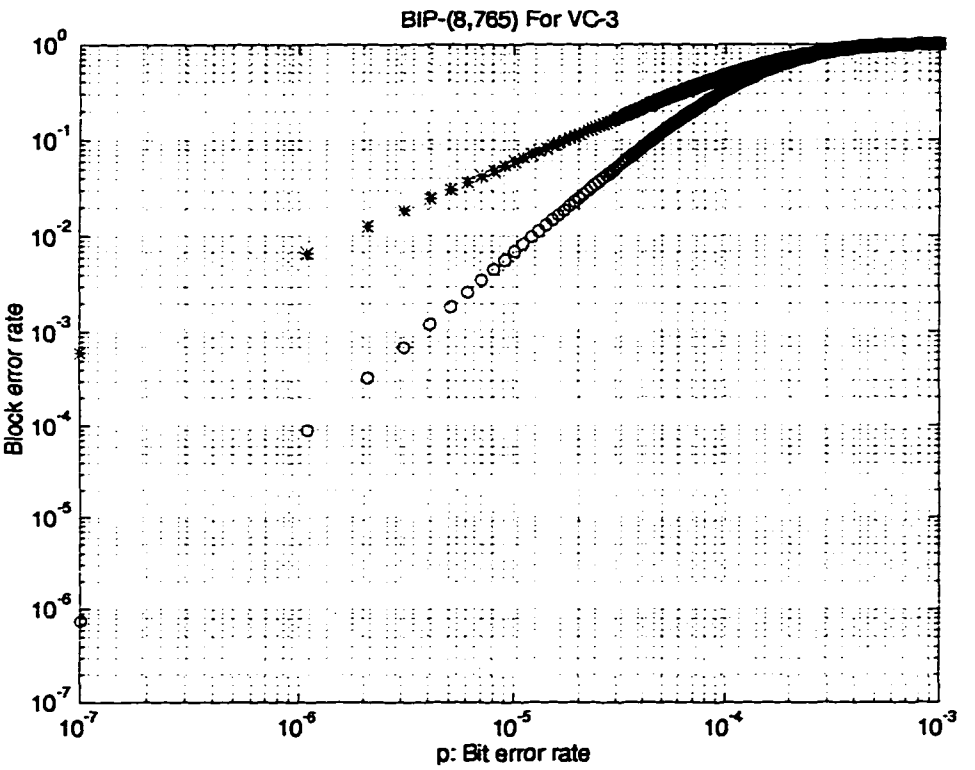

Figure 4.4: BLER of VC-3

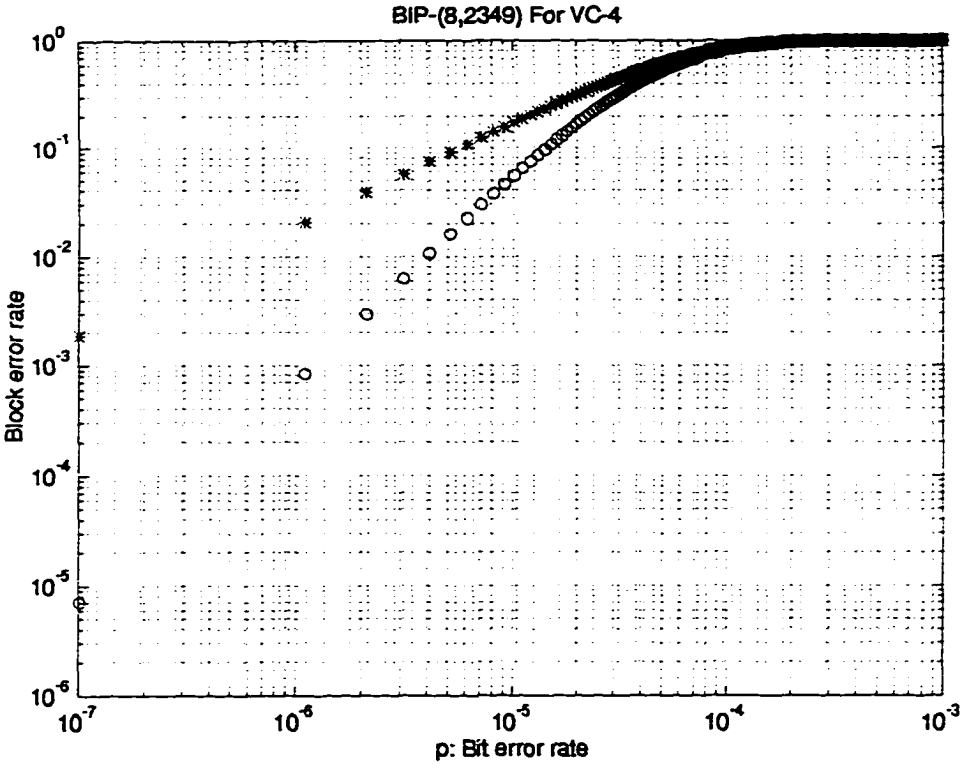

Figure 4.5: BLER of VC-4

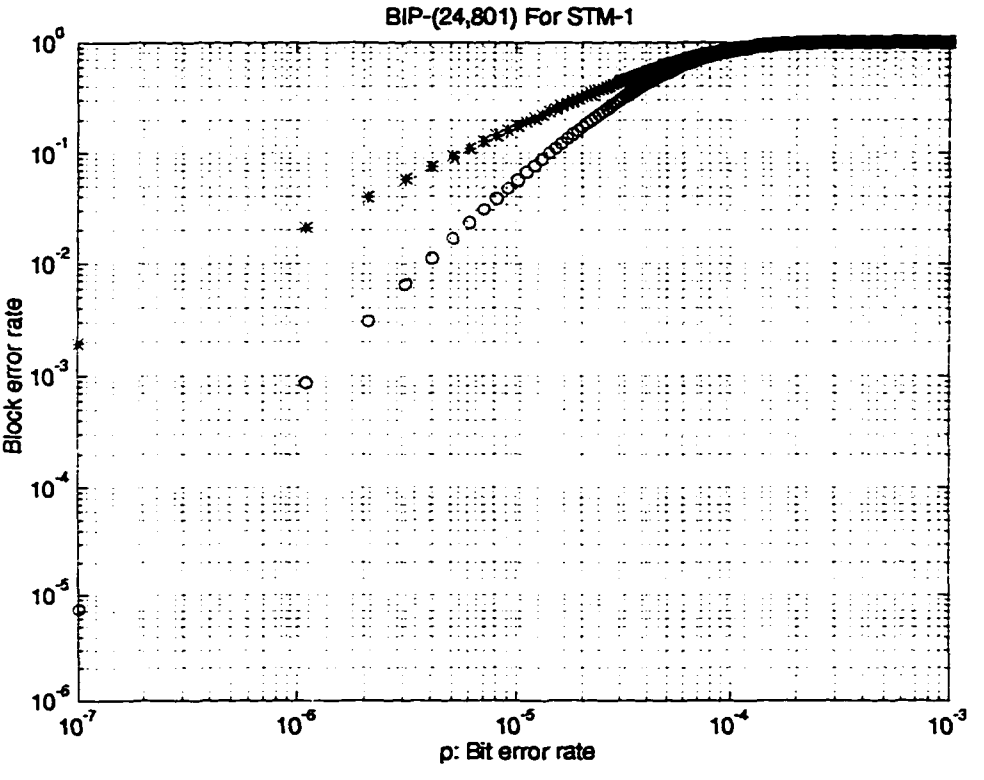

Figure 4.6: BLER of STM-1

For various values of p, m and n we obtain a group of curves shown as Figures 4.1 – 4.6 in which the asterisk " * " symbolizes theoretical values of BLER from formula (4.1), the circle " o " does the detectable ones from formula (4.17).

4.5 Numerical Results

By analyzing the curves given in the section above, we find:

1. It is self-evident that block error rates, either theoretical or detected, of virtual containers with different sizes are increased as bit error rate p increases.

2. For fixed bit error rate p, the bigger the size of virtual container, the higher the block error rate.

3. When the size of virtual container is smaller, the theoretical and detected block error rates in the same virtual container are about the same between $p = 10^{-7}$ and $p = 10^{-3}$. It indicates that formula (4.1) is more suitable for describing block errored ratio of the virtual containers with smaller size. When the size is larger, which means n is larger, detected block error rate is lower than theoretical one below $p = 10^{-4}$. It indicates that the performance of BIP-N's monitoring error is better if N is larger. This matches with practical value.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this dissertation, we have studied research on the three basic aspects of SDH transmission network. These are: frame synchronization system, payload multiplexing and error block estimation.

First, we presented a new parallel scheme realizing 155.520 Mbytes/s frame synchronization system. The scheme improves the conventional detector of frame synchronization code. It allows processing in SDH system to be performed at 19.44 MHz. This ensures that all operations are byte operation after the framer. The functions that follow the framer include discramble, section overhead monitoring, pointer processing, etc. It gets the wider frame synchronous detective pulse, provides consequent circuits with sufficient processing time and accesses data bytes directly from the Detector. The result suggests that the circuit design requirements for a FSS in STM-1

can be relaxed and some high speed system be realized with lower rate integrated circuits. The performance analysis indicates that the scheme has the advantage to quickly synchronize the incoming frame, and that some cases its performance is better than that of the traditional approaches under the some condition. Although the improvement in channel detection is obtained here at the expense of slightly higher circuit complexity, it is worth as the integrated circuits cost is remarkably decreased. We expect that this scheme will be useful for further research in SDH's technology.

Secondly, we proposed a new method for multiplexing payloads in SDH networks. In particular, we have formulated and developed a multiplexing scheme for C-3 type of payload. Our scheme is based on the use of appropriate size buffers in order to avoid information loss due to gapped clock. We have also performed calculations to determine the minimal buffer size for C-3 user transmission rate. The computations were done for C-3 type of payload, however, similar calculations could be performed to determine buffer sizes for other SDH containers. We believe that the scheme presented here is an efficient solution for multiplexing a variety of SDH containers.

Thirdly, we found a closed-form expression for the undetected error probability by applying Binomial Theorem when even parity is used for detecting transmission errors. We calculated the theoretical and measured values of block error rate according to the formulae recommended by ITU-T and amended by us. It is found that when the size of virtual container is small, the theoretical and detected block error rates in the same virtual container are about the same between $p = 10^{-7}$ and $p = 10^{-3}$.

It indicates that formula (4.1) is more suitable for describing block error ratio of the virtual containers with smaller size. When the size is large, which means n is large, the detected block error rate becomes lower than theoretical value. It indicates that the performance of BIP-N's monitoring error is better if N is larger. This result is in agreement with practical cases.

5.2 Future Work

So far we theoretically presented a parallel frame synchronization scheme and analyzed its performance. In the next phase we will try to seek cooperation from industry to implement the scheme.

Based on the calculating method proposed in this dissertation, we will continue to find buffer capacity for the other containers and expand it to dynamic case.

Also, we want to estimate error block rate under more complex probability distribution functions.

Furthermore, we intend to apply our scheme to wireless communication networks. Wireless broadband systems, which can accommodate data rates ranging between 2 Mbits/s to 155 Mbits/s [82], are emerging rapidly. Wireless access systems have gained extensive acceptance for mobile and fixed narrowband communications [83]. Demand for wide area networks with high speed is growing, the future wireless broadband networks will be able to carry ATM cells and multimedia traffic [84] [85]. In

these systems, terminals can be mobile-moving while communicating, or portable-static while communicating, the bandwidth may be fixed, or dynamically allocated depending on the user demands. For a number of years, the extension of mobile systems to broader bandwidths and a richer variety of services than messaging, paging, voice, and low-bit-rate data have been explored in activities around the world. Future telecommunication networks will combine terra firma and satellite, wire and wireless into one integrated network, so it is beneficial to study interface between wire and wireless communications based on the SDH network.

Broadband communications is the central enabling technology for the well publicized information superhighway, which apart from being seen as the key to economic prosperity, promises to profoundly change the way we work and play. The development of the SDH in the ITU-T has been one of the significant events in the telecommunication industry in this century and will continue in the next century. We expect more people to get involved in the research activities related to it and promote its growth.

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