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Parallel ultrafast digital optical computations

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PARALLEL ULTRAFAST DIGITAL OPTICAL COMPUTATIONS

by

YAO LI

A dissertation submitted to the Graduate Faculty in Engineering in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York.

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ABSTRACT

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by

Yao Li

Advisors: Prof. G. Eichmann and Prof. R. R. Alfano.

New methods to implement optical digital computation elements and processors are studied in this thesis. Various ultrafast nonlinear optical effects, such as Kerr, phase conjugation, second harmonic generation processes are used for optical computation. The ultrafast Sagnac interferometric logic switches which have a better mechanical stability over other two beam interferometric switching geometries are described. Using a variety of these switches, various binary and multiple-valued optical logic elements is detailed. As an alternative optical logic implementation technique, an optical phase conjugation pattern logic method is proposed and demonstrated. The major advantage of this type of optical logic elements together with a transparent/opaque logic code is it can perform all sixteen two-input Boolean logic functions. Using a polarization encoding methods, optical implementation of multiple-input binary as well as multiple-valued logic operations are also studied.

In this thesis, the implementation of ultrafast optical inteconnection devices, i.e. an optical sampler, an A/D converter, a dynamic cross-bar, as well as various generalized perfect shuffles, is also described. Most of the proposed schemes uses a parallel processing geometry. Using a Sagnac interferometric sampler, the sampling frequency can be doubled with respect to other existing sampling geometry. With the theta-modulation-based optical A/D converter, a fast (subnanosecond), compact and flexible A/D conversion can be performed. Compared to other existing parallel data shuffling geometries, the implementation methods described in this thesis are more compact and efficient. Using the proposed phase-conjugation-based dynamic cross-bar, the parallel interconnection speed has been increased from microsecond to picosecond region.

In this thesis, for the optical numerical computation, various binary and non-binary computing structures are also investigated. In the binary case, using a number of cascaded Sagnac interferometers, optical implementation of a full adder and an array multiplier are studied. Using a combination of the digital multiplication via analog convolution algorithm and the ultrafast noncollinear second harmonic generation effect, a number of ultrafast data convolution pre-processing techniques are proposed. The proposed methods are generally suitable for ultrafast pre-processing involving scalar, vector and matrix multiplication operations. In the non-binary optical numerical processing case, a number of new processing methods are also presented. Using the Sagnac interferometer-based approach, the optical binary coded ternary adders are implemented. Based on residue arithmetic, using optical second harmonic generators, a number of ultrafast optical residue computing structures are described. Finally, a new approach to implement a content-addressable memory-based modified sign-digit addition and subtraction elements are detailed.

To My Wife Hong-Bing and Son Calvin.

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I. INTRODUCTION

1.1, Thesis Statement And Organization

In this thesis I have studied a number of important optical computing engineering problems and applications. The focus of the research has be on the implementation of ultrafast optical logic, arithmetic and interconnect elements needed for optical digital computation. For this purpose, I have studied a number of ultrafast nonlinear optical effects and various optical parallel processing concepts. Based on my research, I have proposed and experimentally demonstrated various new and efficient methods to implement various optical logic, symbolic, arithmetic and interconnection processors. The use of these new processing techniques may lead to the future realization of powerful, ultrafast, parallel computation systems.

The thesis has been divided into nine chapters. This introductory chapter provides a general background of what optics can offer to computing, why optical digital computation is needed and some historical events in this area. The second chapter contains a systematic overview of the known techniques to perform optical digital computation. Beginning with chapter three, my contribution to the field, i.e. various new optical digital computing concepts and implementation methods are described. In chapter three, three new ultrafast optical switching techniques to perform optical single- as well as array-switching are described. These are the ultrafast optical Sagnac interferometric switch (SIS), optical phase conjugate (OPC) array and optical noncollinear second harmonic (SHG) array switch. In chapter four, using an optical SIS as a fundamental building block, various ultrafast optical binary and binary encoded multiple-valued logic elements are proposed. In chapter five, as alternative optical logic implementation techniques, a number of new pattern logic encod-

ing and processing methods are described. In chapter six, the research on the optical implementation of fast interconnects is reported. An optical SIS sampler, a theta-modulation (T-M) A/D converter, an OPC-based reconfigurable cross-bar, as well as various static optical generalized perfect shuffles are presented. In chapter seven, based on the various proposed logic and interconnect elements, optical binary arithmetic operations are described. In the last two chapters, new optical non-binary arithmetic computing techniques are described. Specifically, in chapter eight, optical binary encoded multiple-valued arithmetic computation is proposed, while in chapter nine, new optical techniques to implement residue and modified sign-digit (MSD) arithmetics are presented.

1.2, What Optics Can Offer to Computation ?

Compared with electronics, optical beams and materials possess several salient properties: (1) 3-D unbounded propagation - optical beams can propagate in any direction in the 3-D space, (2) non-interaction in a linear medium - optical beams can intersect without interaction in a linear medium, (3) polarization - optical beams with orthogonal polarization states can propagate together without interaction, (4) high processing bandwidth - some optical materials can process more than 100 GHz bandwidth optical signals, and (5) ultrafast processing speed - optical pulses has been compressed down to eight femtoseconds (10^{-15} sec.) [1] and some material switching speeds are also in the femtosecond region. The first four properties have been known for many decades, while the last property, as a result of laser and other modern-day technologies, is relatively new (the recent 10 years). A combination of the first four properties determines the parallel processing nature of optics. Because of these ultrafast and parallel processing advantages, optics can be used to perform parallel, ultrahigh processing speed symbolic and numerical computations.

1.3, Why Digital Optical Computing ?

Historically, most of the optical computing research has been performed in the analog domain. To use the parallel processing property of optics, the two orthogonal spatial coordi-

nates are used to represent two independent variables. The system input and output are either complex amplitudes, intensities, or polarization states of the beams. Typically, using a combination of lenses, prisms, mirrors, gratings, holograms, etc., light patterns are transmitted from one plane to another. With different arrangements, a number of important operations, such as analog addition, subtraction, multiplication, Fourier transformation, as well as convolution/correlation of images can be performed.

Compared to digital mode, the optical analog mode computation has three major disadvantages[2]. They are noise accumulation, approximation noise, and limited flexibility. The first drawback with an analog system is the noise accumulation, i.e. noise propagates in a cascaded analog system. To describe, two, an analog and a digital, optical circuits are shown in Fig.1.3.1 (a) and (b). Each circuit contains a number of basic units cascaded in serial. G_i and Q are the i^{th} unit amplifier and the quantizer, respectively, while x_i and y_i represent i^{th} stage input and output amplitudes. Note that the difference between Fig.1.3.1 (a) and (b) is that in (a) the Q acts simply as a measurement device that does not affect the transmitted value between stages while in (b) Q acts on the value being transmitted from one stage to another. As a result, noisy error generated at the first stage processor in the Fig.1.3.1(a) system will affect the second and subsequent processing stage results. This is not the case with the digital system shown in Fig.1.3.1(b) since the quantizer function is both measured and passed on to the next stage. Thus, the i^{th} stage looks just like the first stage and all stages individually have the same error probability. Thus, it can be concluded that the error probability for a digital computing case is much less than for its analog counterpart. This result can be extended to general computations.

The second problem with the optical analog computing system is the approximation error. Since for any given operation, it is necessary to first synthesize its appropriate transfer function. However, it is always a difficult problem to find an exact transfer function for the desired operation. Although for a digital system, this type of problems may also exist, the accuracy and desired range of approximation can be set to any level.

The third problem is the limited flexibility. As mentioned above, the available optical analog operations are primarily Fourier transformation related operations. Although the optical Fourier transform is certainly more powerful than any of possible electronic implementations, it is still not enough for performing many desirable computations. In other words, the available analog optical computation methods can hardly meet general processing capability. The flexibility of digital system has been recognized as a major driving force behind the interest in developing digital optical computing techniques.

1-4. A History Of Digital Optical Computing Research

Digital optical computation research was initiated about two decades ago. Shortly after the invention of semiconductor laser, the use of laser quenching as binary logic operators was proposed[3]. At the same period, coherent spatial filtering has also found application in logic generation[4]. Since so many new things and promising applications, such as laser holography, interferometry, and spectroscopy, also came of age, this enthusiasm faded away. The renewed interest returned in the earlier 1970s with several other proposed methods to implement optical logic components[5-8]. This time, because of the lack of efficient optical materials and the necessary cooperation among physicists, optics and computer engineers, the discrete, noncoherent research were not able to convince the optics community that optical computing was feasible. From late 70s up to now, the third and stronger trend towards digital optical computing has been witnessed. Over the past few years (after 1983) this topic has even been highlighted at many international conferences and by DOD. This increased interest was mainly due to a number of significant breakthroughs in the related fields, such as, in nonlinear optics, ultrafast laser technology, optical information storage and processing, integrated and fiber optics, as well as the rediscovery of residue and other number representations.

During th current period, research have been performed extensively ranging from the proposed optical computing architecture to the single logic gate design, from the hardware implementation to the software development, from the storage scheme to the

interconnection device, etc.. Some results became very encouraging. Research in optical bistability demonstrated materials with nonlinearity strong enough for implementing cascadable room temperature picosecond, picojoule, optical logic operations[9]. The material development using polymers and superlattice semiconductors has provided more hope for viable optical digital computing that can compete with its electronic counterpart. Another subject that relates optics to computation is the optical memory. Technology has been developed to replace the electronic read-only memory disks with its optical counterpart because, in comparison with an electronic one, an optical disk is much more efficient. For device part, high bandwidth electro-optic (EO)[10] and acousto-optic (AO)[11] devices have been developed to match some special purpose parallel computation requirements. These devices have found applications to optical A/D conversion, optical convolution/correlation, as well as optical matrix manipulations. On the other hand, for the software or algorithm part, several significant progresses have also been reported. These include the use of the optical residue [12-14], the modified sign-digit[15-17] and other multiple-valued number representations[18-20] for pipelined parallel computations.

The future advances in digital computation throughput and capability can only be achieved by exploiting faster switching scheme, more efficient nonlinear materials and computation parallelism, and by algorithmic and architectural innovations. Because of ultrafast processing speed and parallelism of optics, over the next few years, the growing maturity of optical computing concepts and corresponding device technologies will be witnessed. Digital optical computation will be demonstrated to be the right direction to the solutions of generating the future powerful, ultrafast, parallel, and intelligent computation systems for many civilian and military needs. The purpose of this thesis is to contribute a number of new ideas and approaches to the optical computing field. I hope that my research together with many other people's work will eventually lead to the birth of the "golden child" - an ultrafast digital optical computer.

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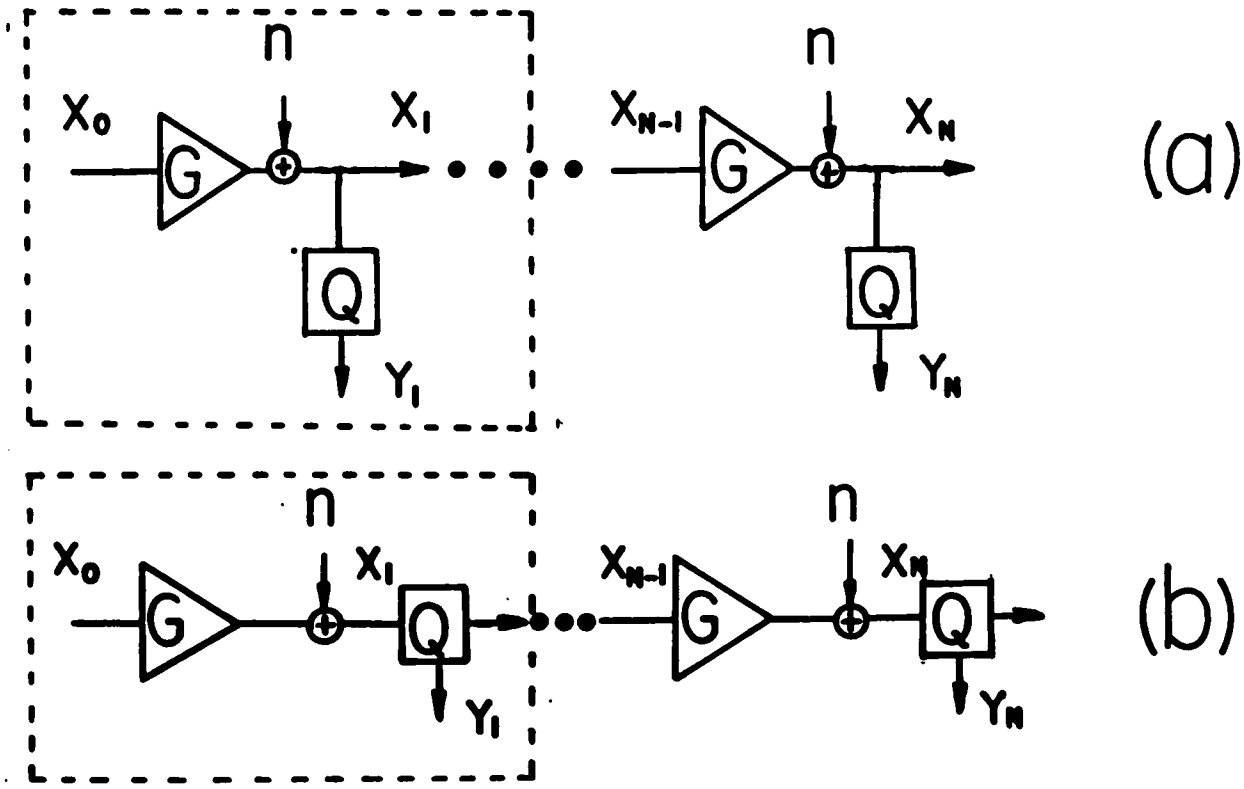

Fig.1.2.1 Two, an analog (a) and a digital (b), network. The basic cell contains an unit amplifier and a sampler.

II. DIGITAL OPTICAL COMPUTING - AN OVERVIEW

Before presenting the details of this thesis research, a review of existing optical computation research efforts is helpful. In particular, the following topics, i.e. digital optical logic, interconnection, A/D conversion, binary as well as non-binary arithmetic implementation, are discussed.

2.1, Optical Logic Devices

For a conventional digital computer, the fundamental element that performs all three basic functions - arithmetic and logic operations as well as a memory element - is a two stable state switch. It has been shown that an electronic switch has its practical switching speed under 1 ns (10^{-9} sec.). Because of the high speed (femtosecond) and the large bandwidth (5×10^{11} Hz) properties of optics, an optical switch is a promising canonical switching element for an all optical digital computer[1]. Up to now, various types of binary optical and hybrid (E-O or A-O) switches have been proposed. For such switches, three optical binary switch state representations are often used[2]. They are (1) the on/off states, (2) the orthogonal polarization states, and (3) the orthogonal spatial pattern states.

2.1.1, Optical intensity on/off logic switches

The first optical logic switch proposed for computation was an intensity on/of state INVERTER where the semiconductor laser quenching phenomena was used[3]. Two intersected laser cavities are implemented with the same semiconductor substrate. First, using current power supply, laser beams were generated in a first cavity that produces an output P_o. As the input light P_i incident to a second cavity, the interaction of two beams can switch off the majority part of the first beam. Thus, this circuit gives inversion operation and an isolation between input and output.

Based on intensity threshold, both logic AND and OR operations were reported. The system consisted of a Fabry-Perot laser resonator with an Nd:glass core and some fibers as

input-output waveguides[4]. Inputs were superimposed on the fiber plate. When the inputs reach a threshold at the onset of lasing, the parallel switches were functioned. The shortcoming of this approach was it causes the change of wavelength from input to output. As a similar approach, the channel plate image intensifier was suggested to perform logic operations [5]. By sequentially applying two logic inputs and adjusting the final acceleration voltage to the phosphor screen, the AND, OR, EOR operations were obtained.

Using a liquid crystal (LC), a variable grating mode (VGM) logic functional device has been reported[6]. The voltage input can create a variable frequency sinusoidal grating inside the LC device. When a optical beam was incident on this LC plate, depending on both the optical and the LC grating frequencies, certain diffraction patterns can be obtained. In other words, the device performed a voltage to angle modulation. When the logic valued are coded spatially, various operations can be performed.

Using E-O waveguide couplers, optical logic operations were proposed[7]. Sandwiched by electrodes, two or more waveguides were directed to a piece of nonlinear substrate. The differently applied electric signals control the guided wave propagation modes which in turn switch the light from one channel to another. Since this type of switch can easily be integrated, its research has been extensively performed and various logic switch geometries were proposed.

In addition to E-O, A-O switches were also proposed. Using either Bragg or Rama-Nath deflection mode, input beams were deflected by the acoustic waves generated by the piezo-electric material across the A-O cell[8]. In this case, the logic input was an electric while output was an angle modulated optical signal. For the fast operation, devices using surface rather than bulk acoustic waves were suggested. Monolithic integration of these A-O surface-wave devices has also been proposed and implemented.

Similar to waveguide switches, optical interferometric switches have also been investigated. Various two-beam interferometers, such as Young, Mach-Zender, Michelson, as well as multiple-beam, i.e. Fabry-Perot (F-P) devices were suggested. For a two-beam

interferometric switch, work has been reported to construct a guided wave modulator using an E-O two-beam device[9]. One arm of the interferometer contains an E-O modulator to which when voltage was applied; it adds a π phase shift to the light passing through its branch. The interference output due to this π phase change could signify either an optical logic zero or a one. Since the dimensions of the waveguide were small and the switch was cascadable, the sequential logic operations can be performed. For a multiple-beam device, the nonlinear F-P etalon receives special attentions for its capability of performing bistable operation. A bistable device can be thought of as the optical nonlinearity (to provide a switching function) combined with feed back (to provide two stable states). The earlier work in optical bistability uses the so-called hybrid effect because a photodetector and electronic feedback were used[10].

In the past ten years, the all-optical intrinsic bistability has been investigated[10]. When a weak optical signal is incident on a F-P etalon, the etalon's output state is determined by its cavity round-trip phase set by the geometrical distance and material linear index. As the input intensity increases, the material nonlinearity causes the cavity index change. This change causes the output intensity to increase or decrease. Because of the positive feed back, this output change will then affect the cavity refractive index that further increases or decreases the next output state, ... etc... Finally, a nonlinear hysteretic output vs. input relation can be observed. The research in optical bistability and multistability has been extensively performed in recent years. Room temperature, picosecond, picojoule optical switching has been demonstrated[11]. Using different bistable operation thresholds and input wavelengths, optical AND OR EOR NOR operations were observed [12].

2.1.2, Optical polarization logic switches

By optical polarization switches, we mean those devices whose two binary levels are optical beam two orthogonal polarizations. In some cases, to cascade a polarization switch with an on/off device, the output of a polarization switch is designed to have an on/off format. The main reason to develop this type switch comes from the belief that since only

polarization states rather than beam power are changed, the polarization switch is most efficient.

To switch between polarizations, optical Pockel and Kerr effects were suggested. The optical second and third order nonlinearities are responsible for the optical Pockel and Kerr effects, respectively[13]. Input beams are polarized along a 45° from the sample horizontal (vertical) axis. In a linear region, both orthogonally polarized components probe an identical refractive index. Therefore, the output beam polarization does not change. To switch the input polarization, another beam delivers power to the sample along one particular, say horizontal direction so that the input beam horizontal component probes a different refractive index. As this component changes its phase by 180 °, the polarization of the output will rotate by 90 °. Thus, a polarization switch between two orthogonal states was performed. From a logic point of view, this phenomena represents a logic AND operation. Using either Pockel or Kerr effect, other logic switches have also been implemented. For example, with a LC light valve (LCLV) that is a Pockel element, optical AND, OR, EOR, NAND operations have been observed[14]. However, it has been found that the processing time with LC materials are very slow (in the order of ms). Using LC-based polarization switches, a number of parallel logic computing experimental efforts have been reported where cascaded controllable $\lambda/2$ and $\lambda/4$ wave plates together with polarizers (analyzers) were employed.

Another example of an orthogonal polarization state switch is a degenerate optical phase-conjugation (OPC) element [15], With a polarization beamsplitter and a OPC cell, optical AND function was generated. For different logic arrangement, different logic operations are also possible.

2.1.3, Optical orthogonal pattern logic switches

Different from the two above-mentioned classes, the optical spatial pattern logic uses orthogonal image patterns as logic assignments. For example, in an earlier work, optical theta-modulation logic operations were proposed. Binary or even multi-level logic values

were represented by either different frequency or same frequency but differently oriented gratings. Using an analog processor and coherent filtering techniques, spatially encoded logic outputs were obtained.

An extension of theta-modulation logic, known as scattering/filtering technique is also available. Two binary values were encoded by a piece of either scatter or non-scatter plate[16]. Using a coherent processor, the thus encoded values can easily be separated on spatial frequency domain. With different spatial filters, various logic operations on inputs were performed.

Another pattern logic encoding method suggested, instead of sophisticated gratings, a pair of pixels. For each of the two binary values, only one of the two pixels was transparent so that the overlap of two encoded mask pattern is always dark implying the pattern orthogonality [17]. For different logic operations, either different combinations of illuminating sources or different output operational masks were /use used. As differences, the output size with former approach becomes larger, while with the latter approach, it does not change.

With a similar idea, a somewhat different pattern logic known as TSE computing structure was proposed[18]. The motivation came from the Chinese written language that uses pictographic characters as its fundamental elements. In an analogous fashion, the TSE computing structure adopts images rather than bits. Incidently, the TSE is the English transliteration of "word" in Chinese. To process, optical fibers are used as input and output transmission lines, while electronic logic gates together with light emitting elements are used for fundamental processing elements.

Recently, another spatial logic method known as symbolic substitution was proposed[19]. Similar to a TSE structure, inputs are treated as image symbols. For computations, desired outputs are directly generated from the parallel symbolic substitutions. Compared to the conventional computation structure where only input values are used for generating outputs, the symbolic substitution operation acknowledges both input values and their

spatial relations, and thus provide an additional degree of computation freedom. In the proposed structure, the optical symbolic substitution, was decomposed into two sub-operations, a symbolic recognition and a symbolic scription. With a number of lenses, mirrors, beam-splitters, as well as an array of E-O NOR gates, various substitutions were experimentally verified.

2.2, Optical Interconnection Devices

The clock distribution and data transmission are two physical communication bottlenecks limiting the potential performance of the current and future high speed synchronous digital systems. For massive electronic pin-to-pin, chip-to-chip and board-to-board interconnects, the present technology uses high density, 2-D integrated electronic transmission lines. Due to their inherent problems, such as interconnection bandwidth, impedance-matching, non-distorted clock phasing, immunity to signal interference, etc., high speed, high density electronic interconnects are very difficult to perform.

The recent research in optical interconnection for digital system offers new insight into the solutions of these very serious problems. Both optical guided-wave and free-space interconnection approaches have been proposed for increasing the speed, the bandwidth and multiplexity. Theoretical study shows that it is possible to pack these high bandwidth, non-interfering optical waveguides or free-space channels on the order of 40,000/mm^2 to 50,000/mm^2 and fiber channels on the order of 5,000/mm^2[20].

2.2.1 Optical static interconnect

For on-board clock distributions, optical holograms has been used to hierarchically map laser diode clock signals to various photodetector sites on chip surfaces. One proposed method used a reflection hologram positioned above a integrated circuit board serving as a mapping element connecting a large number of integrated sources and detectors. In particular, the distribution of pico-second pulse optical clock signals on GaAs logic chips has been experimentally demonstrated [21]. In both spatial invariant and variant interconnection cases,

the computer generated holograms were proved to be very effective. In addition, these holograms has also been used as addressable RAM s with free-space channels interconnected to CPU or other peripheral units. Using guided-wave approach with integrated optics technology, fiber and waveguide-based static I/O networks have also been implemented.

2.2.2 Optical reconfigurable interconnect

For the implementation of optical reconfigurable or dynamic interconnections, devices such as optical perfect shuffles[22], optical cross-bar switching arrays[23] have been proposed. An optical perfect shuffle is an optical data permutation element that can be used to form various shuffle exchange networks. It has been indicated, that for some applications, shuffle-exchange networks are very effective in handling dynamic data interconnections. Shuffle-exchange networks are implemented using repeated stages of the so-called perfect shuffle (PS) together with arrays of exchange boxes that can independently either exchange or bypass the adjacent lines. Different combinations of PS and exchange box arrays have found applications in evaluating polynomials, in sorting data, in transposing matrices, as well as in computing the fast Fourier transform. To implement an optical shuffle, the earlier work used optical fiber or waveguide arrays[24]. One shortcoming with this approach was that for large data arrays, large bundles of fibers are needed. To take full advantage of the free-space propagation property of optical waves, the use of unguided implementation approaches were also proposed. An unguided OPS consisted of either a hologram or a suitable lens and prism combination. While the holographic OPS requires monochromatic light inputs, the lens/prism based counterpart can also be used with white light illumination.

As mentioned above, another method to perform optical dynamic interconnection uses optical cross-bar switches. An N-bit cross-bar switch has N input and N output channels. These channels are crossed to form N^2 intersections. At each intersection, a switch is placed. With the cross-bar network, signals can be switched from any input to any output channels. An analogous to its electronic counterpart, an integrated E-O waveguide switch array has been suggested. However, as the number of channels increases, this approach provides

no additional advantage than its electronic counterpart. A free space propagation mode cross-bar switch has also been proposed and implemented. With an input and an output cylindrical lens, input and output channels were expanded in one dimension to form perpendicular light bar arrays that arrived from both side to a 2-D switch array. The program controlled switches switched an input to an output channel. In particular, optical deformable mirrors were used as these switches.

To physically construct these high speed interconnects, some practical problems, such as the laser diode fan-out, size and speed, micro-hologram efficiency, source-channel and channel-detector coupling efficiency, as well as detector response, size, etc., have been considered. For sources, high modulation frequency (15 GHz) laser diodes were suggested. When the holographic approach was used, these diode should provide 2 - 5 mW power. In addition, for the source geometry, surface-emitting or plano-laser diode array has been proved to be optimum. For detectors and detection circuits, a number of important issues have been considered. First, the process employed to fabricate the detectors should be compatible with the process for circuit fabrications. Second, detector sizes should not significantly increase the chip size. Third, the detection area should have the tolerance for the signal drifts caused by signal frequency shifts. Although optics offers 3D space multiplexity, for relative long distance data transmission, diffraction problem will become seriously. Also, since for each channel, a source/detector pair was used, the overall packaging of the interconnection network might be off the scale. Thus, various multiplexing schemes have been employed. The use of wavelength multiplexing decreases the number of waveguides for long-haul data transmission but not the number of optical source/detector pairs. To alleviate this problem, time-domain multiplexing was also used. However, the use of time-domain multiplexing requires faster source/detector pair. Therefore, with the present technologies, for different requirements, different trade-off must be made.

2.3, Optical A/D Conversion Devices

In any digital systems, a number is represented by a set of discrete bits. To communicate between an analog and a digital devices, a A/D conversion device is needed. In practice, high speed A/D converters are desperately needed to translate sensor measurements into the digital language of computing, signal processing, and communication and control systems. To convert an analog wave to a train of binary digits, a conventional method uses two, a sampling and a conversion, steps. For this reason, in the past, interest has been focused on developing fast optical sampling techniques. To obtain high speed optical sampling, optical Kerr effect was commonly adopted. In one approach, an optical polarization preserving fiber was used as Kerr material [25]. An analog signal with frequency ω_1 and a train of optical sampling pulses with frequency ω_2 are guided into the Kerr fiber. The sampling pulse strength and the fiber length are chosen such that the fiber nonlinear index change caused by the sampling optical pulse is enough to rotate the analog signal polarization state by a 90°. At the output, a cross-polarizer as an analyzer was used to pick up the sampled analog signals. Experiment using fused silica fiber (1 ps response) with 100 ps sampling laser pulses was presented[25].

To perform optical A/D conversion, E-O interferometric approaches were proposed. The operational principle of such a device is based on the periodic dependence of interferometric output intensity on applied voltage. In one method, Mach-Zender type $LiNbO_3$ waveguide devices were used[26]. A train of laser sampling pulses is split into a number of parallel channels that lead to these interferometers. Each interferometer is controlled, through a different length electrode, by an input analog voltage signal. At the output, each interferometer generates its own voltage modulated signal. A collection of all outputs represents the binary version of the analog voltage input. Experimentally, the 500-MHz operation of a 4-bit A/D conversion has been demonstrated [27].

To generate the voltage controlled periodic outputs, other waveguide-based approaches, such as E-O balanced bridge and Fabry-Perot modulators, have also been

described[28,29]. A common feature of these A/O converters is that an additional electronic comparator arrays are needed. Using a different, a shadow-casting, approach, spatially encoded A/D conversion was also performed. A set of masks are used as digital bit planes. Analog input signals are also spatially encoded. With appropriate superpositions, an output image can be generated that corresponds to the input signal binary representation.

2.4, Non-binary Optical Computing Techniques

In some cases, non-binary computing techniques can offer a speed increase over the binary approach. For this reason, considerable interest has been received to develop various number representations and their algorithms.

2.4.1 Optical residue arithmetic

One of the well known non-binary computation method uses the residue number system[30]. The residue number system is based on a set of K-tuple of prime (no common factors) integers, each of which is called a modulus. Compared to decimal and binary arithmetic, one important feature of residue arithmetic is that no carries are used so that computations can take place in parallel. Thus, in principle, the residue arithmetic offers a faster processing speed than its binary and decimal counterparts.

To implement an optical residue processor, different types of physical phenomena have been proposed. Among the proposed structures, two major approaches were used. They are the use of phase, polarization, and spatial position in situations where they provide an cyclic response characteristic; and the use of table look-up memory. With the first approach, E-O techniques for residue encoding, processing, and decoding based on cyclic optical polarization and phase modulation were used. A spatial light modulator was also used to generate the repeated accumulation of polarization rotations[31]. A lens and grating-based coherent processor that is capable to perform decimal-to-residue and residue-to-decimal conversions was presented[32]. In this processor, residue number was encoded as spatial positions. Using an array of E-O directional waveguide couplers, an integrated residue proces-

sor was also proposed. With a second approach, both direct table look-up and content-addressable memory methods were developed. Residue numbers were commonly encoded with different spatial positions. With holographic techniques, the content-addressable table look-up method promised a fast processing speed and a compact geometry[33]. One shortcoming with a residue processor is that when large numbers need to be processed, large prime modulo logic elements, elements that are difficult to implement, must be used. Furthermore, since the different modulo subprocessors create a non-symmetric system architecture requiring many delay elements, these architectures can also lead to a speed reduction. Thus, to gain the advantage of parallel processing while reducing the implementation complexity, other number representations and algorithms have been sought.

2.4.2 Optical modified sign-digit (MSD) arithmetic

It has been indicated that the modified signed-digit (MSD) number representation is another candidate for fast, parallel digital optical arithmetic processing operations[34] The MSD is a redundant radix-two number representation. With its balanced weighting factors, the MSD can represent both positive and negative numbers. Using this balanced nature, a number of bit-wise transfer and weight function rules for MSD arithmetic have been proposed. To optically synthesize both the transfer and weight logic functions, a location-addressable memory (LAM) logic was first proposed[35]. According to four addition rules, four different processors that employ arrays of prisms, gratings, and bistable etalon were constructed. Later, using optical symbolic substitution methods, a modified MSD adder was proposed. Using three parallel symbolic substitution steps, MSD addition of two integers were described.

2.4.3 Other optical non-binary arithmetic

In addition to the residue and MSD arithmetic, other non-binary logic and arithmetic computing methods have also been introduced. An example is the use of ternary or quaternary number system for logic computing[36]. The use of higher logic density for computing

can transfer and process more information through each interconnect in a unit time interval. Using E-O devices together with spatially coded inputs, both ternary and quaternary logic processors were proposed. Using this method, various Post and Webb logic operations can be implemented. Experimentally, a ternary to binary converter and a ternary half adder were constructed. Other non-binary optical arithmetic and logic computing techniques reported included the use of decimal[37], mixed-binary, as well as higher order redundant number representations.

2.5, A Short Summary

Although considerable amount of work has been performed, relative to digital electronics, the research in digital optical computing is still in a new-born stage. For almost all related areas, evolutionary improvements and revolutionary breakthroughs are needed. To compete with an electronic computer, a large number of fundamental research and engineering problems need to solve. The recent rapid research increase in optical computing has shown that a digital optical computer will no longer be just a dream but a foreseeable real machine.

2.6, References

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III. NEW ULTRAFAST ALL-OPTICAL SWITCHES FOR OPTICAL COMPUTING

3.1, Introduction

The fundamental element in a digital computer is a switch. For various reasons, an electronic switch has its switching speed in nanoseconds. However, because of the high speed (femtosecond) and other properties (such as large bandwidth and interaction-free propagation) associated with an optical beam, an optical switch is a promising switching element for an ultrafast digital computer.

The optical $\chi^{(2)}$ and $\chi^{(3)}$ nonlinearities are sources of various ultrafast optical phenomena[1]. Since an ultrashort optical pulse can be focused to deliver an ultrahigh instantaneous power density (power/area), $\chi^{(3)}$ is more popular and easier to use for optical switching. One example is a multiple-beam nonlinear Fabry-Perot interferometer switched by an optical pulse[2]. Because of its compact geometry, good mechanical stability and ease of alignment, in the past decade, a rapid research interest increase in this area has been observed. Compared to its multiple-beam counterpart, the two-beam interference phenomena, that in principle requires the same (as its multiple-beam counterpart) amount of power to switch, has seldomly been used. This is mainly due to the poor mechanical stability associated with most two-beam interferometers. In this chapter, we first describe a new two-beam switching device - a Sagnac interferometer (SI)[3] that does not suffer from the poor mechanical environment. Because it is also compact and easily to align, it can be used as a fundamental switching device for various logic processing. Following the discussion about the two-beam optically controlled interference, an ultrafast optical phase-

conjugation (OPC) effect[4] (also $\chi^{(3)}$ dependent) for switching will also be described. Unlike other proposed OPC logic structures where either the input phase or its polarization (related to phase) is utilized to obtain either a phase or polarization conjugated output[4,5], here, an OPC device is simply treated as an array of parallel switches that in response of an intensity input generates an output distribution. Next to the OPC, in a similar fashion, another well known ultrafast phenomenon - a noncollinear second-harmonic generation (SHG)[6] effect that uses $\chi^{(2)}$ nonlinearity will be introduced for ultrafast parallel switching. Because the SHG input and output frequencies are different, it has not been introduced to optical computing. However, despite of this frequency change, it does possess many unique advantages, such as speed and array processing capability, over many existing optical switches.

3.2, A Sagnac Interferometric Switch (SIS)

3.2.1, An optical Sagnac interferometer (SI)

Over the past two decades, there has been considerable interest in using the interferometric method to probe short-time phenomena. Work has been performed to diagnose plasma produced by an ultrashort laser pulse.[7] One of the advantages of using pulsed laser interferometry (PLI) is that it solves the so called synchronization problem. Other works using PLI are also available[8,9]. In all these experiments, there is a common problem. Because of the instability of optical components, there is no fixed phase relationship between two interfering beams, i.e. for the same physical condition, fringe patterns due to different laser shots are not identical. As a consequence, most applications are restricted to measurements of single shots events. Recently, this problem has been overcome using a new technique of combining a Mach-Zehnder type interferometer (MZI) with an active electronic stabilizing device. The active MZI was used to measure the orientational relaxation time of CS_2 [10]. This measurement was accomplished by real time scanning of the signals resulting from the interference between a reference pulse and the pulse that has

undergone an induced refractive index change caused by a strong laser pulse. The output optical signal is stable because, for different laser shots, a fixed phase relation exists between two interfering beams. However, an electronic feedback control system is needed. In addition to the expense, the method works well only for either cw or high but not for low repetition rate pulse lasers.

In most interferometers, the two optical beams traverse distinct optical paths before recombining. While the use of different optical paths has many advantages, unfortunately, it does not allow for auto-compensation of unwanted vibrations. This may not be the case for a SI. Here, the two interfering beams travel along identical optical path but in opposite directions. The applications of the SI are found in constructing the antiresonant ring lasers; in coupling the laser output as well as in performing the optical inversion [11,12,13]. The purpose of this section is to show the stability advantage of a SI over that of a MZI.

Consider two different interferometers (see Fig.3.2.1). In Fig.3.2.1(a) a rectangular SI, while in Fig.3.2.1(b) a rectangular MZI are depicted. The solid lines designate the two ideal and identical optical paths ($l_1 = l_2$), where, $l_{1,2}$ are the path length of arms 1,2, respectively. When the mirror M_2 suffers a translational shift (Δx; Δy), the new optical path difference in the SI can be expressed as:

$$\Delta l_s = |l_1 - l_2 + 2(\Delta y - \Delta x)| = 2|\Delta y - \Delta x| \qquad (3.2.1)$$

While for the same translational shift for a MZI, the two beams can not recombine at the same point on the beamsplitter (BS). When a beam of coherent plane wave with the finite beam width is used, the new optical path difference for the MZI is:

$$\Delta l_m = |l_1 - l_2 + \Delta y| = |\Delta y| \qquad (3.2.2)$$

For a purely translational shift, Δy should be equal to Δx. Then, Eqs.(3.2.1 and 2) reduce to $\Delta l_s = 0$, and $\Delta l_m = \Delta x$. This result shows that a SI is less sensitive to vibrations than a MZI.

The phase difference between the two interfering beams is

$$\Delta\phi = \frac{1}{c}(\Delta l\, n\, \omega + \Delta n\, l\, \omega + \Delta\omega\, n\, l) \qquad (3.2.3)$$

where l is the optical path length, n is the index of refraction, ω is the angular frequency of the optical source and c is the velocity of light. The first term in the parenthesis is due to a vibrational contribution, while the second and the third terms are due to the index of refraction change in one of the optical paths and the frequency shift of the optical source, respectively. When a laser output frequency is stable i.e. ($\Delta\omega = 0$) and when there is no change in the index of refraction i.e. ($\Delta n = 0$) in the optical paths, then both the second and the third terms vanish. Thus, a translational shift in the mirror M_2 does not effect the phase difference in a rectangular SI but does affect a MZI even with a coherent plane wave illumination. The common spatial shift of the interference pattern obtained in the outputs of both interferometers is small and is negligible. When the input beam is not a coherent plane wave (see Fig.3.2.1(b), the MZI suffers an additional phase shift. A rectangular type SI is vibration stabilized as long as it is kept free of rotation and the vibrational frequency is limited to

$$\Omega_{max} < \frac{c}{l_p} \qquad (3.2.4)$$

where Ω_{max} represents the maximum horizontal vibrational frequency, l_p is the optical loop length. It can be shown, that the stability of other type of SI may not be as good as that of a rectangular type SI shown in the Fig.3.2.1(a). For example, a triangular (see

Fig.3.2.1(c)) SI[11,12] can perform the auto-stabilization only with a coherent plane wave illumination. When the input is not the coherent plane wave, a problem similar to that in an MZI will arise.

Compared to other type of interferometers, the SI is easy to align. The use of ultrashort optical pulses requires accurate alignment of the optical elements. In a SI, adjustment are needed only for the counterpropagating beams so that they are incident on the same points on the beamsplitter and on all mirrors. However, a SI has the drawback that some optical beams are retroreflected.

3.2.2, A nonlinear Sagnac interferometric switch

According to Eq.(3.2.3), a change in the refractive index can cause a change in the phase difference between the two interfering beams. This fact has been widely used in interferometry. For most two beam interferometers, when only one of the two beams propagates through a material that has undergone an index of refraction change, the interference pattern can be used to analyze this change. However, in a SI, the two interfering beams travel along the identical path. Any slow change probed by one beam will be compensated by the same change probed by the other beam. Thus a SI is not applicable for many usual cw laser interferometric applications, such as the measurement of the index of refraction change etc. In a pulsed laser operation, however, when one of the two beams undergoes an ultrafast phase change caused by an ultrafast index of refraction change, this change will not be auto-compensated. This fact allows to probe ultrafast dynamics of a material, while benefiting from its vibration stabilization property[14]. Next, the use of a pulsed SI for ultrafast intensity switching is described.

For the construction of a binary interferometric optical switch, switch stability is one of the most important requirements. For a rectangular SI, this requirement is automatically satisfied. We will assume that to realize such a switch, an ultrafast, efficient NLM is available whose orientational relaxation time τ_o is much faster than the inducing pulse width τ_i. For this NLM, the induced refractive index change from its linear counterpart is

$$\Delta n_{||} = n_2 \langle E^2(z;t) \rangle \tag{3.2.5}$$

where the symbol $\langle\ \rangle$ represents the time average, the subscript $||$ is the direction parallel to the inducing light field E, and n_2 is the nonlinear refractive index corresponding to $\chi^{(3)}$. When both a signal and an inducing pulse are passed simultaneously through the NLM, an induced refractive index change $\Delta n_{||}$ is probed. For a SI, when only one of the two counterpropagating beams undergoes this change, the output intensity of the interferometer can be expressed as

$$I_o(z;t) = B \langle E^2(z;t) \rangle \left| 1 + \cos [k_0 L n_2 \langle E^2(z;t) \rangle + \phi] \right| \tag{3.2.6}$$

where B is a constant, L is the length of the NLM cell, k_o is the propagation constant corresponding to the center wavelength of the input beam, and ϕ is the geometrical phase difference between two interfering beams. In order to achieve a π phase shift, a nonlinear material with a high n_2 value is required. For an isotropic material such as CS_2 ($n_2 = 2 \times 10^{-20}$ mks unit), achieving a π phase shift requires 300 MW/cm^2 in a 1 cm cell[15]. It has been reported that PTS polydiacetylene has a higher nonlinearity ($n_2 = 8 \times 10^{-19}$ mks unit)[16]. The recently developed semiconductor multiple-quantum-well (MQW) materials can have nonlinearity orders of magnitude higher than liquid and other bulk materials have. In fact, 3 pJ, 82 MHz optical gates in a room-temperature GaAs/AlGaAs MQW ($n_2 = 10^{-10}$ mks units)[17] have been experimentally demonstrated. Theoretical calculations predict that even performance can be achieved by using flatter, thinner MQW samples. In the following discussion, it is assumed that a π phase change can be induced from a high n_2 material with a reasonable input power. Fig.3.2.2 shows the normalized output intensity curve, calculated from Eq.(3.2.6), for a Gaussian input pulse as a function of time. It has assumed that a 50/50 BS is used. It is clear that the output pulse shape depends on both input pulse shape and the intensity-dependent cosine phase change. For a low initial output alignment ($\phi = \pi$), the output pulse I_o is narrower than the input pulse. However, for a high initial output alignment ($\phi = 0$), the output I_o splits into

two smaller peaks with vanishing intensity at the midpoint[18].

An implementation of a SIS is shown in Fig.3.2.3. The input beams are two light pulses A and R. A cell containing NLM is asymmetrically placed into the interferometer loop so that only one of the interfering pulses can probe the induced refractive index change. Either of the two counterpropagaing pulses R_1 or R_2 can be chosen to undergo this change. To ensure that A and either R_1 or R_2 will arrive simultaneously, a delay prism D is used to adjust the temporal overlap between two beams. Since the cell is placed asymmetrically in the loop, three pulses will not overlap simultaneously in the medium. Therefore, A does not generate a phase-conjugated signal. To obtain a large overlap region, s small arrival angle between the two beams should be employed. When the intensity of beam A is turned off, by an adjustment of the mirror, the interference output I_o can be placed either in an initial low energy state (in an ideal case) or in an initial high energy state. When beam A is turned on, the original output state can be switched (assuming an induced π phase change) from a low to a high state or vice versa.

This interference mechanism can serve in the role of an optical logic inverter (INV). For this INV, the input R serves as a reference beam, while A is the signal beam to be inverted. A similar optical INV is described in Ref.13. There, the NLM is placed at the midpoint of the interferometer loop and is illuminated with a cw laser beams. Since there is no external inducing beam, the nonlinear phase shift is generated by the interaction of two counterpropagating beams. However, in that case, the output high state is lower than the input low state. To have an inversion between two well-defined states, a reference beam is required.

3.2.3, Experimental results

Fig.3.2.4(a) shows our experimental setup[14]. A QUANTEL mode-locked Nd^{3+} : YAG laser generates two pulses: one at 532 and another at 1064 nm wavelength. The 532 nm pulse is separated, by a 50/50 beamsplitter (BS) into two parts: with one pulse traveling in a clockwise while the other pulse travels in a counterclockwise directions. The two pulses

recombine at the same point on the BS. Both beams pass through a 1 cm CS_2 cell. A 1064 nm pump pulse is separated by a mirror (M_1) that only reflects 1064 nm beam. The beam passes through a delay prism (D), driven by a AEROTECH stepping motor, and is then focused to a 1 mm spot in the CS_2 cell. The cell overlap angle, between the 1064 nm beam and the 532 nm beam, is about one degree. All optical beams are vertically polarized. At distances (d_1) and (d_2), two HA-30 filters are used to remove the 1064 nm radiation. At the output of the SI, a HAMAMATSU S-20 photodiode, with a front adjustable aperture is used to collect the interference signal. This signal is displayed on a TEKTRONIX-7104 oscilloscope.

When the 1064 nm pump beam is off, the interference pattern, observed at the output due to the 532 nm beams, contains a few fringes. When at the cell the 1064 nm beam temporally overlaps with one 532 nm beam, such as the counterclockwise beam shown in Fig.3.2.4(a), a portion of the output fringe shifts. This result is due to the refractive index change of CS_2 induced by the 1064 nm beam as probed by only one of the 532 nm (counterclockwise) beam. In fact, either one of the 532 nm beams can be chosen to undergo this induced index of refraction change. We used the beam with a longer path length. To have a required time difference between the two 532 nm beams, the cell is positioned asymmetrically. The front aperture of the photodiode is adjusted so that only the changing portion of the output pattern is detected. A delay prism scans the cell overlap between the 1064 nm pump beam and the 532 nm signal beam. The scanned interference signal, is displayed in Fig.3.2.4(b). The width of the curve is about 33 ps. This width represents the pulse duration of our Nd^{3+}:YAG laser. In general, with CS_2, optical pulses wider than 20 ps can be measured using this method. Our fringe visibility (contrast), defined as $V = (I_{max} - I_{min})/(I_{max} + I_{min})$, is about 52% Since the SI measurement was performed on a table without vibration isolation, the result shown in Fig.3.2.4(b) demonstrates the stability of this device.

3.3, An Optical Phase-conjugation (OPC) Switch Array

3.3.1, Degenerate OPC effect

OPC is a technique that uses various nonlinear optical process to generate an exact phase reversal of an incoming electromagnetic wave[4]. Because of this phase reversal, OPC has found numerous practical and scientific applications, such as wave propagation through a distorting medium, aberration correction, pulse compression, image processing, real-time holography, ultrafast optical quantity measurement, etc.[19].

In this section, the principle of the degenerate OPC is shortly reviewed. When two counterpropagaing optical plane waves $E_{1,2}$ of an identical frequency where

$$E_{1,2} = A_{1,2}(\bar{r})\, e^{i(\omega t - \bar{k}_{1,2}\bar{r})} \tag{3.3.1}$$

and a third wave

$$E_3 = A_3(z)\, e^{i(\omega t - kz)} \tag{3.3.2}$$

arrive simultaneously at a $\chi^{(3)}$ medium, according to the relation

$$P_i = \chi_{ijkl} E_j E_k E_l, \tag{3.3.3}$$

a polarization field

$$P_i(\omega = \omega + \omega - \omega) = \chi_{ijkl}(-\omega,\omega,\omega,-\omega) E_j(\omega) E_k(\omega) E_l^*(\omega) \tag{3.3.4}$$

which can also be expressed as

$$\dot{P}^{(\omega = \omega + \omega - \omega)}(\bar{r}, t) = \chi^{(3)} A_1 A_2 A_3^*\, e^{i[\omega t - (\bar{k}_1 + \bar{k}_2)\bar{r} + kz]} \tag{3.3.5}$$

is generated. Since $\bar{k}_1 + \bar{k}_2 = 0$ and A_1 and A_2 are constants, this polarization field will excite a new electromagnetic wave

$$E_4 = A_3^*(z)\, e^{i(\omega t + kz)}. \tag{3.3.6}$$

that propagates oppositely to E_3. Once generated, this wave will mix with waves $E_{1,2}$ to regenerate the E_3, etc. As a result, the interaction and power exchange of waves $E_{3,4}$ is mediated via the pump waves $E_{1,2}$ (see Fig.3.3.1). Theoretical calculation and experimental results have shown that the OPC power gain and the four wave mixing length L as well as the medium nonlinearity are related by[1]

$$\left| \frac{A_4(0)}{A_3(0)} \right|^2 = \tan^2 |p|L \tag{3.3.7}$$

where

$$p^* = \frac{\omega}{2}\sqrt{\frac{\mu_0}{\epsilon}}\chi^{(3)}A_1A_2. \tag{3.3.8}$$

Since some materials, such as various organic polymers, can offer both large (order of 10^{-11}) and fast (pico- and femtoseconds responses) $\chi^{(3)}$ nonlinearities, the degenerate OPC is a good candidate for ultrafast digital optical computing.

3.3.2, An OPC optical switch array

The use of OPC for optical computing was first proposed by O'Meara[4] who recognized that the polarization-conjugation effect of OPC can be used to form a polarization encoded optical AND gate. In addition to the OPC cell, his AND gate consists of a number of mirrors and polarizing beamsplitters. Recently, a another type of OPC logic gates was proposed. In these OPC elements, each of the two counterpropagating pump beams is spatially equally divided into two parts. With a Kerr cell, that generates a π phase change, placed in either part of the pump beams, the generated OPC signals can form either a constructive or destructive interference pattern corresponding to different logic values. In both approaches, the reversal of the input quantity, either polarization or phase, is utilized. In the following, we will show that a fundamental OPC cell itself is an intensity-encoded AND gate and a large aperture OPC device can generate a large parallel array of monolithic AND gates[20].

In Fig.3.3.2, an OPC device is depicted. Inputs A, B and C are mixed inside the $\chi^{(3)}$ nonlinear material to generate the output O. When intensity coded binary inputs are used, the output O is an AND function of the three inputs, i.e. $O = A\ B\ C$. As a logic function, this triple-input AND operation is not important. However, if a 2D array of such AND elements can be constructed, many useful digital logic, arithmetic as well as interconnection operations can be implemented. In other words, together with various spatial encoding methods, a triple-input AND array can be used to obtain various digital operations. In the later chapters, the of OPC AND gate array for various digital applications will be discussed in detail.

To obtain a large 2D or 3D array of OPC AND switches, a large aperture OPC device needs to be employed. When an area of $50 \times 50\ \mu m^2$ (a practical integrated optics scale) is used for each channel, a $2 \times 2\ cm^2$ OPC aperture contains 1.6×10^5 2D spatial channels. The beam expansion of a commercial QUANTEL mode-locked Nd^{3+}: YAG laser pulse, that can deliver a 60 mJ energy over a 30 ps pulse duration, to $2 \times 2\ cm^2$ area can still provide a power density of 50 MW/cm^2. With this power density and the CS_2 nonlinear material, it is not difficult to obtain the OPC signal over the whole aperture. Using a mode-locked dye laser pulse, even higher power density and a much higher repetition rate (100 MHz) can be obtained so that this $2 \times 2\ cm^2$ OPC device can perform 10^{13} AND operations/sec. Moreover, when a long OPC material cell is used, a 3D AND array can also be obtained. However, to cover the whole 3D volumn, a longer input pulse is needed.

3.4. An Optical Second Harmonic Generation (SHG) Switch Array

3.4.1. Noncollinear SHG effect

The source of the above proposed switches is the $\chi^{(3)}$ nonlinearity. In this section, we will show that the $\chi^{(2)}$ nonlinearity that is based on electronic mechanism can also be used for ultrafast optical switching. Noncollinear optical SHG effect[6,21] for a parallel two-input AND switching will be described.

When two input electromagnetic waves $E(\omega_1)$ and $E(\omega_2)$ are directed to a $\chi^{(2)}$ crystal, a polarization field

$$P_i^{\omega_3 = \omega_1 + \omega_2} = \chi_{ijk} \; E_j^{\omega_1} E_k^{\omega_2} \tag{3.4.1}$$

is generated. When both input waves have an identical frequency ω, the Eq. (3.4.1) reduces to

$$P_i^{2\omega} = \chi_{ijk} \; E_j^{\omega} E_k^{\omega}. \tag{3.4.2}$$

Depending on a phase-matching condition, the generated polarization field may radiate a frequency-doubled wave $E^{2\omega}$ where[1]

$$E_i^{2\omega} = D \; \chi_{ijk} \; E_j E_k \frac{e^{i \Delta k L} - 1}{i \Delta k} \tag{3.4.3}$$

where Δk and D are a phase mismatch and a constant, respectively. For a perfect phase match, the relation

$$\bar{k}_2^{2\omega} = \bar{k}_{11}^{\omega} + \bar{k}_{12}^{\omega} \tag{3.4.4}$$

where subscripts 11 and 12 denote the first and second input components, must be satisfied. Since the ordinary material dispersion function is always a single-valued function with respect to frequency, conventionally, Eq.(3.4.4) can never be satisfied. However, with some birefringent materials where both ordinary and extra-ordinary refractive indices exist, Eq.(3.4.4) may be satisfied. In Fig.3.4.1, for ω and 2ω, two pairs of index ellipsoidals where subscripts o and e denote ordinary and extra-ordinary are depicted (a negative uniaxial crystal is assumed). With these ellipsoidals, input vectors must be chosen so that their vector sum is equal to the SH output vector. Such a phase-matching case is also shown in Fig.3.4.1, where $\bar{k}_{11}$ and $\bar{k}_{12}$ are two primary input wave vectors with θ_{11} and θ_{12} as angles to the crystal optic axis OX. $\bar{k}_2$ is the frequency-doubled output wave vector. The

phase-matching geometry shows the relation:

$$|\bar{k}_{11}| \cos(\theta_2 - \theta_{11}) = |\bar{k}_{12}| \cos(\theta_{12} - \theta_2) = |\bar{k}_2/2| \qquad (3.4.5)$$

When this condition is satisfied, the input and the SH signals must be ordinarily and extraordinarily polarized, and the SH signal emerges with an angle that bisects the input beam intersection angle, i.e $\theta_2 - \theta_{11} = (\theta_{12} - \theta_{11})/2$. Note that a special case, also known as a 90 ° phase-matching[21], occurs when $\theta_2 = 0$. Since the input and output frequencies are well separated and the phase-matching condition acts as an angular filter, noncollinear SHG has widely been used as a background-free detection method for measuring temporal information down to 8-fs[22]. Another advantage of SHG process is its angular or frequency multiplexity. In Fig.3.4.2 these two cases are shown with their corresponding phase-matching diagrams. In Fig.3.4.2(a), using an angular multiplexed SHG crystal, two parallel channels I and II are parallel processed, while in Fig.3.4.2(b), with a frequency multiplexing scheme, two channels of differency inputs are parallel processed. With these schemes, a SHG device can be used for ultrafast and parallel signal processing and computation.

3.4.2 SHG-based optical array switching

Similar to OPC, a SHG device can also be viewed as an optical AND gate. In Fig.3.4.3(a), a SHG-based AND gate is shown. Two symmetrical identical frequency and polarization logic input beams, denoted as A and B with an angular separation θ, are directed into the SHG crystal. When the angle is adjusted so that the phase-matching condition is satisfied, in the bisecting input angular direction, a second harmonic (SH) output is generated. One advantage of this structure is that, since only a small part of the input energy is converted to a SH output, most of the fundamental input power passes through the gate allowing the outputs to be used as inputs to feed subsequent AND gates. In Fig.3.4.3(b), with parallel input pulses, a schematic SHG AND gate array where the intersections indicate the AND element placements is shown. The outputs from these elements are marked by dashed lines. To guarantee the simultaneous arrival of the two optical

signals at each intersection, using either a holographic grating or a composite prism , both input wavefronts are tilted at an angle[23]

$$\theta = \sin^{-1}[n_o(\lambda)\sin(\phi/2)] \qquad (3.4.6)$$

where the use of negative uniaxial crystal is again assumed. The output of each logic AND gate is directed to subsequent logic or memory device for further processing. When the two groups of inputs, each containing N channels, are used, the generation of up to N^2 outputs is possible. This network is similar to an optical cross-bar switch[24], except that the roles of the input and output are interchanged. Another major attraction of this scheme is that an array of optical AND elements can be monolithically implemented on a single crystal plate. It is, therefore, suitable for optical circuit integration. Using either different input frequencies or different phase-matching directions, either frequency or angle-multiplexed multichannel processings can be performed. For multi-stage operation, since it is necessary to convert the SH signal back to its fundamental frequency, parametric frequency down (PFD) conversion is needed[23,25]. Using a parametric wave-mixing process with a strong fundamental frequency third-harmonic (TH) beam, the SH signal can be converted to the fundamental and amplified. With a KDP crystal, the process has been experimentally demonstrated [26].

3.5, Summary

In this chapter, three new fundamental ultrafast all-optical switching schemes were introduced. Among the three approaches, the two-beam interferometric and the OPC switching schemes use $\chi^{(3)}$ while the SHG scheme uses $\chi^{(2)}$ as the source of nonlinearity. In comparison, the input and output frequencies are identical for the first two, i.e. SIS and OPC, schemes, and are different for the last, the SHG, switching scheme. In terms of switching speed, the SHG switch offers a fastest speed (fs) because of using purely electronic $\chi^{(2)}$ nonlinearity. Using different NLM placements in a SI loop, different optical intensty on/off binary and multiple-valued logic elements can be constructed. On the

other hand, together with various spatial encoding schemes, OPC and SHG array switches can also be used for optical logic processing. From the next chapter and on, based on these three new fundamental ultrafast switches, various digital logic, arithmetic and interconnection processors will be proposed. Some of them will be experimentally demonstrated.

3.6 References

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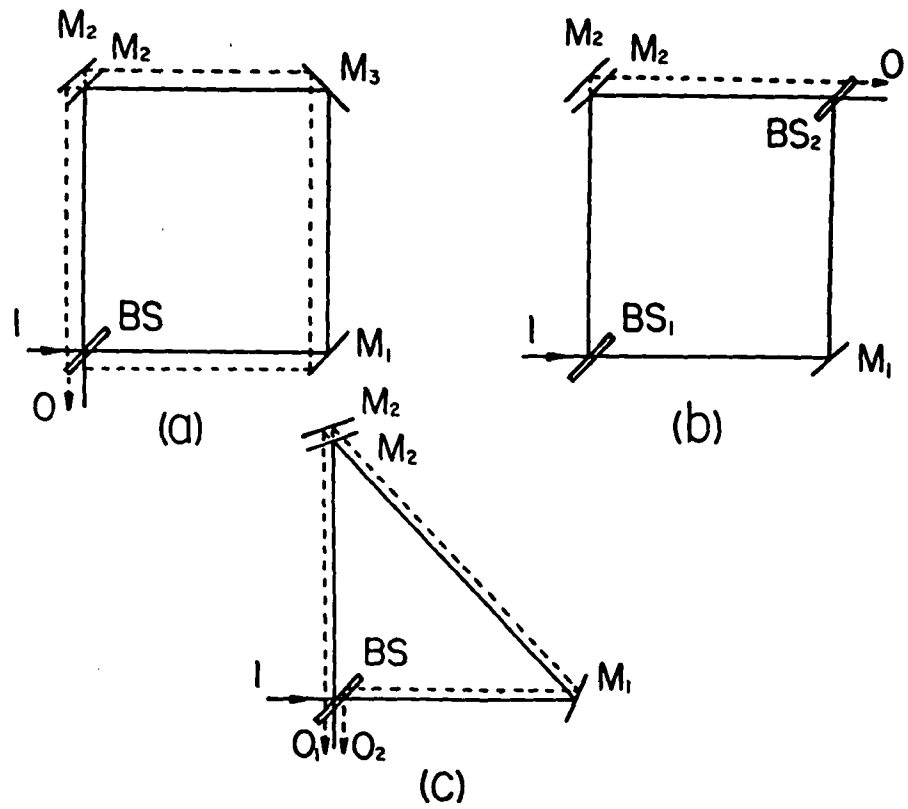

Fig.3.2.1 Vibrational stability comparisons betwen different arrangements of interferometers: (a) a retangular Sagnac; (b) a rectangular Mach-Zender; (c) a triangular Sagnac interferometers. Δx, Δy, translational shift of a mirror caused by vibration.

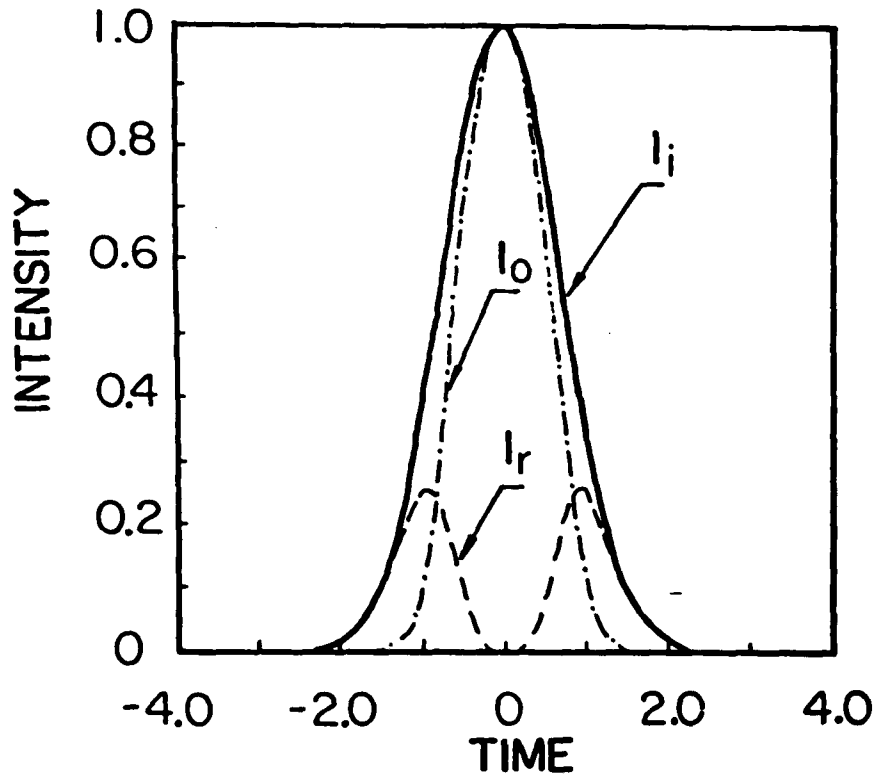

Fig.3.2.2 Normalized time-dependent input-output relation for a Gaussian input pulse in a Sagnac interferometer.

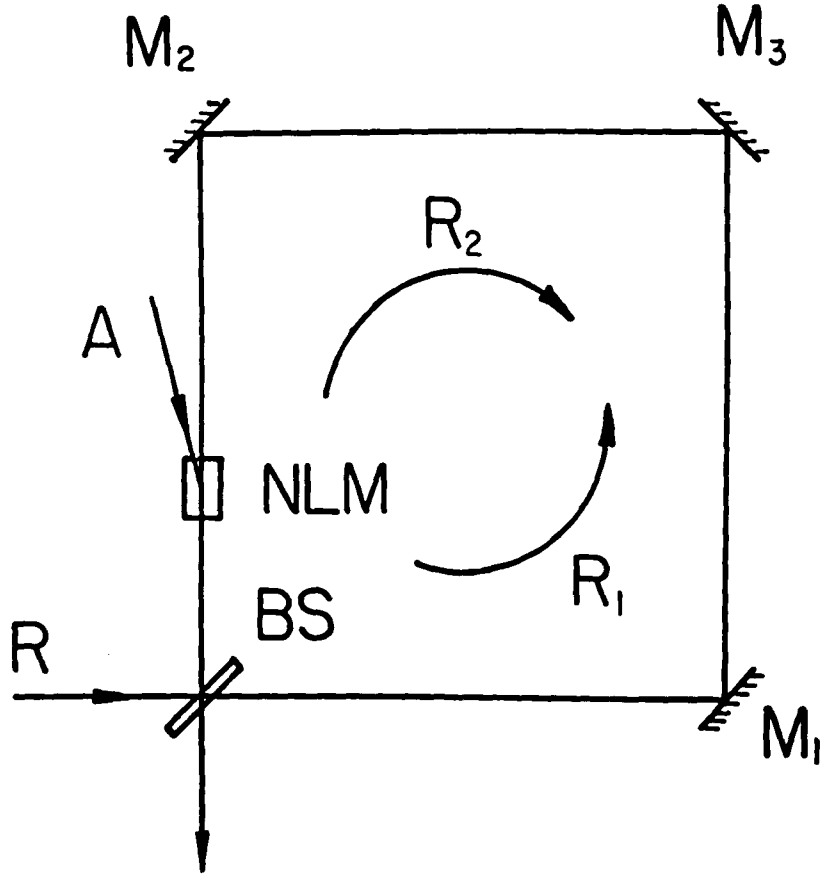

Fig.3.2.3 Optical SI implementation of a logic INVERTER. NLM, nonlinear material; A, inducing (logic input) beam; R, reference beam, with subscripts 1 and 2 as counterclockwise and clockwise directions.

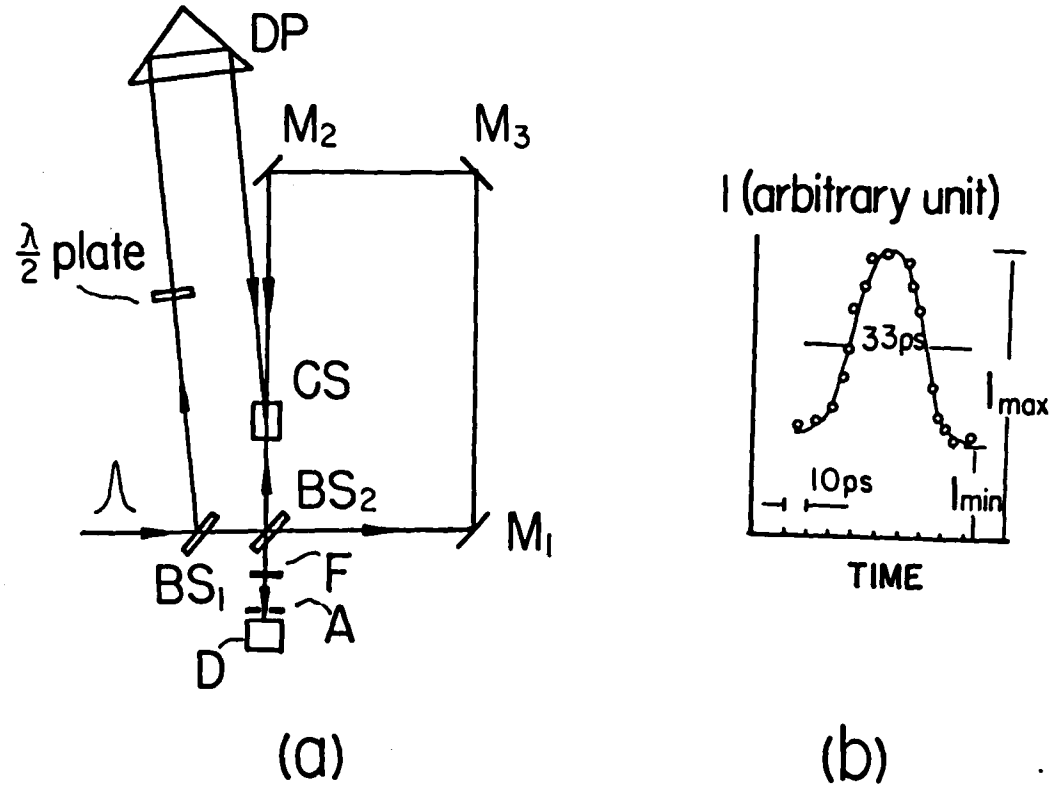

Fig.3.2.4 (a) Experimental setup. The input pulse contains two wavelengths at 1064 (532) nm and M, mirror; BS, beamsplitter, DP, delay prism; F, filter; λ/2 plate, half wave plate; A, adjustable aperture; and D, detector. (b) Output intensity curve obtained by scann ing the overlap between pulses at CS_2 cell vs delay time.

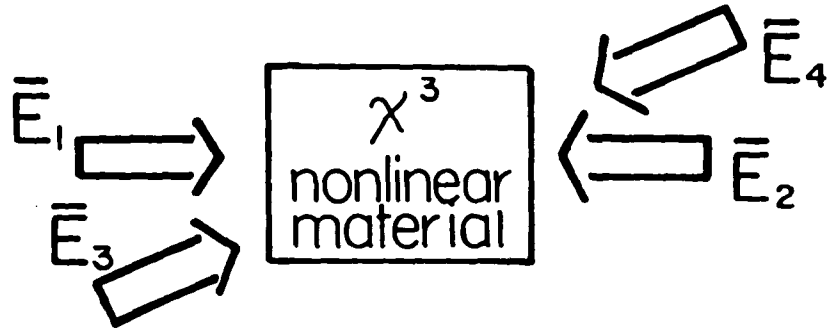

Fig.3.3.1 A schematic OPC geometry. Two counterpropagating beams $E_{1(2)}$ and a third beam E_3 are mixed in a third order nonlinear material to generate a fourth, a phase conjugate beam E_4.

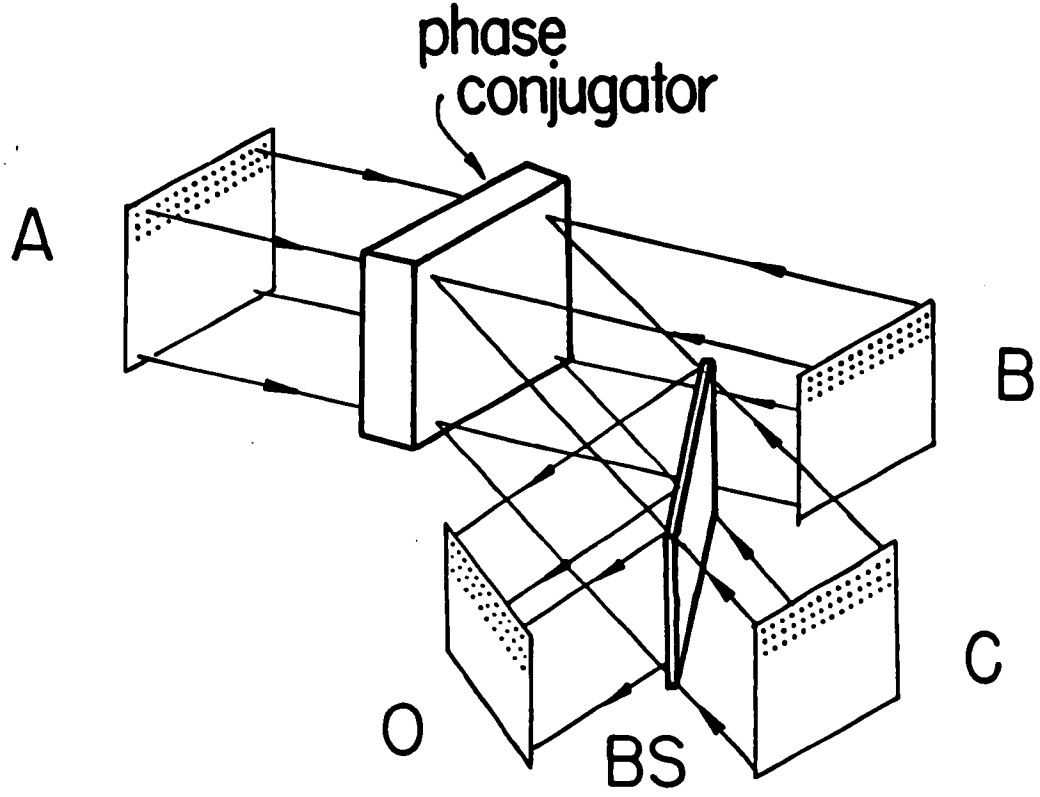

Fig.3.3.2 A schematic OPC-based parallel optical three-input binary AND gate array.

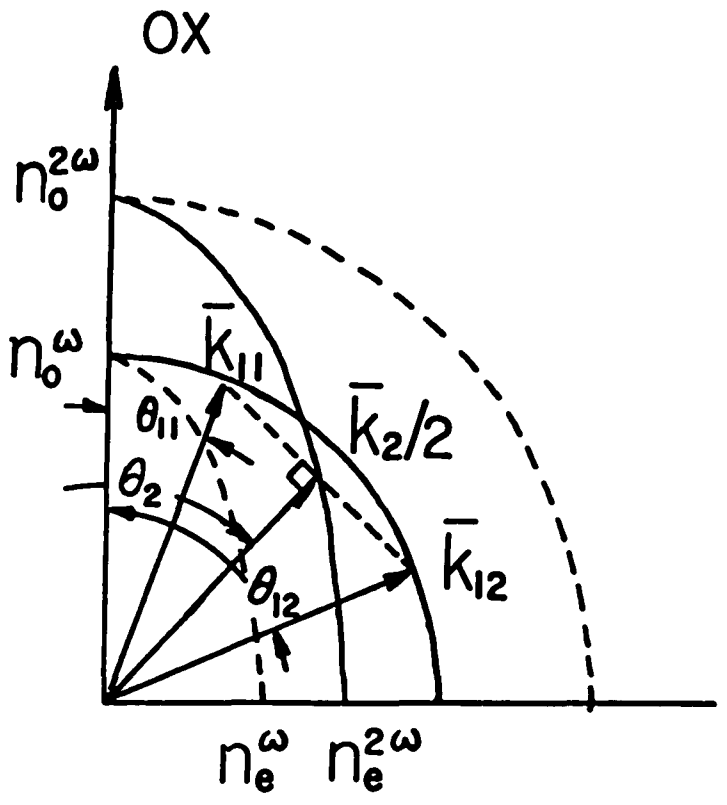

Fig.3.4.1 Index ellipsoidals and phase-matching diagram for a noncollinear SHG process. n_o and n_e denote the ordinary and extraordinary refractive index of the

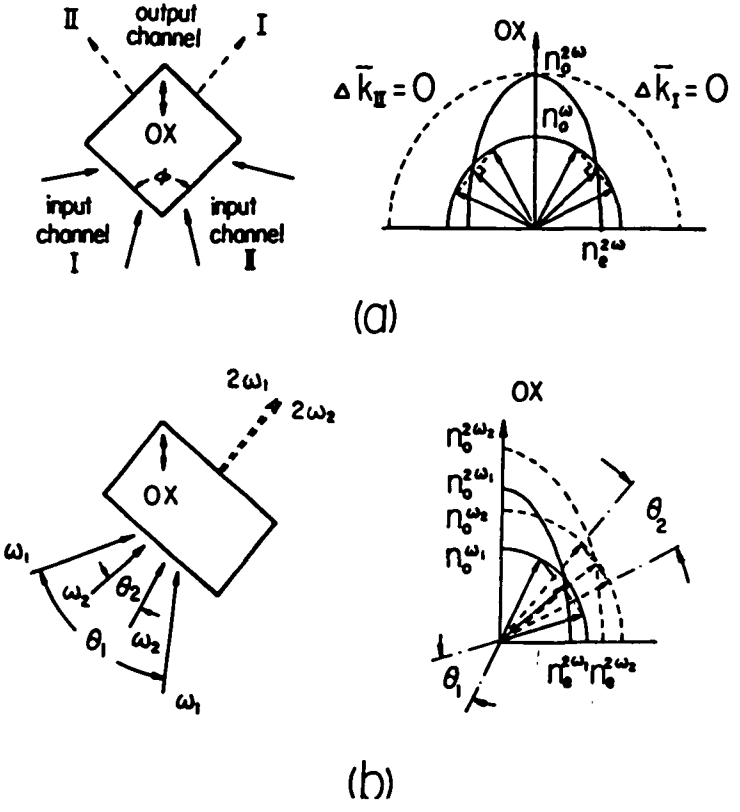

Fig.3.4.2 Using either (a) an angular, or (b) a frequency, multiplexing scheme, two SHG channels are processed in parallel.

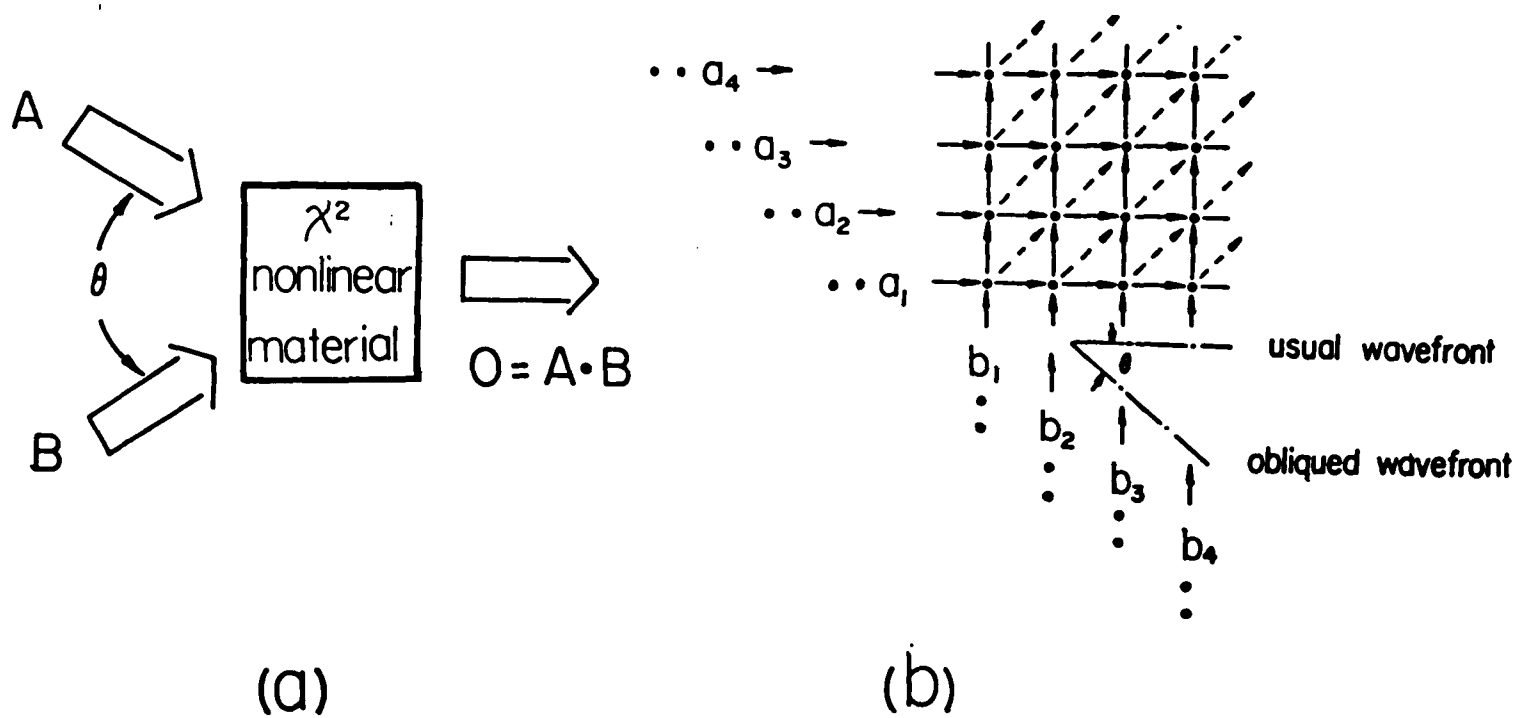

Fig.3.4.3 (a) A schematic SHG-based optical two-input binary AND gate. (b) With an oblique wavefront and spatially separated channels, an array of SHG AND operations is generated.

IV. SIS-BASED ULTRAFAST OPTICAL LOGIC ELEMENTS

4.1, Introduction

In this chapter, the use of the proposed fundamental Sagnac interferometric switch (SIS) to optical logic implementation[1-4] is described. With different SIS NLM placements, different optical binary as well as multiple-valued logic gates can be constructed. We begin our discussion with the constructions of a number of fundamental SIS-based binary logic switches. To solve the SIS output retroreflection problem, a modified version of SIS, a two-port SIS (TPSIS), will be used for binary logic implementations. Following this section, the use of TPSIS to synthesize various multiple-valued logic elements will be described. Finally, an additional nonlinear SI-based switching device, a SI Fabry-Perot (SIFP) resonator is proposed. The corresponding SIFP nonlinear bistability and multistability will be investigated.

4.2, SIS-based Optical Binary Logic Implementations

In this section, the formation of various binary optical logic elements using the SIS is discussed. We first describe implementations of the two-variable canonical switching elements, EXCLUSIVE-OR (EOR) and AND type SISs. These switches can be shown to take more than two logic variables. The parallel processing of different logic functions using only one SI element will also be discussed.

4.2.1, Two-variable optical logic elements

Table 4.2.1 shows all 16 possible two-variable binary logic functions. For our convenience, the table is not organized the same way as it usually appears in the logic textbooks. In the table, the symbols 0 and 1 represent false and truth values. Thus, positive

logic, i.e. bright intensity true logic, is used. The first six columns contain either the constants or the single-input logic functions. The optical implementation of an INV was discussed in the previous chapter. Columns 7 and 8 in Table 4.2.1 represent the EOR and the complement of EOR (ENOR) logic functions, respectively. Optical SIS implementation of EOR and ENOR is shown in Fig.4.2.1. The logic variables, beams A and B, are the two optical logic inputs. The beam R is an optical reference pulse. The initial optical intensity is chosen as a 0 (low energy) interference state [1,5]. When either of the input pulses A or B is turned on and temporally overlaps the counterclockwise reference beam at a NLM (either N_A or N_B), the reference pulse will be delayed by a half wavelength. This half wavelength delay leads the output to a 1 (high energy) state. However, when both beams A and B are turned on, the cumulative phase delay for the counterclockwise pulse is a 2π. This delay forces the output pulse to return to the previous 0 State. Therefore, for the input logic variables A and B, the output represents an EOR logic function. On the other hand, when one of the mirrors is slightly misaligned so that 1 is obtained as the initial output, this device represents an ENOR logic function.

Instead of working with one of the two counterpropagating beams, we can also let one logic input beam overlap the clockwise reference beam and the other logic input beam overlap the counterclockwise reference beam at the NLM[1]. Using this approach, when two NLMs are placed symmetrically in the SI, there is no time delay between the two logic input beams. To implement these two logic functions, another alternative is to time-code the two inputs in the same NLM. The NLM is placed asymmetrically into the SI, with the arrival time for the two inputs adjusted so that one input overlaps the counterclockwise reference pulse and the other overlaps the clockwise reference pulse at the NLM.

For the optical generation of the two-variable AND function, column 9 of Table 4.2.1, the optical circuit similar to the optical INV (see Fig.3.2.3) is used [1]. For an AND function, the reference R pulse is replaced by a signal pulse B (see Fig.4.2.2). Assume that the initial output, when beam A is on, is a 0. The only way to switch this output to a 1 is to

have both beams A and B on. Therefore, this SIS yields a two-variable logic AND function. Here we notice that, compared to the amplitude of signal A, the signal B is a primary input. When the value of B is a 1, depending on the initial SI mirror alignment and the value of A, the output can either be a 0 or a 1. However, when the value of B is a 0, the output stays permanently at 0. Therefore, when 1 is chosen as the initial output, the function ($\bar{A}$ AND B) is realized. The function (A AND $\bar{B}$) can be obtained simply by interchanging the order of two inputs.

The two-variable INCLUSIVE-OR (OR) operation, column 11 of Table 4.2.1, can be realized with a BS. When a BS is used to combine two coherent beams, it serves as an interferometer. For an OR logic function, the phase difference between two inputs A and B should be adjusted to such a value that when both A and B are on, the interference output is the same as the output when either one of the two inputs is on. The remaining four function, columns 13 through 16 in Table 4.2.1, can also be obtained using the SIS techniques. They can be synthesized using two canonical SIS elements, i.e. AND EOR INV, etc..

4.2.2, Multi-variable optical logic elements

The SIS logic elements can synthesize multivariable logic functions s-2[1]. To illustrate this process, we present a number of examples. As a first example, consider a three-variable logic function G:

$$G = A \oplus B \oplus C \tag{4.2.1}$$

where $\oplus$ stands for an EOR operation. To realize G, we add one more NLM and an additional signal pulse C to the original EOR switch (see Fig.4.2.3). Again, by adjusting the SI, a 0 initial output is obtained. When one or three of the inputs are 1, because of the odd multiple of π phase difference between two interference beams, the output is switched from a 0 to a 1. On the other hand, when two or none of the three inputs is a 1, the resultant phase difference is an even multiple of π; then, the output stays at 0. With an SIS, using similar reasoning, an N-input variable EOR operation can be performed.

As a second example, consider the generation of a three-variable AND function E :

$$E = A \bullet B \bullet C \tag{4.2.2}$$

where the $\bullet$ stands for the logic AND. In this case, two NLM cells are used (see Fig.4.2.4). The two NLM cells are illuminated with the signals B and C . For loop length compensation, a phase retardation plate (RP) is employed. A delay prism D, which adds a slight translational shift, is used to feed the output of the AND function ($A \bullet B$) back to the SIS. In this case, the two counterpropagating beams do not travel along the same loop. However, after traversing an identical optical distance, they recombine at a common point on the BS. After completing two round trips, this output yields the desired AND function. In principle, this method can generate an N input AND function.

By replacing the desired logic functions in displaced loops in a SI, optical parallel processing is possible. An example of this type of arrangement is shown in Fig.4.2.5. Here, eight input (A , B , C , U , V , X , Y , and Z) and three output (O_1, O_2 and O_3) logic variables are used. When low initial states are assumed, the three logic outputs are $O_1 = A \bullet Z$, $O_2 = B \bullet Y$, and $O_3 = C \bullet (U \oplus V \oplus X)$. In general, the number of outputs is equal to the number of primary inputs, i.e. A , B , and C in this example. The SI parallel processing not only reduces computing time but also aids in system synchronization. In SI parallel processing, when one of the mirrors suffers a small translational shift, all optical signals are identically delayed. This is an improvement over a series-connected system, in which the delays vary between different processing steps.

4.3, Two-port SIS (TPSIS) Based Optical Logic Implementations

In the previous section, the principle of a SIS to perform various logic functions was described. One advantage of the SIS is its auto-stabilization property[5]. However, when two or more SISs are cascaded, because the optical beams are retroreflected, optical isolators are needed. The use of these optical isolators can complicate system alignment and synchronization. In this section, we present a modified version of SIS, the two-port SIS (TPSIS). The

TPSIS is a solution to the retroreflection problem. An additional advantage of the TPSIS over a SIS is that there are two independent input-output channels.

4.3.1, An optical TPSIS

In Fig.4.3.1(a), a schematic diagram of an optical TPSIS is shown. The input and output beams are denoted as I_1, I_2 and O_1, O_2, respectively. The beam S is the optical switching signal. The optical components are a non-polarizing 50/50 beam splitting ratio beamsplitter (BS), a polarizing beamsplitter (PBS) that transmits a linear and reflects its orthogonally-polarized beam counterpart, and a half-wave plate (H) whose fast axis is oriented at an angle 45° with respect to the input polarization direction resulting in an orthogonal linear polarization between the input and output beams. Similar to the SIS, a nonlinear material (NLM) is placed asymmetrically in the interferometer so that for the two counterpropagating beams, the delay times needed to traverse the distance between the BS and the NLM are different. To avoid four-wave-mixing effect, this time difference must be greater than the correlation curve width between the inducing pulse and material orientational relaxation times[4]. When the optical signal S is off, the two counterpropagating beams traverse identical optical path. At the BS, one of the beams undergoes an additional air-glass-air reflection, the interferometer output is retroreflected[5,6]. Because H plate forces the output polarization to be orthogonal to that of the input direction, the PBS separates the retroreflected beams. When the optical signal S is on and is polarized parallel to either input I_1 or I_2 beam polarization, it is adjusted so that it arrives at the NLM simultaneously with the clockwise traveling beam and with an intensity that provides an induced π phase shift to the clockwise traveling beam. Because of the asymmetrical NLM placement, the counterclockwise traveling beam does not probe this induced π phase shift. Therefore, there is an intensity induced π phase imbalance for the two counterpropagating beams arriving at the BS. This intensity induced imbalanced π phase shift, together with the BS induced π phase shift, leads to constructive (destructive) interference state of the output O_2 (O_1) for the input I_1, or of the output O_1 (O_2) for the input I_2. Thus, the input energy will switch from I_1 (I_2)

to O_2 (O_1). Thus, using a TPSIS with polarization as an aid, an intensity switching is performed. Notice that the intensity induced π phase imbalance can also be obtained using an orthogonally polarized pump beam. However, an additional inducing power is required[6]. Since the polarization states between the TPSIS inputs and outputs are mutually orthogonal, a PBS can be used to isolate the outputs from the inputs. A distinct property of the TPSIS is the absence of retroreflections toward the input sources. Therefore, no additional optical isolation is needed.

Often a two-port switch, with two input-output channels controlled by a single switching signal, is required. An example, where the switching signal is an electrical voltage, is the two-port e-o waveguide[7]. In Fig.4.3.1(b) the schematic diagram of an e-o waveguide switch is depicted. To perform all-optical switching, the electrical voltage must be replaced by an optical signal. One way of realizing an all-optical two-port switch is to use a TPSIS. Similar to Fig.4.3.1(b), the TPSIS can be resketched as in Fig.4.3.1(c). Here, the input and output terminals are drawn separately. Both input-output channels are identical. Thus, a TPSIS is more functionally flexible.

Before a functional description of various logic elements are presented, a short discussion on the optical interconnect between TPSIS stages is in order. First, because of the orthogonal polarization states between the TPSIS input and output signals, interconnections of two TPSIS requires the polarization matching. This matching can be performed in different ways. One way is to use a H plate at a TPSIS output to force the input and output polarization directions to be identical. To cascade N TPSISs, this method requires N additional H plates. To reduce the number of H plates, matched TPSIS pairs can be used. Here, the second TPSIS takes, as the input, the orthogonally polarized signal (relative to the first TPSIS input polarization), and generates an identical (relative to the first TPSIS) polarization output. Therefore, no additional cascading H plates are needed. This concept will be used in the subsequent TPSIS interconnection examples. Another important TPSIS interconnection factor is the interconnect power. Since both binary logic and arithmetic operations

usually require the use of a number of interconnected logic gates, the output power requirement (fan out), needed for the subsequent switches, is an important quantity. One advantage of an interferometric switch is that its output state is determined by the phase difference between interfering beams. When the phase difference is a multiple order of 2π (regardless of the source) the same output state (not the output power) is obtained. This fact has been demonstrated with an all-optical transistor[8], where using a nonlinear etalon, a strong beam serves as a reference beam and the etalon is tuned so that its output is in a low energy state. The beam to be amplified is a weak beam. However, when the energy of the weak beam is added to that of the strong beam, the total energy reaches a critical etalon switching energy and that the output switches to a high energy state. Similarly, in a TPSIS, a strong reference beam and a weak switching input signal can be used so that when both of them are in the high energy state, the output state can have enough optical power to drive subsequent switches. In the following discussion, whenever cascading of elements is required, this concept may be applied.

4.3.2, TPSIS-based optical binary logic elements

In the previous section, the operation of a TPSIS was described. To perform optical switching, either channel can be used. Similar to an SIS, the TPSIS can be viewed as a binary logic INV. In Fig.4.3.2(a), the identically polarized optical inputs A and R, where A is an input logic and R is an interferometric reference beam, are shown. The A beam low and high energy states are represented by two positive (bright true) logic values: zero and one, respectively. When the beam A is a zero, the input reference beam R is retroreflected and is separated by the TPSIS to channel O_1. When the beam A is a one, its output is switched to channel O_2. Therefore, for the binary input A, the channels O_1 and O_2 display logic variables $\bar{A}$ and A, where the bar denotes logic inversion. Similarly, when the reference beam R is named as the binary logic variable B, the channels O_1 and O_2 display the logic functions $\bar{A} \bullet B$ and $A \bullet B$, where $\bullet$ denotes the logic AND function[4]. When a beamsplitter is used to combine two beams, this combination yields an optical OR

element. Here, when neither of the two input beams is on, the zero logic output (low energy state) occurs.

Next, a TPSIS implementation of an EOR gate is considered. In Fig.4.3.2(b), two cascaded NLMs are placed in the TPSIS loop. The NLMs are interrogated by the two logic inputs A and B. For identical logic values, the corresponding results for the two input channels are logic one for O_1 and logic zero for O_2. For opposite logic values, the logic values zero (one) for channels O_1 (O_2) are obtained. Thus, at the output channels O_2 (O_1), the logic functions EOR and its complement are generated[4].

Now, the generation of a canonical optical binary NAND function is described. Since the logic NAND gate is an universal element[9], from the combination of these gates any binary logic function can be synthesized. A two input binary NAND function is defined as

$$NAND\ (A, B) = \overline{A \bullet B} = \bar{A} + \bar{B} \qquad (4.3.1)$$

where symbol + denotes an OR gate. As per Eq.(4.3.1), there are two, each involving two steps, ways to realize an optical NAND logic function. Either the AND of two inputs is logically inverted, or these logic inputs are first inverted and then combined by an OR gate. Because with our method it is easier to implement an OR than an AND function, we prefer to use the second approach, i.e. first to generate two NOT functions for two inputs using a TPSIS, and then to combine the signals with a beamsplitter. In Fig.4.3.2(c), using the parallel processing property of TPSIS, a schematic diagram of the two input optical TPSIS NAND gate is shown. Here, A and B beams are two logic inputs. The logic variable $\bar{A}$ and $\bar{B}$ are obtained in parallel at the output of the TPSIS. The two inverted signals are then combined, using a BS, to yield the function A NAND B.

4.3.3, TPSIS-based optical multiple-valued logic generations

Recently, there has been a revival of interest in non-binary optical computing.

Among various proposed multiple valued computation structures it is ternary logic; logic that uses three logical values[10], that has received the most interest. In this section, optical implementations of ternary Post and Residue as well as the universal Webb logic functions using a number of TPSISs will be discussed.

A ternary number is an ordered string of symbols a_j, where $a_j \in (0, 1, 2)$. such a set is usually called an ordinary ternary set[11]. Other ternary value set, such as the balanced ternary set with values $(-1, 0, 1)$, is also available. Here, the ordinary ternary set is used. To represent optically the value of a ternary number, various methods can be used. In a pulse-position coding method (see Refs.12), each ternary value is represented by a spatially coded light spot. Therefore, to represent a ternary value three spatial channels are employed. To reduce the channel number and thus to accommodate a compact ternary logic and arithmetic processor, another PPC method, a binary coded ternary PPC (BCT PPC) method can be used. Here, the ternary representation takes only two channels. In general, to represent a number in a modulo N (usually N is a prime integer) logic system, a number of $\log_2 N$ binary channels are required. The encoding of the ternary set into binary values can take on different forms. In our discussion, a BCT representation is chosen as

$$\begin{aligned} 0t &= [0, 0] \\ 1t &= [1, 0] \\ 2t &= [1, 1] \end{aligned} \qquad (4.3.2)$$

where the letter "t" denotes the ternary value. Therefore, for TPSIS implementation, each ternary bit is represented by a set of two binary spatial light channels.

In Post logic, the logic functions called MIN and MAX are used[13]. In the truth table of Fig.4.3.3(a), the ternary MIN, the analog of the AND function, is defined. Using BCT, instead of direct generating the ternary logic function f, a set of two binary logic output functions f_1 and f_2 are produced. In Fig.4.3.3(b), the corresponding BCT value truth table is shown where x_{ij} $(i, j = 1,2)$ is the j^{th} bit of the i^{th} input, and f_i, $i = 1,2$ is the

i^{th} bit output of the MIN gate. After the logic simplification, using Karnaugh maps, the two channel binary MIN logic functions of can be represented as

$$f_1 = x_{11} \bullet x_{21} \tag{4.3.3a}$$
$$f_2 = x_{12} \bullet x_{22} \tag{4.3.3b}$$

The optical implementation of the ternary MIN logic function is thus decomposed into generating two parallel binary AND functions. In Fig.4.3.3(c), a schematic diagram of the four input and two output ternary optical MIN logic function is shown.

A second Post logic is the MAX, an analog of the OR, function. In Figs.4.3.4(a and b), ternary and BCT value MAX logic truth tables are shown. The notation follows the previous example's convention. The two logic-reduced BCT MAX output functions f_1 and f_2 are

$$f_1 = x_{11} + x_{21} \tag{4.3.4a}$$
$$f_2 = x_{12} + x_{22} \tag{4.3.4b}$$

Thus, a binary optical circuit two BS OR gates can realize this ternary logic function. In Fig.4.3.4(c), this implementation is shown.

Similarly, other BCT logic functions, such as unary operators succession (SUC), negation (NEG), and literal (LIT) operators, the universal Webb as well as residue logic operators can also be optically generated. For each function, first, a BCT truth table is produced. After logic simplification, a set of binary logic functions can be obtained which can be implemented using the proposed SIS elements. In Table 4.3.1, the reduced BCT expressions for these logic functions are included. Correspondingly, in Figs. 4.3.5 through 7, the truth tables and the TPSIS-based BCT SUC, NEG, and LIT implementations are presented.

4.4, SI-based Multistable Resonator For Optical Logic

Since a passive SI is a highly mechanically autostablized device, it can be used as an optical retro-reflector. In this section, we propose another SI application to optical logic

switching. Specifically, we will investigate the switching multistability of an Fabry-Perot (F-P) etalon that consists of a SI as its end reflector[14]. In convenience, a term SIFP is used to represent the proposed device. The multistable switching phenomena of the proposed SIFP can be used to perform various digital, such as logic and memory, operations.

4.4.1, SIFP - an equivalent optical Fabry Perot cavity

In Fig. 4.4.1(a), an SIFP with three mirrors (M_i, i =1,2,3) and a beam-splitter (BS) and with wave direction-dependent amplitude transmission and reflection coefficients as t_j (t'_j) and r_j (r'_j) with j =1, b , and with round-trip phases for the co-linear, the clockwise (counterclockwise) SI sections as δ_l , δ_{s1} (δ_{s2}), respectively, is depicted. In Fig.4.4.1(b), an equivalent FP for this SIFP is shown.

The SI complex amplitude transmittance and reflectance, denoted as $\tilde{t}_s$ and $\tilde{r}_s$, are[15]

$$\tilde{t}_s = r_2 r_3 (t_b^2 e^{i\frac{\Delta\delta_s}{2}} - r_b^2 e^{-i\frac{\Delta\delta_s}{2}}) e^{i\bar{\delta}_s} \tag{4.4.1}$$

$$\tilde{r}_s = 2 r_2 r_3 r_b t_b \cos\frac{\Delta\delta_s}{2} e^{i\bar{\delta}_s} \tag{4.4.2}$$

where the average SI counterpropagating wave phase and phase difference are $\bar{\delta}_s = (\delta_{s1} + \delta_{s2})/2$ and $\Delta\delta_s = \delta_{s1} - \delta_{s2}$, respectively. The corresponding SI intensity transmittance (T_s) and reflectance (R_s) are

$$T_s = |\tilde{t}_s|^2 = R_2 R_3 - R_s \tag{4.4.3}$$

$$R_s = |\tilde{r}_s|^2 = 4 R_2 R_3 R_b T_b \cos^2\frac{\Delta\delta_s}{2} = R_{sm}\cos^2\frac{\Delta\delta_s}{2} \tag{4.4.4}$$

where R_{sm} is the maximum SI intensity reflectance. In agreement with Ref.15, for unity intensity reflectance for both R_2 and R_3 and $R_s = T_s = 0.5$, Eqs.(4.4.3) and (4.4.4) become zero and one, respectively.

For the SIFP, the equivalent amplitude transmission (t) and reflection (r) coefficients are

$$t = \frac{E_t}{E_i} = \frac{t_1 \tilde{t}_s \, e^{i\,\delta_l/2}}{1 - r_1 \tilde{r}_s \, e^{i\,\delta_l}} \quad ; \qquad r = \frac{E_r}{E_i} = \frac{r'_1 + \tilde{r}_s \, e^{i\,\delta_l}}{1 - r_1 \tilde{r}_s \, e^{i\,\delta_l}} \tag{4.4.5}$$

Using Eqs.(4.4.1)-(4.4.5), the SIFP intensity transmittance (T) and reflectance (R) are

$$T = |\,t\,|^2 = \frac{A}{1 + F \, \sin^2(\delta_T / 2)} \tag{4.4.6}$$

$$R = |\,r\,|^2 = \frac{B + F \, \sin^2(\delta_T / 2)}{1 + F \, \sin^2(\delta_T / 2)} \tag{4.4.7}$$

where

$$F = \frac{4\sqrt{R_1 R_s}}{(1 - \sqrt{R_1 R_s})^2} \quad ; \tag{4.4.8}$$

$$A = \frac{(1 - R_1)(R_2 R_3 - R_s)}{(1 - \sqrt{R_1 R_s})^2} \tag{4.4.9}$$

and

$$B = \left| \frac{\sqrt{R_1} - \sqrt{R_s}}{1 - \sqrt{R_1 R_s}} \right|^2 \tag{4.4.10}$$

where the total round-trip phase is $\delta_T = (\delta_l + \bar{\delta}_s)$. For the SIFP, in addition to a total round-trip phase δ_T, because of the use of R_s, both T and R also depend on the SI beam counterpropagating phase difference $\Delta\delta_s$. Similar to an active FP, an intensity-dependent nonlinear refractive material (NLM) can be used to modulate both R_s and T (R) leading to an intensity-dependent cavity round-trip phase. The intensity-dependent round-trip phase, in turn, changes the cavity transmittance (reflectance) and results in multistable behavior of the equivalent FP cavity.

4.4.2, An active optical SIFP

A passive SI is a mechanically stable device. However, the use of intensity dependent nonlinear materials within the SIFP can cause the device to be optically multistable. Since different NLM placements in a SIFP can cause completely different transmission (reflection) effects, two different cases need to be considered. First, let the average SI phase $\bar{\delta}_s$ be fixed while the co-linear section phase δ_l vary. Because now the two SI counterpropagating waves traverse identical optical path, the SI phase difference is zero or $\delta_{s1} = \delta_{s2}$. Thus, from Eq.(4.4.4), $R_s = R_{sm}$ is fixed. This is similar to a co-linear FP case. Since the parameters R_2 and R_3 are not always equal to unity, in Eq.(4.4.9), instead of the usual co-linear factor $(1 - R_s)$ the factor $(R_2R_3 - R_s)$ is used. This replacement causes the SIFP transmission modulation to be lower than that of the corresponding FP. For an equal-ratio BS, the power transmission of Eqs.(4.4.6 and 9) reduces to zero, while for a non-equal-ratio BS, transmission (reflection) expressions are similar to a conventional FP expressions. Thus, further discussions on its characteristics are omitted.

Next, we let the co-linear phase δ_l be fixed while we vary, with the pump intensity, the average phase $\bar{\delta}_s$. Because the two SI counterpropagating beams now traverse different optical paths, the SI phase difference is nonzero. As the phase difference $\Delta\delta_s$ changes, R_s oscillates between its maximum value R_{sm} and zero. This configuration is equivalent to a co-linear FP with a single fixed and a variable reflectance mirror. By inserting a cubic optical NLM in the SI loop, i.e. $n = n_0 + n_2 \langle E^2 \rangle$, and using an non-equal-ratio BS, an intensity-dependent non-zero phase difference $\Delta\delta_s$ can be obtained [6,16]. Substituting in Eqs.(4.4.6 and 7) the relations

$$\delta_T = \delta_{T0} + \Delta\bar{\delta}_s \tag{4.4.11}$$

$$\Delta\delta_s = (2R_b - 1)\,\Delta\bar{\delta}_s = (2R_b - 1)\,\frac{2\pi L}{\lambda}\,n_2 \langle E^2 \rangle \tag{4.4.12}$$

where δ_{T0}, $\Delta\bar{\delta}_s$ and L are the initial total round-trip phase, the SI average phase change

and the NLM cell length, respectively, results in an intensity-dependent SIFP transmission (reflection) curve. While with a FP tuning either the mirror reflectance or the initial resonator phase either affects the transmission modulation depth or translates the transmission curve, with a SIFP, because of different sine- and cosine-square function frequencies and initial phases in Eqs.(4.4.4, 6 and 7), the corresponding tuning can result in radically different curves.

As examples, in Figs.4.4.2(a,b and c), three sets of the SIFP transmission versus input intensity curves, with different adjustable parameters R_1, R_b and δ_{T0}, are shown. In Fig.4.4.2(a), the effect of changing the front mirror reflectance R_1 is shown. For large R_1, because in each period the peaks of the two off-center resonances are higher than the center resonance peak there are two dominant transmission regions. These multiple resonances are due to competitions between different sine- and cosine-square phase functions. Also, because of multiple-beam interference, the resonance bands are relatively narrow. As R_1 decreases, the resonance curve broadens and the center (side) transmission gradually increases (decreases). As R_1 approaches zero, in agreement with Ref.6, the off-center peaks recede yielding a single SI sinusoidal transmission curve. By varying the BS reflectance R_b, the curves of Fig.4.4.2(b) are obtained. Two extreme cases, when R_b is equal to 0.0 (1.0) and 0.5 (a equal-ratio BS), are of interest. In the former case, a constant bias $(1 - R_1)R_2R_3$ curve is obtained indicating, that in this case, there is no interference effect. For a balanced (equal-ratio) BS, because on both sides of the NLM the SI incident intensities are identical, the SI phase difference is zero and, therefore, $R_s = R_{sm}$ is fixed. Although the intensity-dependent round-trip SI phase $\bar{\delta}_s = \delta_{s1} = \delta_{s2}$ does vary, independent of δ_T, $(R_2R_3 - R_s)$ is always equal to zero. Correspondingly, the SIFP transmission also reduces to zero. Thus, except for a change in geometry, the above two special cases belong to a FP category. In Fig.4.4.2(c), the effect of varying the initial phase δ_{T0} is illustrated. Unlike a FP, where a change of the initial phase translates the transmission curve, here, a change in the initial phase, because it only affects the sine-square function, modifies the transmission

curve.

4.4.3, Intensity multistability of a SIFP

To study resonator multistability phenomena, the SIFP transmission (reflection) curves of Fig.4.4.2 are utilized. Using the Felber and Marburger (F-M) method, taking transmission as an example, Eq.(4.4.6) is interpreted as a solution of two simultaneous equations where the left hand side is a linear equation with a fixed slope as a function of input intensity while the right hand side is the nonlinear intensity-dependent transmission curve [17]. For a given slope, wherever multiple intersections of two curves can be found, multistable intensity transmissions may exist. When a pump beam illuminated co-linear section NLM is used, the corresponding multistable SIFP operations exhibits the same characteristics as does the usual co-linear FP. For this case both experimental and theoretical results are available [18,19]. When a pump beam illuminated SI section NLM is used, different multistable operation is expected. In Fig.4.4.3(a), indicated by the solid line, two cycles of a Fig.4.4.2(b) SIFP transmission curve is shown. The horizontal and vertical axes represent the input intensity and SIFP intensity transmittance, respectively. Initially, indicated by the intersection between the transmission curve and the vertical coordinate, the SIFP is in a low transmission state. Increasing the input intensity decreases the slope of the straight-line. The intersection then gradually moves up toward a point a where the straight line is tangent to the nonlinear curve. Correspondingly, the output intensity slowly increases. By increasing the input intensity (a further decrease in the straight line slope), a second intersection between the straight line and the nonlinear curve is sought. The closest intersection to a is the point b which is the next transmission state. Increasing the input intensity until the intersection reaches another tangential point c results in a slowly increasing output intensity. Past intersection c, another sudden jump brings the transmission state to a new intersection d resulting in another output intensity jump. Similarly, by continuously decreasing the input intensity the intensity-dependent transmission is forced to change from point e through n, and finally reaches a zero output

intensity state. In Fig.4.4.3(b), the corresponding multistable intensity discontinuities are illustrated. The first (second) switch-on threshold input intensities are labeled as I_{on1} (I_{on2}), respectively. To obtain bistability, the input intensity should be below I_{on2}. For input intensities larger than I_{on2}, a number of output intensity levels can be probed. In principle, a SIFP and the nonlinear antiresonant ring interferometric switch proposed by Ref.6 have the same switching power requirement. In both devices, using an identical NLM, the switching power depends on the BS intensity transmittance (reflectance). The larger the imbalance between the values of the BS intensity transmittance and reflectance, the less the switching power is required. To lower the switching power requirement, materials with a large nonlinearity must be used. However, some large nonlinearity materials can have a severe carrier diffusion problem. For example, because the diffusion length is 60 μm in a InSb [20], nonlinear index modulation of a period less than this length will be washed out. To overcome the diffusion problem, the use of multiple-quantum-well semiconductor materials may be helpful[21]. It has been reported that semiconductor-doped glasses can produce large, fast and diffusion-free optical third order nonlinearities[22].

4.4.4, SIFP applications to optical logic

Finally, compared to a nonlinear FP, a nonlinear multistable SIFP is a flexible device with several additional adjustable parameters. In Fig.4.4.4(a), an optical SIFP device is shown. The NLM may be placed in either one of two possible locations. With this device, in addition to the primary (cavity) input beam A, using differently placed NLMs other external incident beams, i.e. B, C, D or E can also be used. As the overall inducing intensity exceeds the first switch-on threshold, both hysteretic and non-hysteretic bistabilities are obtainable. While a hysteretic bistability is suitable for optical memory and sequential logic operations, for asynchronous logic operation, a non-hysteretic bistability can be used to implement an optical limiter or a switch. The use of higher input intensities can cause SIFP multistable outputs. The tuning of initial phase, and other parameters such as BS reflectivity, can totally change the transmission curve. Properly choosing these parameters

leads to different multistable operations. A SIFP multistability application is multistable optical switching. A combination of different SIFP multistabile operation modes may help in the design of multiple-valued optical logic and arithmetic computing elements. In Fig.4.4.4(b), four possible SIFP characteristic curves together with their applications are illustrated.

4.5, Summary

In this chapter, based on a Sagnac interferometer, various optical logic implementation schemes were proposed. First, using different NLM placements in a SI loop, the constructions of optical binary INV, AND EOR and its complement were described. With different combinations of these gates, all 16 two-variable binary logic functions were synthesized. A problem with this basic scheme is that part of the logic signals is retroreflected. To alleviate the beam retroreflection problem, the TPSIS was then introduced. The TPSIS is able to perform two-port binary all-optical switching. The use of the TPSIS to both binary and multiple-valued optical logic were discussed. Finally, another alternative logic switching device (a SIFP) was proposed. To implement a SIFP, in addition to an elemental SI, a feed-back mirror is also employed. By properly adjusting the SIFP mirror and beamsplitter reflectivity and the cavity round-trip phase, intensity dependent multistable switching phenomena were investigated. The applications of the SIFP include optical limiting, amplifying, binary and multiple-valued logic switching, as well as optical memory.

4.6 References

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A	B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	1	0	0	1	1	0	1	0	0	0	0	1	1	1	1
0	1	0	1	0	1	1	0	1	0	0	0	1	1	0	1	1	0
1	0	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1	0
1	1	0	1	1	1	0	0	0	1	1	0	0	1	1	1	0	0
		0	1	A	B	$\bar{A}$	$\bar{B}$	$A \oplus B$	$\overline{A \oplus B}$	$A \cdot B$	$A \cdot \bar{B}$	$\bar{A} \cdot B$	$A + B$	$A + \bar{B}$	$\bar{A} + B$	$\overline{A + B}$	$\overline{A \cdot B}$

Table 4.2.1 A list of all sixteen two-input binary logic functions.

Minimum	$MIN(x_1,x_2)$	$= x_1$ if $x_1 \leq x_2$	$f_1 = x_{11} \cdot x_{21}$	$f_2 = x_{12} \cdot x_{22}$
Maximum	$MAX(x_1,x_2)$	$= x_1$ if $x_1 \geq x_2$	$f_1 = x_{11} + x_{21}$	$f_2 = x_{11} \cdot x_{12} + x_{21} \cdot x_{22}$
Succession	$SUC(x_i)$	$= (x_i + 1) \bmod 3$	$f_{i1} = \overline{x_{i2}}$	$f_{i2} = x_{i1} \cdot \overline{x_{i2}}$
Negation	$NEG(x_i)$	$= (2 - x_i) \bmod 3$	$f_{i1} = \overline{x_{i2}}$	$f_{i2} = \overline{x_{i1}}$
Literals	${}_a X_b$	$= \begin{cases} 2 & \text{if } a \leq x \leq b \\ 0 & \text{otherwise} \end{cases}$	${}^0X_1^0 = {}^0X_2^0 = \overline{X_1}$	${}^0X_1^1 = {}^0X_2^1 = \overline{X_2}$
			${}^0X_1^2 = {}^0X_2^2 = 1$	${}^1X_1^1 = {}^1X_2^1 = X_1 \cdot \overline{X_2}$
		$(a,b) \in 0,1,2$	${}^1X_1^2 = {}^1X_2^2 = X_1$	${}^2X^2 = {}^2X^2 = X_2$
Summation (mod 3)	$SUM(x_1,x_2)$	x_1 \ x_2: 0 1 2 / 0: 0 1 2 / 1: 1 2 0 / 2: 2 0 1	$f_1 = x_{11} \oplus x_{21} + x_{12} \cdot x_{22} + x_{11} \cdot \overline{x_{12}} \cdot \overline{x_{22}}$	
			$f_2 = x_{12} \cdot \overline{x_{21}} + \overline{x_{11}} \cdot x_{22} + x_{11} \cdot \overline{x_{12}} \cdot x_{21} \cdot \overline{x_{22}}$	
Product (mod 3)	$PRO(x_1,x_2)$	x_1 \ x_2: 0 1 2 / 0: 0 0 0 / 1: 0 1 2 / 2: 0 2 1	$f_1 = x_{11} \cdot x_{21}$	
			$f_2 = x_{11} \cdot \overline{x_{12}} \cdot x_{22} + x_{21} \cdot \overline{x_{22}} \cdot x_{12}$	
Webb	$WEB(x_1,x_2)$	x_1 \ x_2: 0 1 2 / 0: 1 0 0 / 1: 0 2 0 / 2: 0 0 0	$f_1 = f_2 + \overline{x_{11}} \cdot \overline{x_{21}}$	
			$f_2 = x_{11} \cdot x_{21} \cdot \overline{x_{12}} \cdot \overline{x_{22}}$	

Table 4.3.1 Various useful ternary Post, Webb and Residue logic functions and their reduced BCT representations.

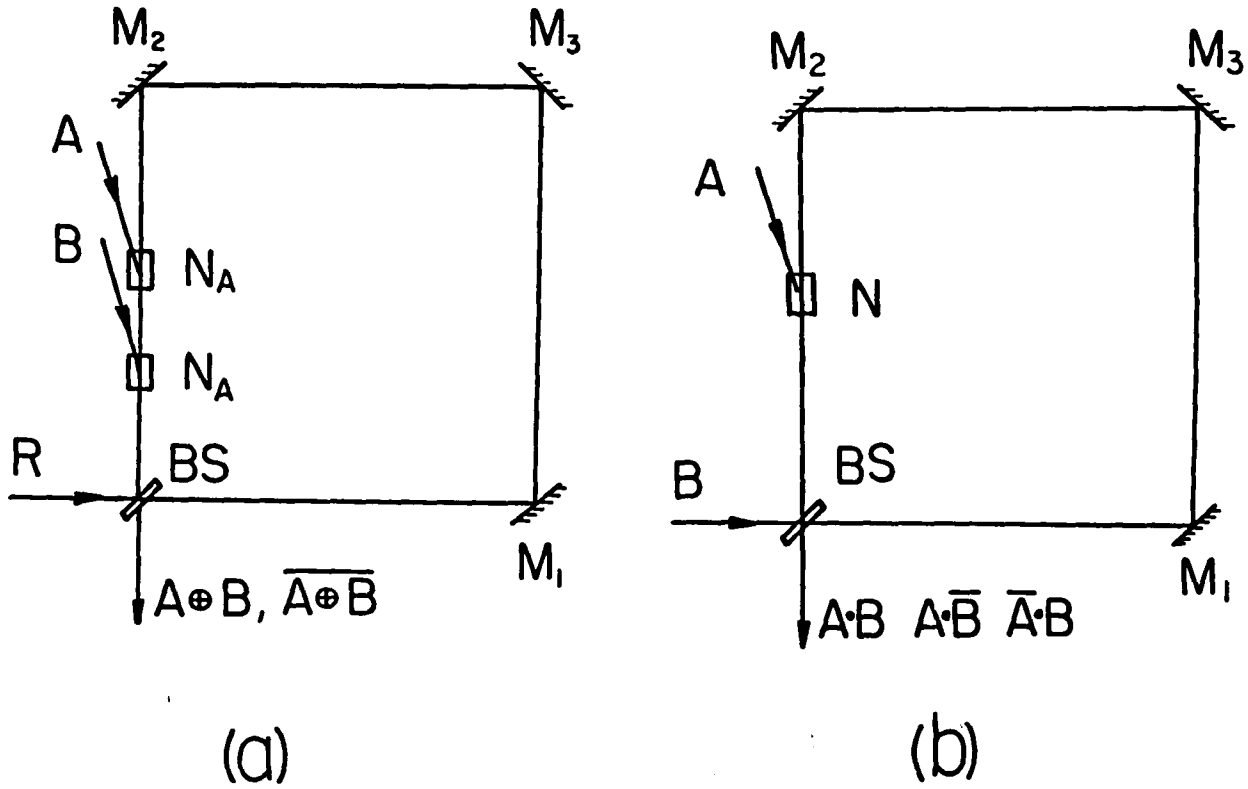


Fig.4.2.1 Schematic diagrams of optical SI-based two-input binary (a) EOR and (b) AND switches. With tilted BS, other logic elements can also be implemented.

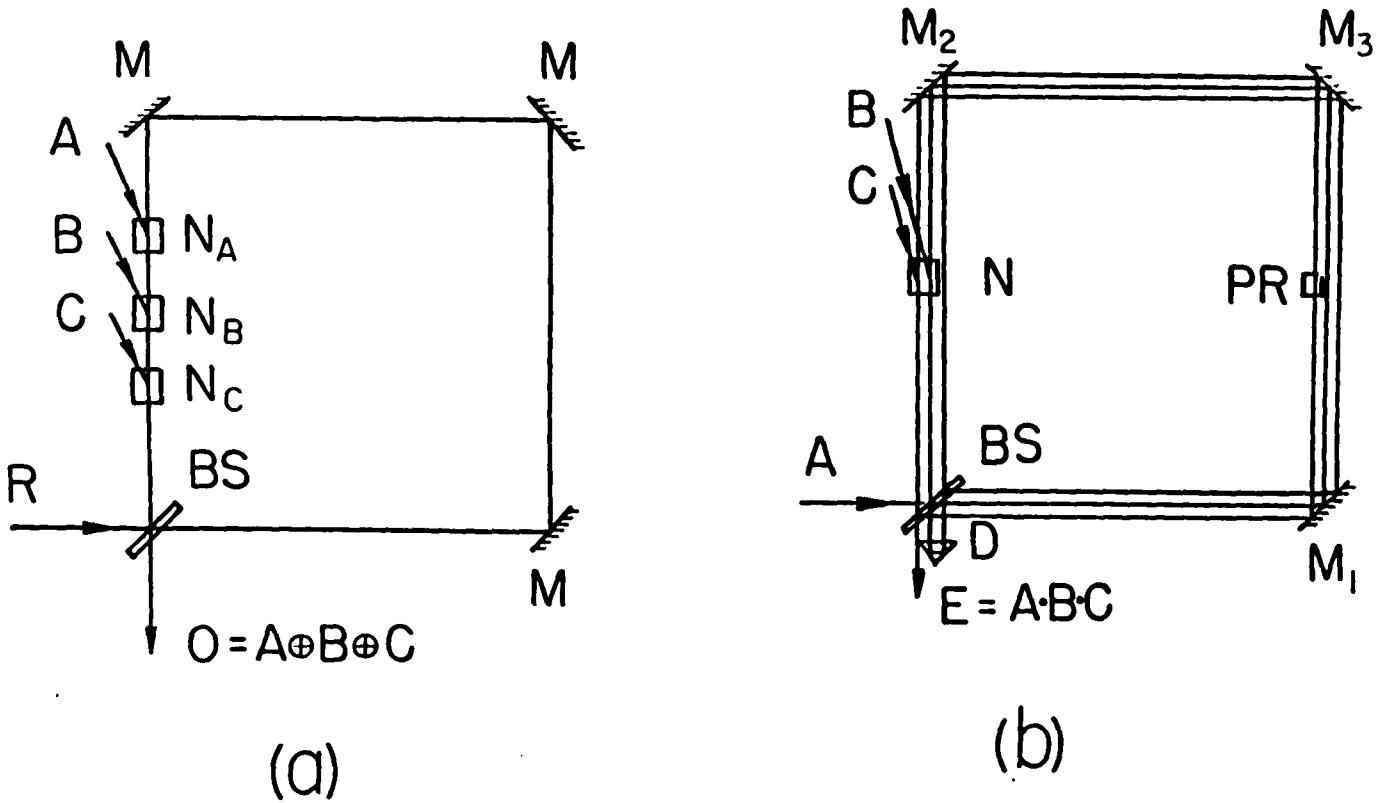


Fig.4.2.2 Optical SI implementations of three-input binary (a) EOR and (b) AND switches. D, delay prism; and PR, retardation plate.

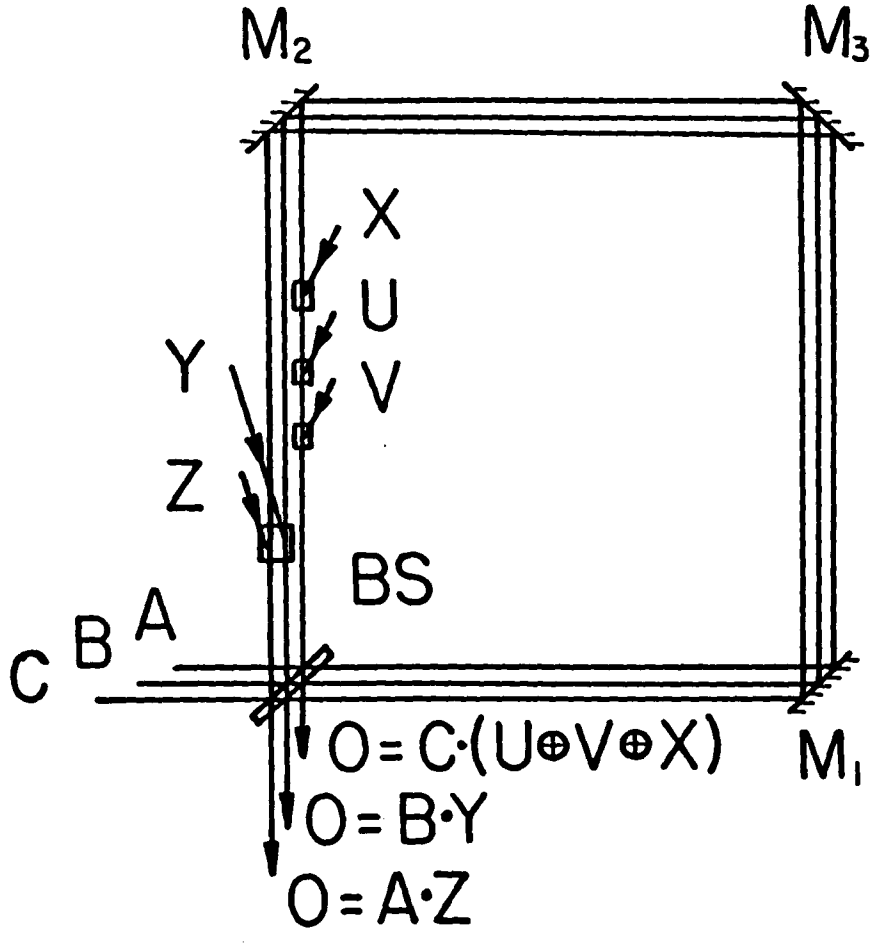


Fig.4.2.3 Parallel processing of three logic functions using a single SL

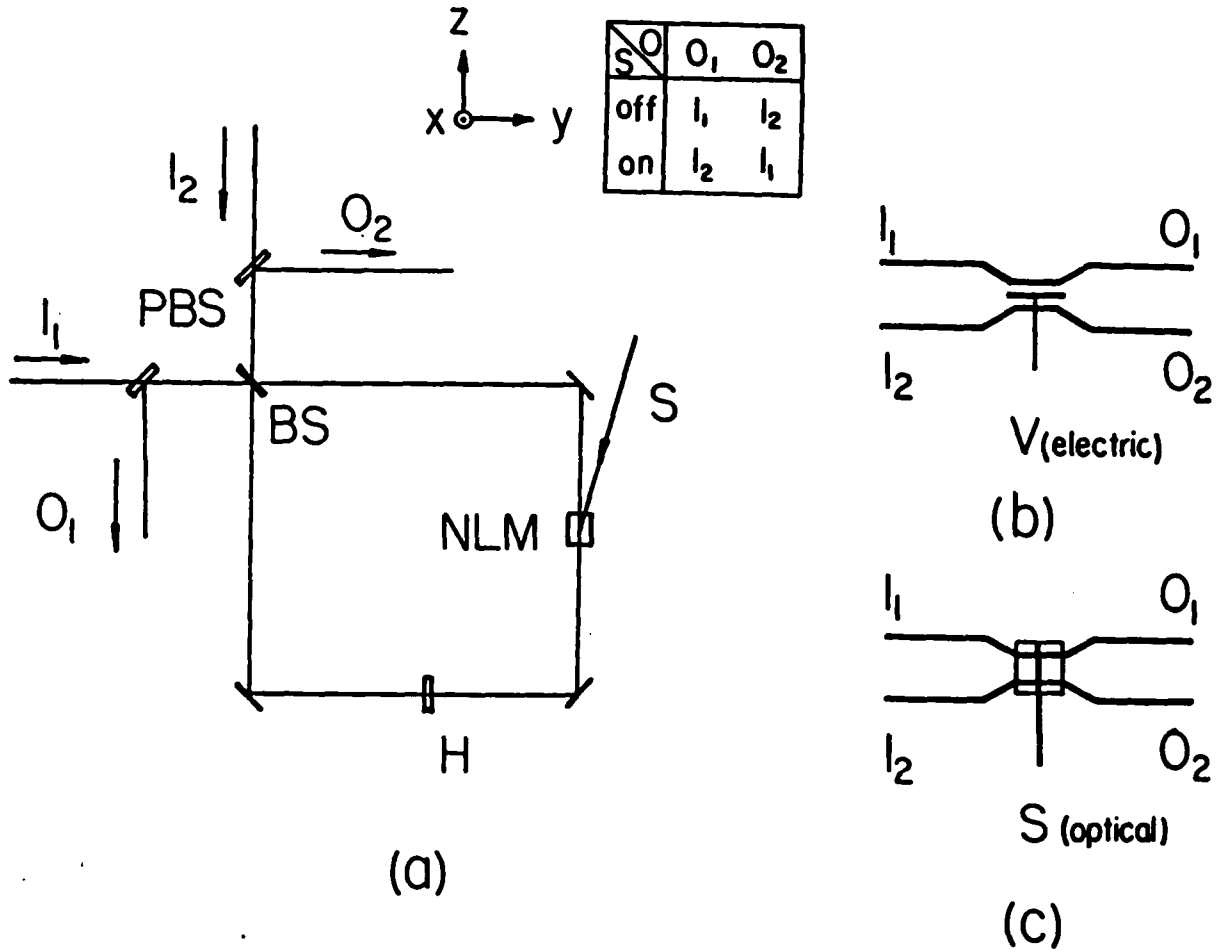


Fig.4.3.1 (a) Schematic diagram of an optical TPSIS. PBS, polarizing BS; H, half wave plate. $I_{1,2}$ and $O_{1,2}$ are two input and output channels. A schematic (b) electronic and (c) optical two-port switch.

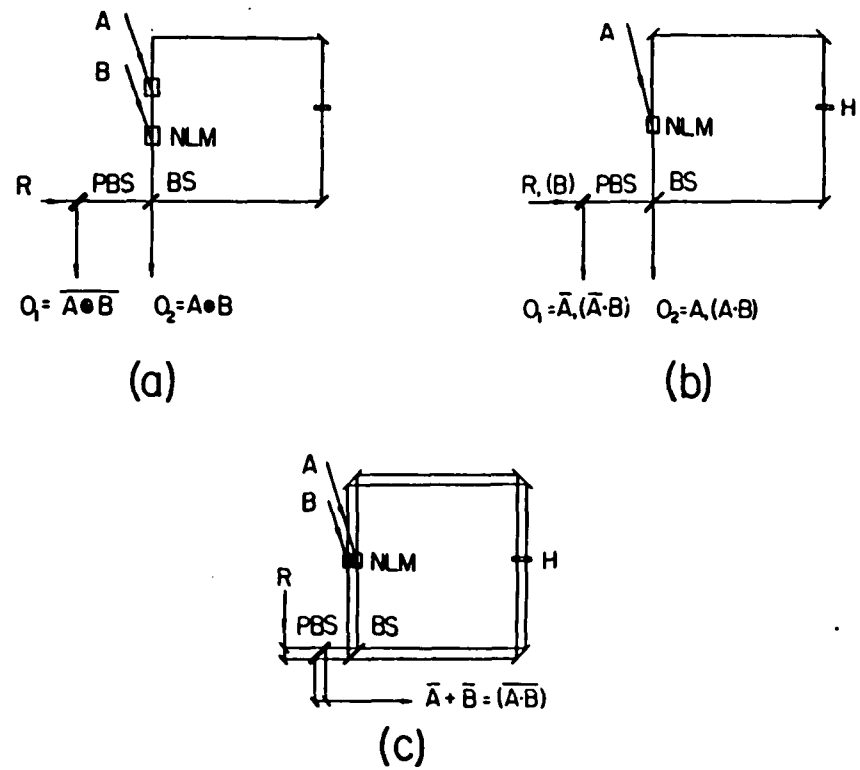


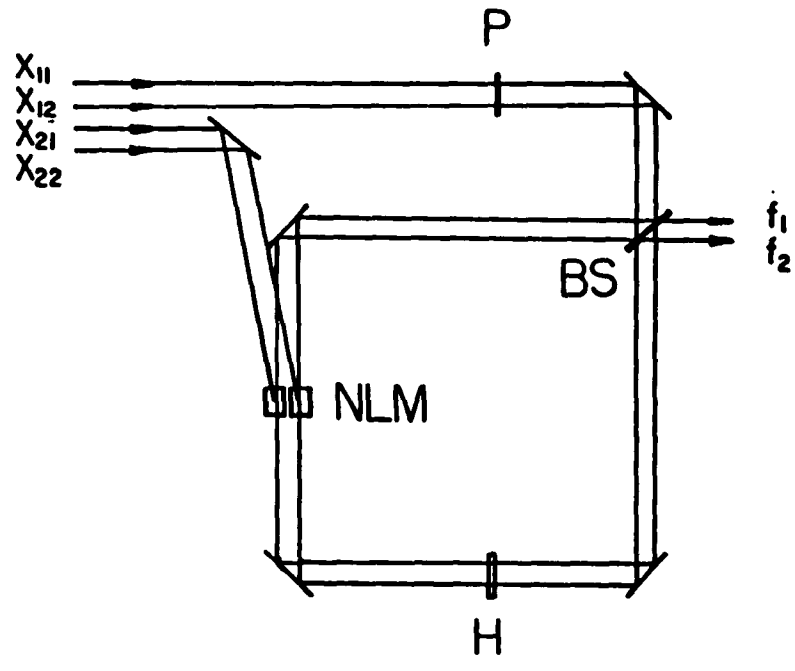
Fig.4.3.2 **Optical TPSIS implementations of two-input binary (a) EOR; (b) AND, and (c) NAND switches. Using a second output channel, other logic functions can also be implemented.**

X_1 \ X_2	0	1	2
0	0	0	0
1	0	1	1
2	0	1	2

(a)

X_{21} / $X_{11}X_{12}$	00	10	11
00	00	00	00
10	00	10	10
11	00	10	11

(b)



(c)

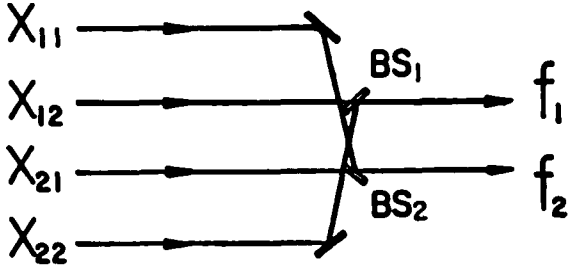
Fig.4.3.3 (a) Ternary and (b) BCT truth table of a two-input MIN logic operation. (c) the corresponding TPSIS implementation.

X_1 \ X_2	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

(a)

$X_{11}X_{12}$ \ $X_{21}X_{22}$	00	10	11
00	00	00	00
10	00	10	11
11	00	11	10

(b)



(c)

Fig.4.3.4 (a) Ternary and (b) BCT truth table of a two-input MAX logic operation. (c) the corresponding optical implementation.

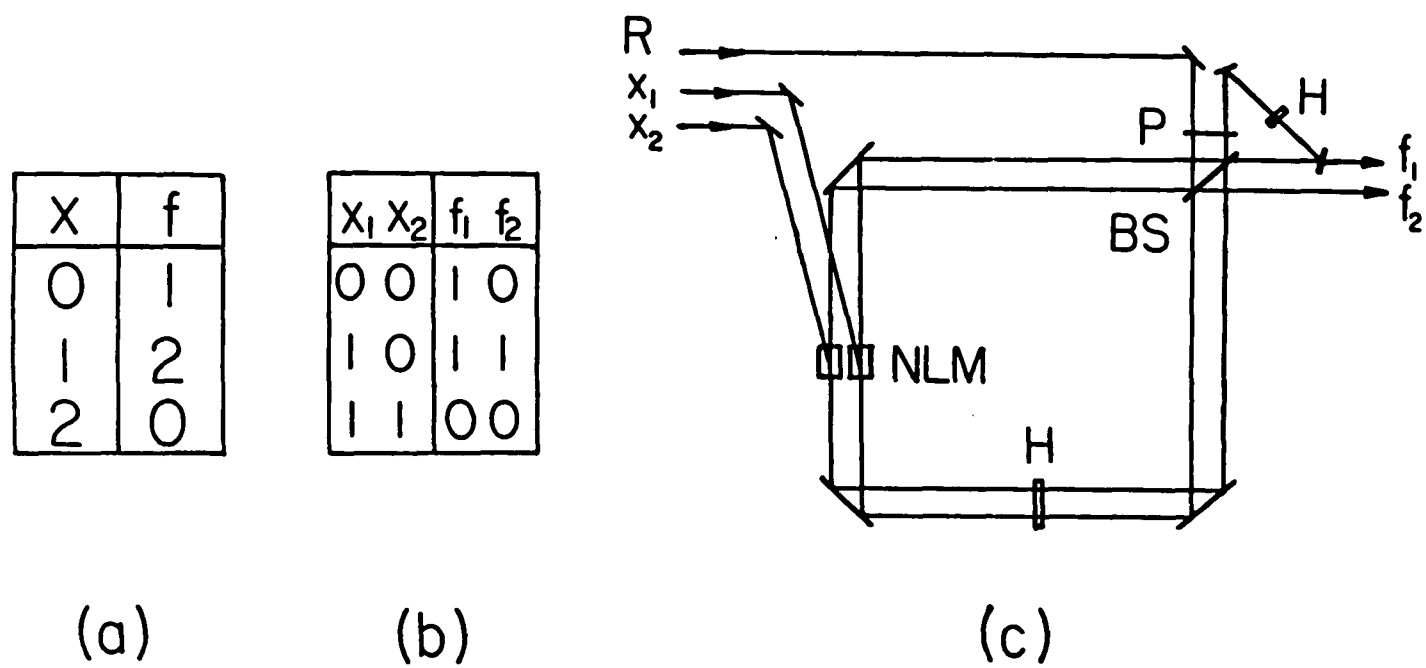


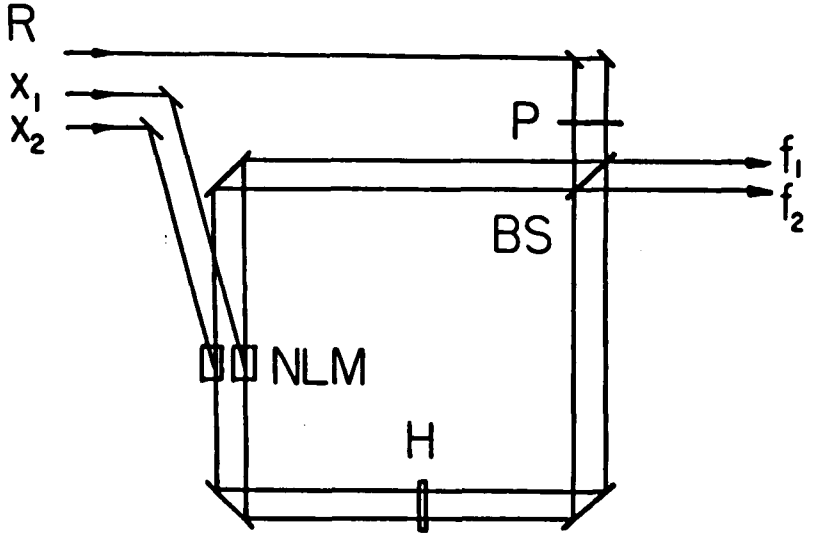
Fig.4.3.5 (a) Ternary and (b) BCT truth table of a SUCCESSOR. (c) the corresponding TPSIS implementation.

X	f
0	2
1	1
2	0

(a)

x_1 x_2	f_1 f_2
0 0	1 1
1 0	1 0
1 1	0 0

(b)



(c)

Fig.4.3.6 (a) Ternary and (b) BCT truth table of a NEGATOR. (c) the corresponding TPSIS implementation.

X	0^0_X	0^1_X	0^2_X	1^1_X	1^2_X	2^2_X
0	2	2	2	0	0	0
1	0	2	2	2	2	0
2	0	0	2	0	2	2

(a)

X_1X_2	$0^0_{X_1}0^0_{X_2}$	$0^1_{X_1}0^1_{X_2}$	$0^2_{X_1}0^2_{X_2}$	$1^1_{X_1}1^1_{X_2}$	$1^2_{X_1}1^2_{X_2}$	$2^2_{X_1}2^2_{X_2}$
00	11	11	11	00	00	00
10	00	11	11	11	11	00
11	00	00	11	00	11	11

(b)

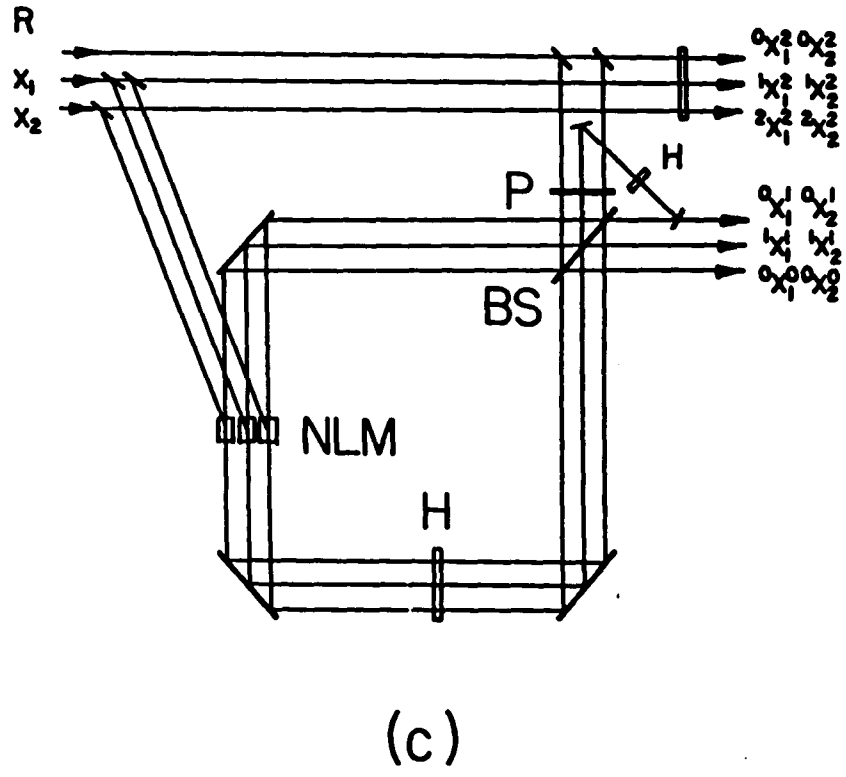


Fig.4.3.7 -(a) ternary and (b) BCT truth table of various Literal operators. (c) the corresponding TPSIS implementation.

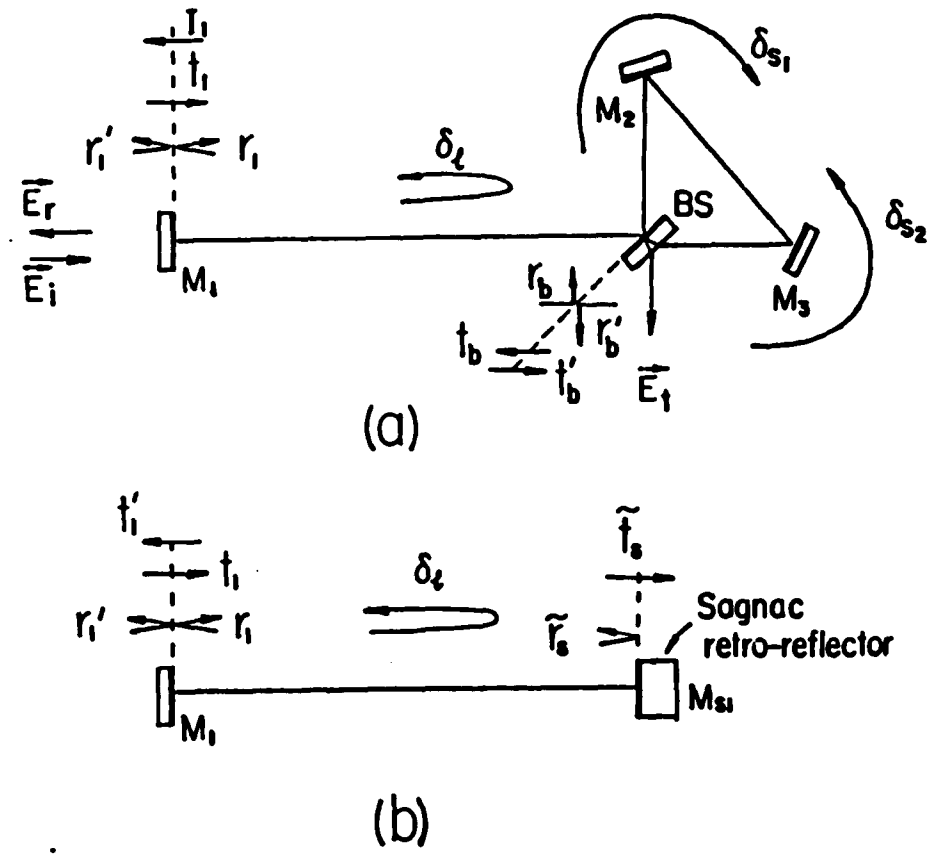


Fig.4.4.1 (a) A schematic diagram of the SIFP: $\bar{E}_i$ and $\bar{E}_t$ ($\bar{E}_r$), the resonator input and transmitted (reflected) output waves; M_i (i =1,2,3), mirrors; BS, beamsplitter; t_i (t_i') and r_i (r_i') (i =1, b), direction-dependent mirror and BS wave amplitude transmittance and reflectance; δ_l and $\delta_{s,1}$ ($\delta_{s,2}$), co-linear section and the SI clockwise (counterclockwise) section round-trip phases. (b) the equivalent FP diagram with an effective SI as an retro-reflector (M_{SI}), $\tilde{t}_s$ and $\tilde{r}_s$, SI wave amplitude effective transmittance and reflectance.

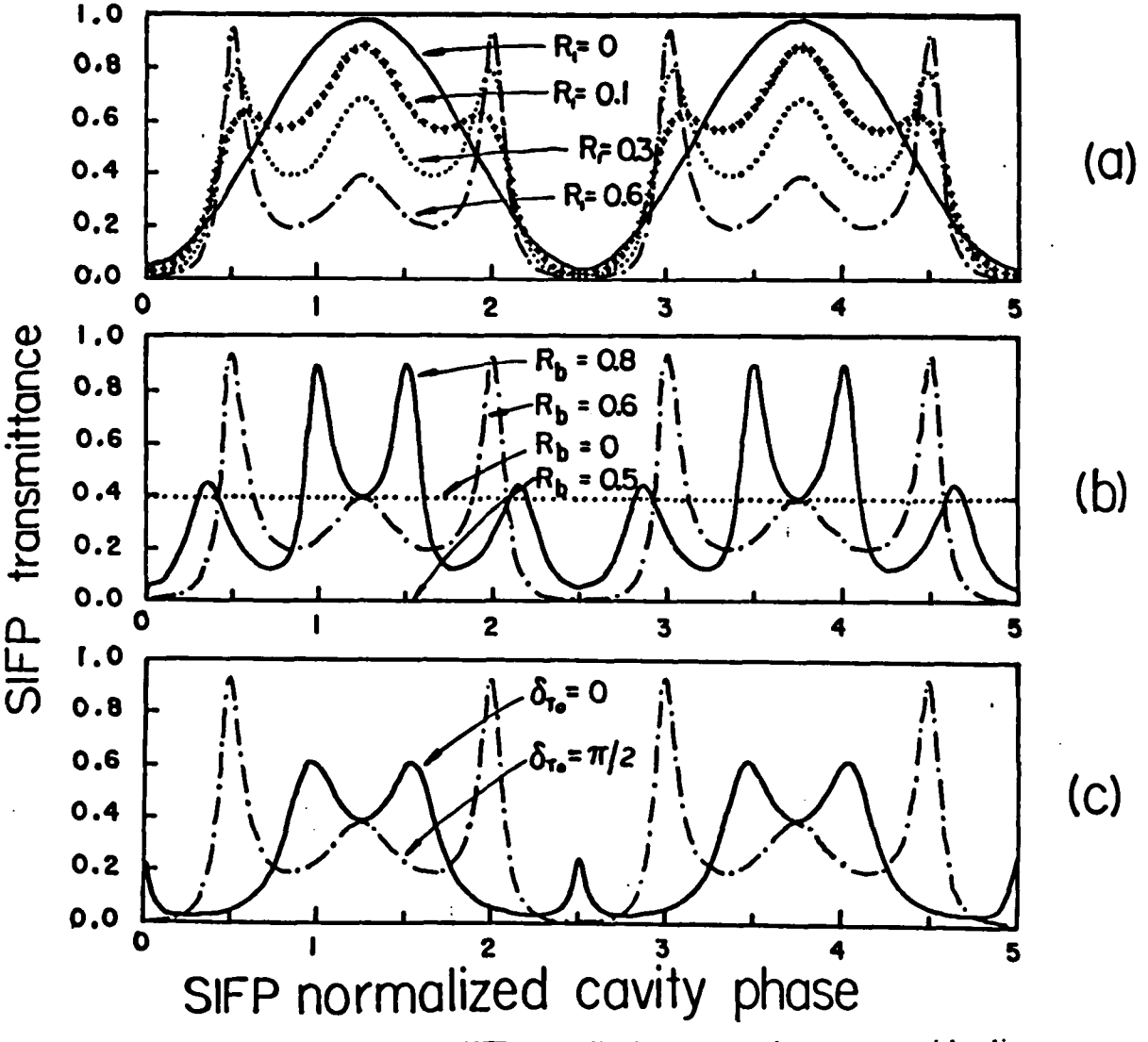


Fig.4.4.2 Intensity transmission vs. SIFP normalized resonator phase curves with adjustable parameters (a) input mirror reflectance R_1; (b) BS reflectance R_b and (c) resonator initial phase δ_{T0}.

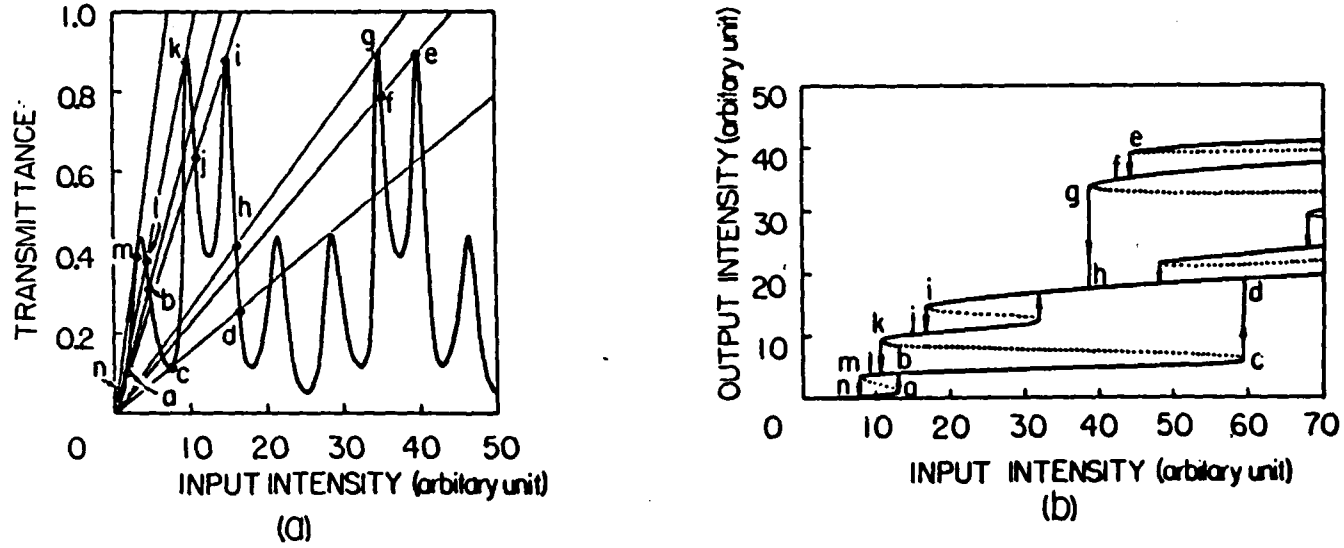


Fig.4.4.3 (a) A typical SIFP transmission vs. input intensity curve used for SIFP multistability analysis. Intersections of the straight line with the nonlinear transmission curve indicate multiple critical switching input and output intensities. (b) multistable input and output SIFP intensity relations with corresponding critical switching points a, b through m, n.

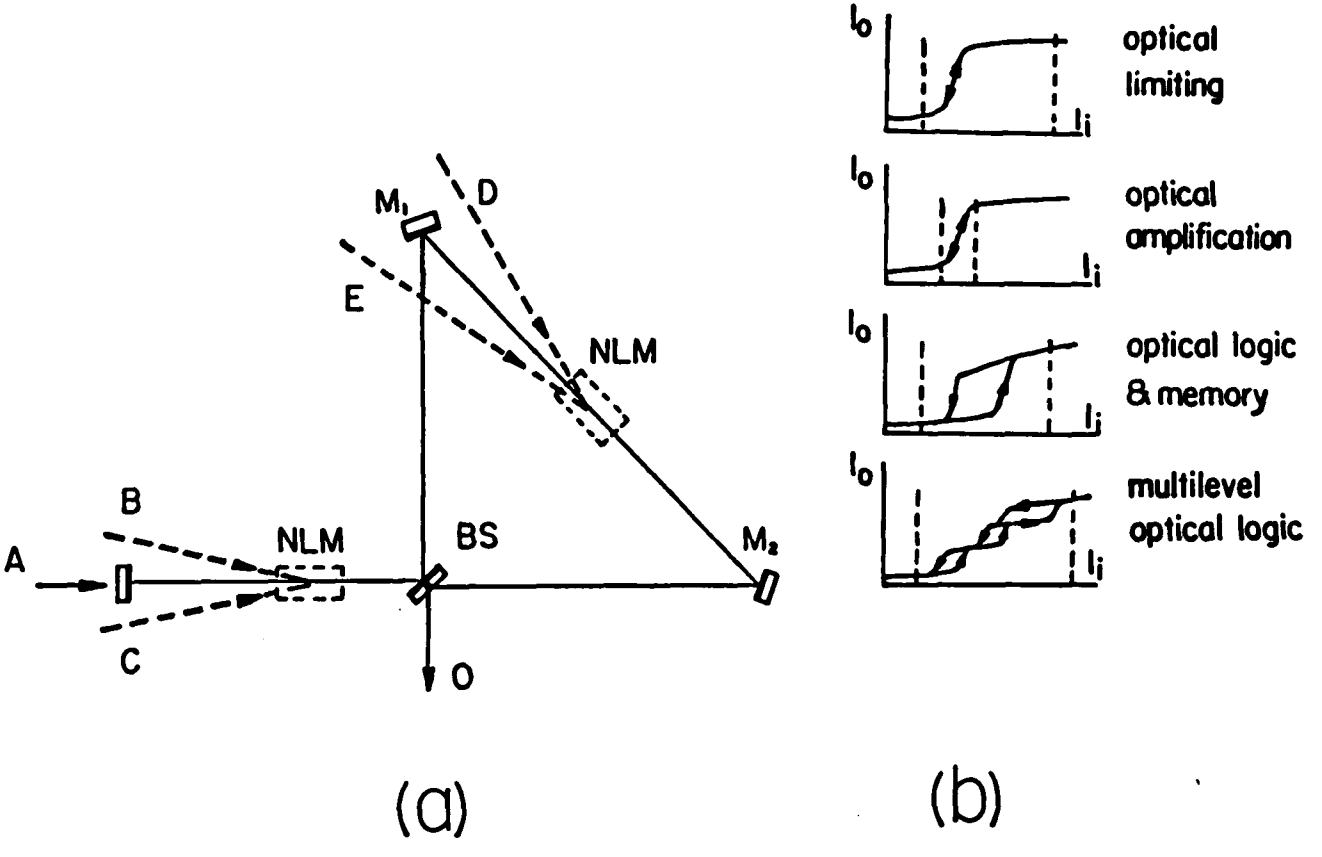


Fig.4.4.4 (a) A SIFP-based optical logic device. NLM can located at either one of the two marked places. In addition to primary input A, the NLM can be pumped by the logic beams B, C, D, and E. (b) Four possible SIFP applications to optical computing. The vertical dashed lines indicate the operational region.

V. OPTICAL PATTERN LOGIC AND SYMBOLIC PROCESSORS

5.1, Introduction

In an electronic digital computer, binary bits are represented by voltage levels. For positive logic, high and low voltages are used to denote logic one and zero. Since using nonlinear optics methods, optical signals can also be switched between two intensity levels, a number of proposed optical binary logic structures also adopt the intensity on/off switching state assignment. In the previous chapter, using various SIS arrangements, a number of binary canonical logic elements were proposed. However, a common difficulty found with this logic representation is that not all 16 two-input binary gates can be implemented with a single step. Using a particular nonlinear optical phenomenon, the implementations of INV, AND, OR, and EOR are always found more easily than others. When other gates, e.g. NAND and NOR, are needed, a cascade of INV with AND and OR must be employed. Thus, for different gates, switching speed will be different. In addition, with this on/off state assignment, optical parallel processing property is not fully utilized.

Optical pattern logic[2] offers an alternative way to perform digital logic processing. Using pattern logic, two binary states are represented by two orthogonal patterns. In a two-input binary case, two pairs of orthogonal spatial patterns are used. Because each pattern contains two sub-pixels, for each logic gate, four input and two output pixel channels are preserved. However, with optics, to obtain these parallel channels is not difficult. It can be performed by simply dividing the whole input aperture into four parts. For logic operation, either illuminating inputs (the correlation approach[1,2]) or an output mask (the

triple multiplication approach[3]) is switched. In the following sections, we propose and demonstrate a number of new optical pattern logic schemes. In the first approach, an ultrafast OPC processor is modified to perform picosecond binary logic operations. Both the correlation and the triple multiplication methods will be used. The corresponding logic inputs are intensity-encoded pixel patterns. Then, we will investigate other possible pattern logic encoding, such as polarization encoding, scheme. It will be shown that with the new encoding scheme, more input variables or data can be used and multiple logic operations can be performed simultaneously. Finally, we will describe a new ultrafast symbolic pattern recognizer that can process input binary symbolic patterns in picoseconds.

5.2, Ultrafast OPC-based Binary Pattern Logic Processors

Nonlinear optical phase conjugation (OPC) offers solutions to many problems in real-time optical signal and image processing. In an analog mode, using OPC, optical signals (images) can be processed in parallel. In this section, a new method to perform parallel digital optical logic that combines OPC with parallel logic generation techniques is proposed. This technique is suitable to optically implement all sixteen binary logic operations.

In both, the correlation and the triple multiplication approaches the logic encoding is identical with the difference being in how the different logic operations are performed. While the correlation approach uses different LED source patterns, the triple multiplication method uses a switchable operation mask to obtain different logic operations. It will be shown that both methods can be implemented with an ultrafast parallel OPC element.

5.2.1, OPC-based optical triple-multiplication logic processor

An OPC technique based on the use of the triple multiplication scheme will be described first. In Fig.5.2.1, a typical OPC experimental setup is shown. Three input beams generated from the same laser, labled by E_A, E_B, and E_C, are collimated into a cubic ($\chi^{(3)}$) nonlinear material (NLM). The beams E_A and E_B are mutually phase-conjugated. The third beam E_C serves as the probe. The nonlinear interaction of the three beams in

the NLM generates a polarization source that radiates a fourth beam

$$E_O \propto \chi^3 E_A^* \cdot E_B^* \cdot E_C^* \tag{5.2.1}$$

where the * stands for complex conjugation. In analogy to the triple multiplication parallel logic geometry, the two encoded logic input masks T_A and T_B (the encoding and operation schemes for both the triple multiplication and the correlation methods are summarized in Table 5.2.1) are inserted into the path of beams E_A and E_B, respectively, while the operation mask T_C is placed on the E_C beam. The phase-conjugate signal E_O, separated out by a beamsplitter, is the logic output. This output beam possesses the same properties as the usual triple multiplication logic arrangement. Since this OPC geometry is no longer colinear, both input and output beams can be either separated spatially or directionally. This separation allows for the optical interconnection of various stages of parallel logic processors. These processors are needed to perform multiple-instruction multiple-data (MIMD) parallel processing. Also, to generate a phase-conjugate signal, as long as E_A and E_B beams counterpropagate (phase- conjugated), the third E_C beam can be incident from any angle. Thus, using different operation masks with various angular probe beams together with an angular multiplexer that selects, at a given time, a different probe beam, both space- and angle-variant optical parallel processing of large amounts of data are possible. Furthermore, since the OPC is a coherent optical technique, the combination of the OPC parallel digital logic method and other standard coherent optical analog processing techniques can make it a more flexible arrangement.

5.2.2, OPC-based optical correlation logic processor

Next, using the NLM cell as a real-time triple-product operator, an correlation type parallel OPC logic generation[5] is discussed. As mentioned earlier, to obtain the various optical binary logic operations, the correlation method uses an array of switchable LED source patterns. From a geometric point of view, the interlaced output pattern, due to the different LEDs, can be interpreted as an optical shadowgram. However, this operation is

also equivalent to a two dimensional (2D) optical multiplication followed by a incoherent correlation. It is well known that 2D coherent optical correlation can be performed using a Fourier transform lens[6]. Based on this concept, in Fig.5.2.2, an coherent real-time OPC correlator for implementing correlation type parallel logic operations is shown. This coherent OPC correlator was first proposed and demonstrated by White and Yariv[7] as a means to perform various coherent analog image convolution and correlation operations. In addition to a NLM cell, three equal focal-length Fourier transform lenses are also employed. For the 2D optical signals E_A, E_D and E_C in front focal planes of three lenses, the phase-conjugated output is

$$E_O \propto \chi^{(3)} E_A * E_D \bullet E_C \tag{5.2.2}$$

where $\bullet$ and $*$ denote correlation and convolution operations, respectively. To obtain the required multiplication operation for the correlation type parallel OPC logic, the two logic input masks T_A and T_B are superimposed and placed on the E_A beam. In analogy to the correlation LED source array, a corresponding source mask T_C is inserted into the path of the E_C beam with four transparent dots representing four displaced Dirac-δ functions. Since no additional convolution is required, the E_D beam mask has a single on-axis dot representing a central δ function. To obtained the correct correlation function, the E_C beam δ function displacements d_{x_i} and d_{y_i} where i =1,2,3 and 4, must be chosen as

$$| d_{x_i} | = | d_{y_i} | = D / 4 \tag{5.2.3}$$

where D is input pixel size. Since the convolution of a function with a δ function shifts that function, after the OPC correlation operation, the needed parallel OPC logic is obtained. To insure the correct correlation result, the NLM cell should be made thin enough to enclose only the optical Fourier spectra of the three interacting beams[7]. For clarity, in Fig.5.2.3, the 2D correlation of a square and four properly displaced δ functions is illustrated. The left-most box contains four sub-squares each of which represents a possible

transparent area. When all four middle box δ functions are on, the correlation result, shown in the right most box, contains nine possible illuminated areas. With this method, using sixteen possible on/off combinations of the four δ functions, the sixteen two-input binary logic operations can be performed. In the correlation method, because the input and output areas are not identical, in general, it is difficult to cascade two or more of these processors. For this reason, a conventional (black/white encoded) OSC method is classified as a single-instruction multiple-data (SIMD) processing. To perform parallel multiple-instruction multiple-date (MIMD) operations, other encoding scheme, such as the use of polarization encoding[8], may be used.

5.3, Polarization-encoded Optical Pattern Logic Processing

In the previously described pattern logic methods, both the logic encoding and spatial filtering process are performed by the black/white (transparent/opaque) screen. In this section, the use of a polarization encoding and filtering method to perform the spatial logic operations is proposed. Both linear, orthogonally polarized and hybrid form, polarizations with transparent/opaque mask input, logic signals are used. Using this polarization or hybrid encoded pattern logic method, double- or triple-instruction logic operations can be performed[8]This technique can be extended to generate multi-input binary as well as two-input multiple-valued logic functions. Although this encoding method is suitable for both methods, we only discuss correlation logic processing case. Pertinent examples such as the design of a binary full- and a ternary half-adder are presented.

5.3.1, Polarization encoded two-variable binary logic processing

In the proposed method, while the geometry is identical to the conventional lensless OSC, the logic inputs and outputs are represented by the sense of polarization. Take the two-input (A and B) binary logic as an example (see Table 5.3.1). These inputs are represented by the two polarization encoded masks (the second and third columns of Table 5.3.1) where the symbols - and | denote the two linear, parallel and perpendicular,

polarizations representing the physical x and y - directions, respectively. The two thus encoded input masks (see the fourth column of Table 5.3.1 where $\wedge$ denotes the overlap) are illuminated by a group of four nonpolarized light sources. When three of the four sources (see the first column of Table 5.3.1) are on, corresponding to four overlapped input patterns, on the output screen four different projections are formed. In each of the four cases, two cross-polarized light patterns can simultaneously exist. The x (y) - polarized output plane center cell pattern corresponds to the logic operations A NAND B (A OR B), respectively. Thus, a fixed point source pattern and the rotation of the output center-cell polarizer allows the implementation of two different binary logic functions. By removing the output polarizer, a third binary function, the superposition of the two cross-polarized patterns, can also be generated. With a OSC, because the opaque part of the screen blocks the light, the mutually transparent part of the overlapped inputs is limited to be only a quarter of the mask area. With a POSC, the mutually transparent input mask area is doubled (with each half transparent to one of the two orthogonal linear polarizations). Therefore, for a fixed source and input pattern, two orthogonal transmission channels exist.

Orthogonally polarizing light sources can also be used as light sources. In this case, the overlapped transparent masks respond only to x (y) - polarized sources. Using different combinations of polarized sources, different binary logic functions can be implemented. In Table 5.3.2(a), using either unpolarized on/off or orthogonally polarized input light source states, the generations of all sixteen two-input binary logic functions are summarized. For unpolarized point sources, either output state can be obtained from the other by inter-changing (for both variables) the zero and the one logic assignments. For polarized sources, the cross-polarized outputs represent positive- and negative-true logic functions, respectively. In addition to the input codes shown in Table 5.3.1, other input encoding methods where the overlapped input patterns preserve, for the two orthogonal polarizations, the two mutually transparent parts, are also possible. In Table 5.3.2(b), for the input C, an alternative input variable encoding is shown. For the inputs A and C, the corresponding

sixteen logic function generations are also shown. It has been indicated that a conventional single element OSC processor is a single-instruction multiple-data (SIMD) machine. Using POSC, both double and triple-instruction logic processing can be performed. If in the previous example, we locate three different detectors at the center cell of the output screen, with the first (second) one being x (y) - polarized, and the third one unpolarized, three different logic functions can be simultaneously processed. Therefore, a single element POSC represents a multiple-instruction multiple-data (MIMD) machine.

5.3.2, Polarization encoded multiple-variable binary logic processing

In binary optical computing, implementation of multi-input logic functions are needed. For example, for binary addition, to generate both the output sum and the carry, three inputs need to be used. To perform binary OSC addition, in order to preserve symmetry, Kozaitis and Arrathoon[5] have used four, rather than three, inputs. One of the four input, however, is kept at zero during the operation. With this method, the detectable output signal area is reduced to a quarter of the previously used two-input area. This size reduction limits, due to diffraction effect, the pixel integration area. To achieve a reasonable output, larger input pixels must be used. The use of POSC leads to larger aperture (identical to two-input case) three-input binary logic operations. Using three differently encoded inputs A, B, and C (see Tables 5.3.2 (a and b)), the overlap among the three inputs will always contain a mutually transparent area to either one of the two orthogonal linearly polarized beams. The use of the eight possible input overlaps, together with a group of point sources, can generate 2^8 three-input binary logic functions. For a one-bit binary full-adder, two parallel POSC elements, one for the sum and the other for the carry, need to be used. Because the POSC is a MIMD machine, using other input encoding schemes, it is possible to perform a single POSC element binary addition. As an example, in Fig.5.3.1, a single element POSC binary full-adder is shown. Here, the input uses hybrid (both transparent/opaque and orthogonal polarization) codes. In the first four columns of Fig.5.3.1, the input variables X, Y and Z, and their corresponding overlaps are shown.

When all four unpolarized point sources are on, the two cross-polarized patterns in the center cell of the output plane represent the resultant sum and carry bits, respectively. Thus, using two, one x - and the other y - polarized, detectors at the output center cell, a single element POSC binary full adder can constructed.

5.3.3, Polarization-encoded ternary logic processing

The similar idea can be applied to two-input ternary logic computing. For each input variable, three mutually orthogonal states representing the symbols 0,1 and 2, respectively, are required. For the nine possible overlaps among the two ternary input variables, a mutually transparent area must be provided. The use of the two orthogonal polarizations in the four corners of the overlapped pattern produces eight different states. The ninth state is encoded as an unpolarized but transparent corner. As an example, consider the operation of a two-input POSC ternary half-adder. In Fig.5.3.2, the hybrid form of input variables A and B are shown. Using the input variable truth-table (the first two columns), in the third column, the nine possible two variable A and B overlap forms are shown. One of the overlap patterns is forced to be opaque. The sum output symbols, 0, 1 and 2, are encoded as opaque, y - and x - polarized signals, respectively. Correspondingly, in the fourth column, the source and the center cell output patterns are shown. The results, shown in the fifth column, are obtained from the two, x - and y - polarized, center cell detectors. To generate the carry another POSC cell must be employed. For this carry, in the sixth and the seventh columns, the corresponding point source pattern and the output unpolarized detection results are shown.

5.4, OPC-based Optical Symbolic Substitution Processor

Recently, Brenner, Huang, and Streibl[10], proposed an optical symbolic substitution (OSS) computation scheme. With an OSS scheme instead of decomposing the computation into stages of Boolean logic operations that use multiple inputs to generate a single output, both multiple spatial inputs and their relative locations are utilized to generate, in parallel,

multiple spatial outputs.

The OSS method can be decomposed into a pattern recognition and scription step[10]. In its operation, pattern recognition (searching for the dark pixel locations) consists of possible input multiple spatial shifts, a collinear superposition (an OR), a threshold NOR, and a masking (an AND) operations. In this approach, for the shift and superposition operation, an interferometer is employed, while for the NOR operations, a matrix of parallel nonlinear optical threshold NOR gates is also used. From the DeMorgan's theorem, however,

$$\overline{(A + B + C \cdots + X + Y + Z)} = \bar{A} \bullet \bar{B} \bullet \bar{C} \cdots \bar{X} \bullet \bar{Y} \bullet \bar{Z} \qquad (5.4.1)$$

a multiple-input NOR gate can be synthesized with INVERTERs and AND gates[11]. For INVERSION, instead of searching for the dark, the white (transparent) pixels are recognized. Compared to a threshold NOR, a threshold AND-based approach has the advantage that it is easier to implement optically. However, in terms of signal-to-noise ratio, an optical threshold-AND gate may introduce an additional recognition error. When an N pixel pattern is to be recognized using an optical threshold AND gate, an output of one will be achieved only when the detected total intensity ($N I_0$, where I_0 is a single pixel intensity) is above a threshold. Thus, with this type of gate, one must distinguish between levels $(N-1) I_0$ and $N I_0$. As N increases, its noise immunity decreases. For this reason, a threshold NOR logic-based approach possesses a larger signal-to-noise ratio than its threshold AND-based counterpart[10]. For the pattern scription step, the previously recognized pixel pattern is used in an another device where only spatial shift operations are performed.

In this section, a new OSS pattern recognizer that employs a multiple-input Boolean AND element is proposed. To recognize a multiple-white-pixel pattern, in addition to multiple spatial shifts, only AND operations are used. To prevent noise accumulation caused by a threshold-based approach, an optical phase-conjugate (OPC) multiple-input Boolean AND element will be employed. The advantages of using an OPC-based symbolic recognition scheme will also be discussed.

5.4.1, AND-based symbolic pattern recognition

For an OSS operation, the first step is a symbolic pattern recognition. The input is a 2-D rectangular pattern array that contains several elemental light pixel patterns (the elemental patterns). For the purpose of this discussion, let the elemental pattern consist of a square of four-pixels. When the modulation is a transparent/opaque code, this elemental pattern can form sixteen different pixel combinations. Excluding the two trivial patterns (either all transparent or opaque) that can be recognized by other methods, in Table 5.4.1, the remaining fourteen combinations are listed. These patterns can be classified into three groups: A, B and C. Since for the recognition of the four group-A patterns only an optical masking operation on these patterns is needed, no further discussion is presented.

To recognize the six group-B patterns, shift operations must be performed. As an example, consider the input pattern shown in Fig.5.4.1. The input image contains four four-pixel elemental patterns where one of them that contains two transparent main-diagonal pixels is to be searched. To recognize this four-pixel elemental-pattern, first, the image is replicated into two parts which are then either spatially shifted up or to the left by one unit, respectively. Together with a recognition mask that consists of four transparent pixels at the four elemental pattern's lower left-hand corners, the shifted images are next directed to a three-input 2-D parallel AND gate. In this case, its output indicates that the search pattern resides at the upper-right input image location. The three-input 2D AND operation can also be viewed as two cascaded two-input AND operations, i.e. an AND between the two shifted inputs, and a second AND between the first AND output and the recognition mask. In particular, the two two-input AND operations may help to discriminate against both intra- and inter-elemental-pattern noises. For other type-B inputs (see Table 5.4.1), different spatial shifts and recognition masks are used. When one of the two replicated inputs is stationary, only a single spatial shift, a shift that allows the two transparent pixels to overlap, is sufficient. For example, in Fig.5.4.1, by fixing the lower image position, only the upper image needs to be shifted in the upper right direction to a position

where the two intra-elemental-pattern transparent pixels overlap. In general, to recognize a two-transparent-pixel pattern, a single relative shift and a three-input AND operation are required.

Similarly, for the group-C patterns, to discriminate against the intra-elemental-pattern noises, three copies of an input image with two relative shifts and a three-input AND element are needed. To discriminate against inter-elemental-pattern noises, an additional masking (AND) operation is used. As an example, in Fig.5.4.2, a type-C pattern recognition is shown. The input image contains two elemental search patterns. Here, either a single four-input or three two-input parallel AND elements needs to be employed. In general, to search for a N-transparent-pixel elemental pattern, N-1 pattern spatial shifts and a N-input parallel AND element must be used.

5.4.2, OPC-based implementation

In this section, the use of an OPC element for a Boolean multiple-input AND-based OSS pattern recognizer is described. The OPC device can be considered as a three-input Boolean logic AND element. In Fig.5.4.3, an OPC-based AND device is shown. A collimated type-B input image beam is divided, using a beamsplitter, into two copies. Directed by two plane mirrors, the two beams counterpropagate, with a relative spatial shift, to an OPC material. A third beam, containing the recognition mask, is also directed to the χ^3 material. The generated OPC signal counterpropagates with respect to the third beam. Finally, using a second beamsplitter, this signal is directed to the system output. With a slight modification, the OPC device can also be configured as a four-input, an element called for the type-C pattern recognition, AND element. In this case, all the three OPC input ports are used to carry spatially shifted input images. At the output port, the recognition mask is placed.

Using a polarization encoding method, it is also possible to collinearly combine the third beam with one of the counterpropagating inputs[12] (see Fig.5.4.4 for the geometry). Assume that the two counterpropagating inputs are linearly polarized. With a polarizing

beamsplitting cube, the third input beam that is orthogonally polarized is also collinearly guided, with one of the counterpropagating inputs, to the nonlinear material. In this case, the polarization of the OPC output is identical to the third input polarization direction and it can easily be separated by the polarizing beamsplitter.

5.4.3, Advantages of OPC-based symbolic recognition

This new OPC-based symbolic recognition scheme has the following advantages over the other schemes:

(1) instead of performing, as required by the scheme of Ref.7, three different (an image superposition equivalent to a logic OR, a threshold NOR and a masking equivalent to an AND) logic operations, here, only a single logic element, a multiple-input optical AND gate, is employed.

(2) the OPC-based scheme allows ultrafast processing. Using materials such as semiconductor-doped glasses or nonlinear polymers pico- or sub-picosecond OPC switching response times have been observed[13,14]. When the input binary pixel pattern is also generated by an ultrafast 2D modulation scheme such as from a parallel bistable etalon array[15] an ultrafast OSS pattern recognition can be performed.

(3) the OPC-based approach reduces the cumulative error that occurs with a threshold-based AND gate. This is true because the generation of an OPC-AND output is based on the input phase-matching condition that does not, to the first order, depend on the input intensity levels.

(4) the OPC-based approach also reduces the interference errors that occurs in a collinear input pattern superposition geometry. With the Refs.7 schemes, it is important to perform a large aperture nearly perfect image superposition. Otherwise, any disturbance that changes input wavefront by a fraction of a wavelength will produce slowly changing interference pattern leading to recognition errors. This is not the case with the OPC AND-based device since the off-axis angular inputs produce much higher density interference fringes. The averaged pixel intensity of the high density fringes can reduce the decision

error.

(5) the OPC outputs are potentially cascadable. With a material, e.g. a multiple-quantum-well semiconductor, that exhibits a large nonlinearity and with an increased beam interaction region, an amplified OPC output can be obtained. The OPC amplification has been experimentally observed in CS_2 [12]. Thus, multiple-stages of OSS operation are possible.

One of the problems with the OPC-based scheme is that to recognize a N-transparent-input (where N is larger than three) pattern, a number of cascading AND stages are needed. This sequential operation does decrease the recognition speed. One way to minimize this problem is to use a tree-type (in $\log_3 N$ steps) logic decomposition structure. Another problem with the OPC-based scheme is that the OPC off-axis input is scaled causing a vignetted output. The polarization-encoded counterpropagating OPC geometry (see Fig.5.4.4) can eliminate this problem.

5.5, Experimental Demonstrations

To verify various proposed OPC-based digital processors, using a QUANTEL mode-locked Nd^{3+}: YAG laser that generates 32-picosecond optical pulses, a number of OPC-based logic and symbolic processing experiments were performed. In Fig.5.5.1, an experimental setup is shown. First, using a second-harmonic crystal, the wavelength of the output pulses was converted from 1064 to 532 nm. A 2× telescope was employed to expand the beam spatial profile to an area of 2 cm^2 out of which a small portion (about 1 cm^2) was used. For a larger aperture OPC, parallel processing experiment, before beam expansion, the source needs to be spatially filtered. The spatially expanded laser beam was split, using a 30/70 (reflection/transmission) splitting ratio beamsplitter, into two parts A and B. The beam A was perpendicularly directed into a 2 mm thick CS_2 (2 ps response) cell, and reflected by a retroreflecting plane mirror located 3 mm behind the cell to form a beam counterpropagating geometry. The beam B that passes through a second beamsplitter (with 50/50 splitting ratio) was also guided into the CS_2 cell but in an off-axis (about 5°) direction. The OPC signal that propagates oppositely to this beam was separated by the second beamsplitter to an

output port where a Polaroid instant camera was placed. Although a much better real-time input modulation scheme can be incorporated, in our initial experiment, binary masks with translational stages were employed.

In the first experiment, the test of the OPC-based pattern logic processor was performed. Two orthogonally encoded logic masks f_A and f_B were placed in the beam A loop at the front and back of the CS_2 cell while all sixteen kernel mask mounted onto a translational stage was inserted into beam B. During experiment, these translational stages were synchronously controlled to provide appropriate spatial shifts. As results, in the bottom of Fig.5.5.2, the recorded light patterns corresponding to all sixteen logic operations are presented.

In the second experiment, this processor is modified to perform a multiple-valued logic operation. In particular, a 2-bit ternary to binary conversion was performed. On the left-hand side of Fig.5.5.3, the logic truth table as well as the input encoding are shown. Since, in this case, the output contains three bits, three parallel OPC channels need to be used. In our experiment, the channel separation was again performed by shifting the translational stages. On the right-hand side of Fig.5.5.3, the experimental conversion results are illustrated.

Next, the operational principle of the proposed symbolic processor was verified. First, a group-B pattern was used for recognition. The sixteen-pixel input mask contains four four-pixel type-B elemental patterns. The search pattern was a main-diagonal transparent pixel elemental pattern (see Fig.5.5.4(a)). With an appropriate spatial shift, the two beams containing two shifted copies of the input mask were directed from the opposite directions to the CS_2 cell. A recognition mask was used in the probe beam B. As illustrated in Fig.5.5.4(b), the picosecond OPC output signals shows that the expected search pattern was located at the input image upper-left and lower-right hand corners. The use of this OPC-based processor for a group-C pattern recognition was also performed. Correspondingly, in Fig.5.5.4(c) and (d), the input pattern and the recognized output signal are shown.

5.6, Summary

To summarize, in this chapter, three parallel logic and symbolic computing schemes were proposed. First, the use of a real-time OPC triple-product device to generate coherent optical parallel logic operations was described. A NLM can be used as a major interconnection device that connects logic inputs to different output ports where different logic operations can be performed. The use of both triple multiplication and the correlation type parallel OPC logic implementation schemes were discussed. When both input signals are generated in real-time, i.e. by some ultrafast modulators, fast, real-time parallel logic processing of 2-D data can be performed. Following the OPC-based pattern logic approach, an efficient polarization encoding and filtering method to perform OSC optical computing was then proposed. Inputs are spatially encoded with either polarized or both polarized and transparent/opaque pixels. Either polarized or unpolarized input source arrays can be used. At the center cell of each output element, depending on different parallel polarization filters, three different logic functions can be obtained. In addition to the two-input binary, POSC method is suitable for large aperture multi-input binary and the two-input ternary optical computing. Using e-o material sandwiched between $\lambda/2$-plates and linear polarizers, real-time polarization encodings can be performed leading to optical parallel processing of a large amount of data. In the third proposed scheme, a new OPC binary pixel pattern recognizer for OSS was proposed. Using a number of spatial shift and AND operations, a given optical pixel pattern can be recognized. For an optical implementation, mirrors and beamsplitters were used to obtain the required spatial shifts while an OPC-based device was used for the logic AND operation. Using a 32 ps Nd^{3+}: YAG laser, some first order experiments were performed. The proposed ultrafast parallel logic and symbolic processing concepts have been experimentally verified.

5.7 References

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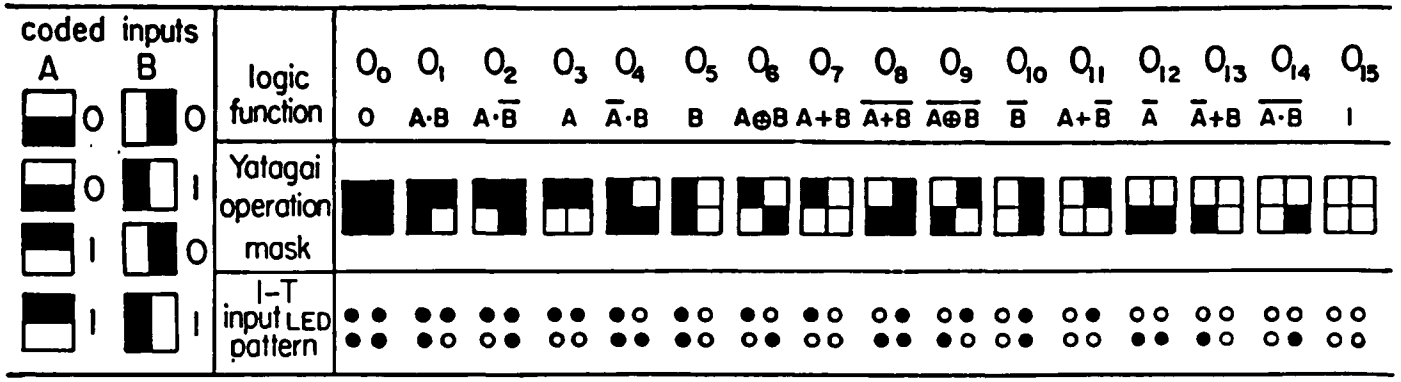


Table 5.2.1 Optical encoding (black/white code) techniques for either triple-multiplication (Yatagai's) type or correlation (I-T) type optical parallel logic processing. Both methods

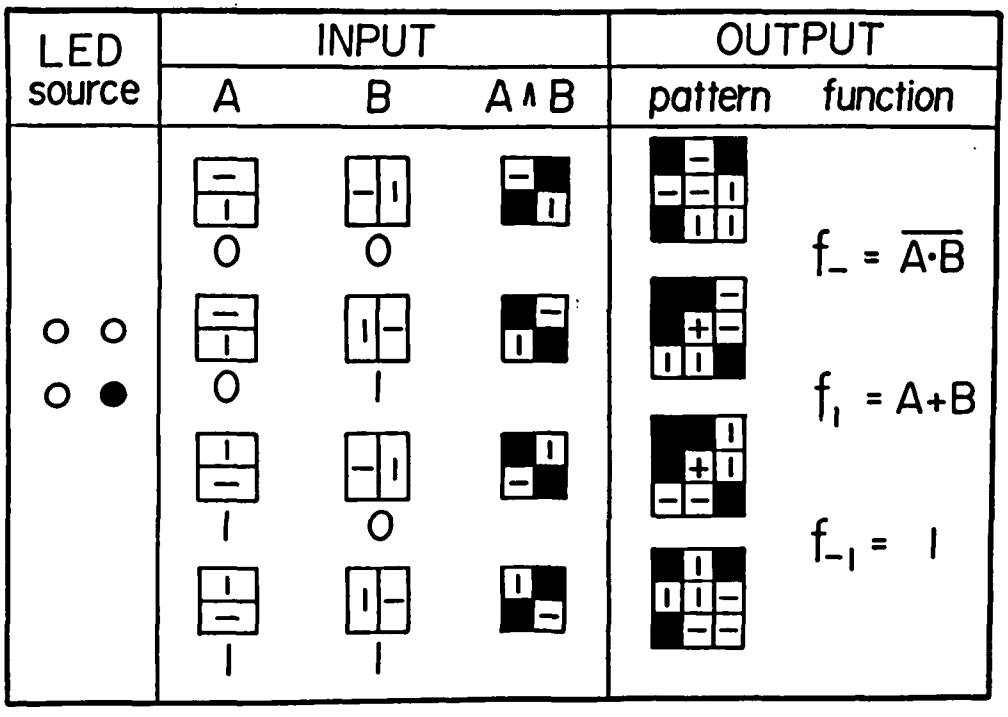
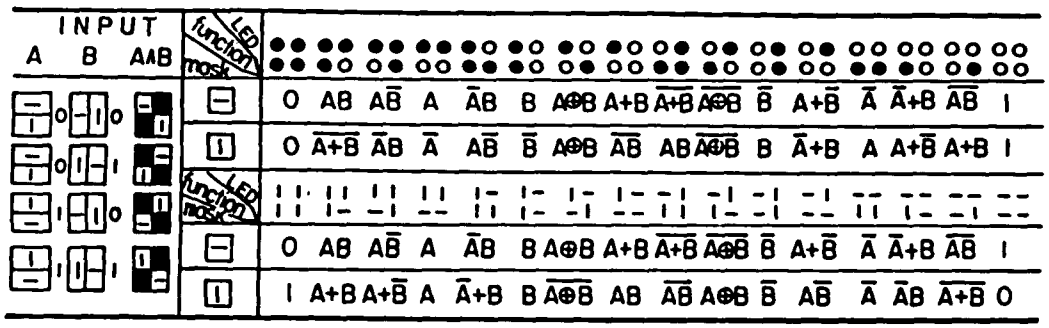


Table 5.3.1 An example of polarization encoding of input, output as well as LED source patterns. The symbols - and | represent x - and y - polarizations, and denotes the input overlap.

Table 5.3.2



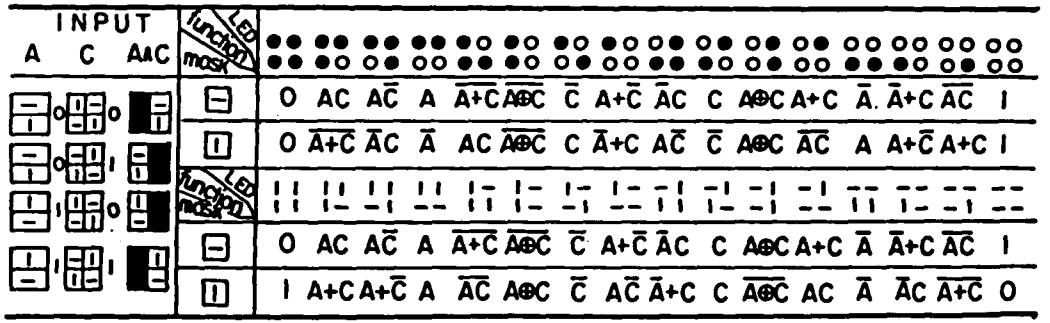


Table 5.3.2 Sixteen possible polarization encoded two-input logic operations. Inputs are encoded with either variables *A* and *B* [2(a)], or variables *A* and *C* [2(b)], logic operations. Both transparent/opaque and orthogonal polarization input LED states are used.

types	input patterns	No. of shifts	No. of inputs for AND
A		0	2
B		1	3
C		2	4

Table 5.4.1 A list of fourteen possible 4-pixel symbolic patterns. These patterns are classified into three, according to the number of transparent pixels, groups.

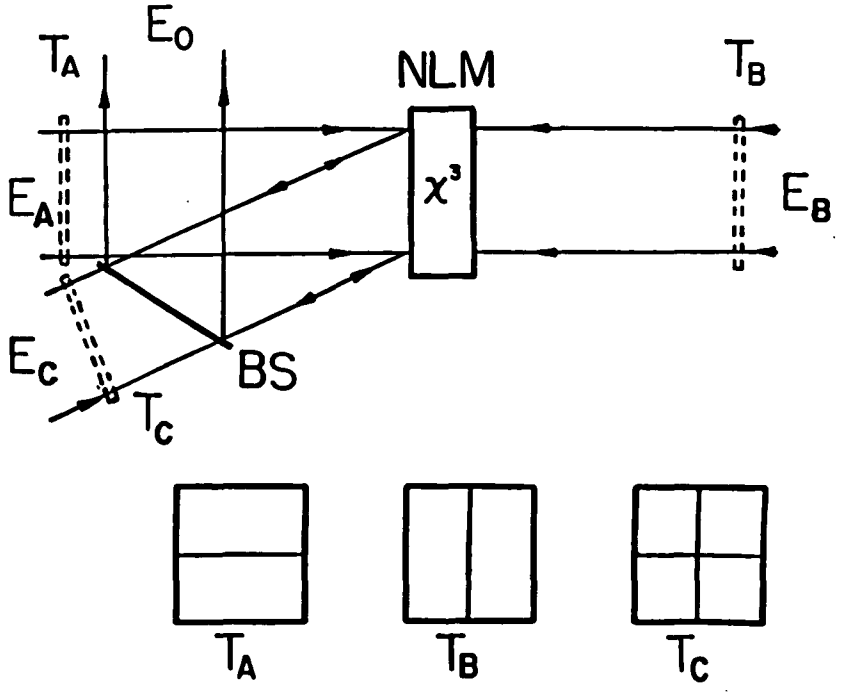


Fig.5.2.1 OPC implementation of a triple-multiplication type parallel logic processor. NLM, cubic nonlinear material; BS, beamsplitter; E_A, E_B and E_C, collimated input beams; E_O, the phase-conjugate output beam; T_A and T_B, two coded input masks and T_C, the logic operation mask.

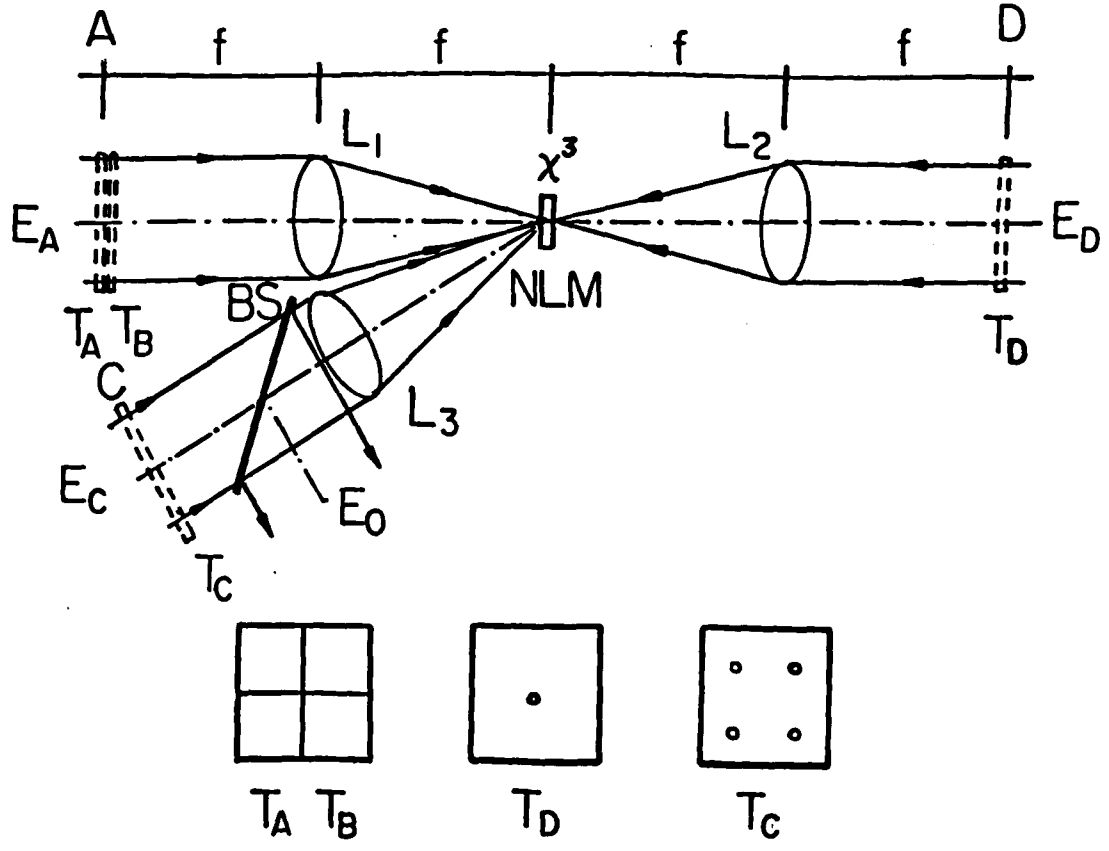


Fig.5.2.2 OPC implementation of a correlation type parallel logic processor. L_1, L_2 and L_3, three equal-focal-length Fourier transform lenses; BS, beamsplitter; NLM, nonlinear material; E_A, E_D and E_C, collimated input beams; E_O, output beam; T_A and T_B; two coded input masks superposed in the plane A; T_D, a mask containing a central δ function placed in the plane D; T_C, a logic operation mask placed in the plane C.

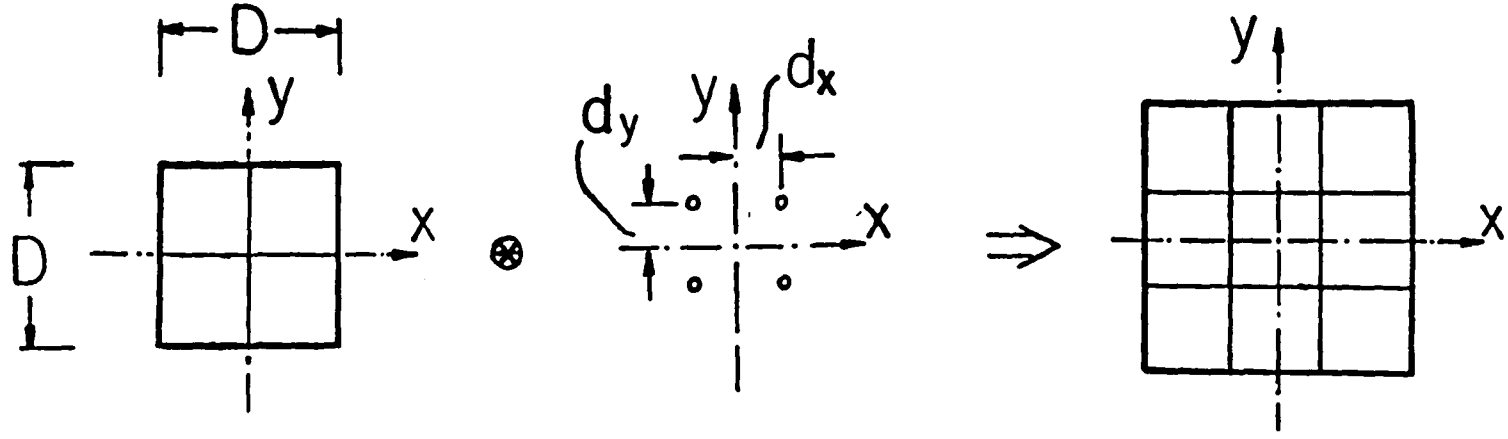


Fig.5.2.3 The correlation process of the overlapped inputs with four shifted δ functions. D, width of coded input variable mask, d_{x_i} and d_{y_i}, displacements of the i^{th} δ function; (left): overlapped inputs containing four possible illuminated areas (see the left part of the Table 5.2.1); (middle): four shifted δ functions; (right): the correlation result containing nine possible illuminated areas.

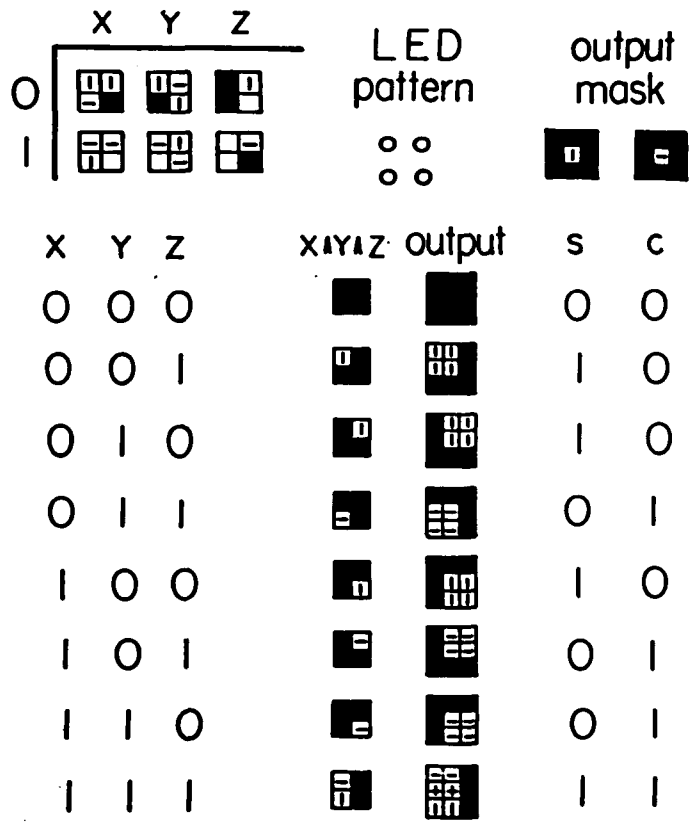


Fig.5.3.1 Optical binary full adder operation using polarization encoded pattern logic. At the output, orthogonally polarized patterns correspond to the sum and carry results, respectively.

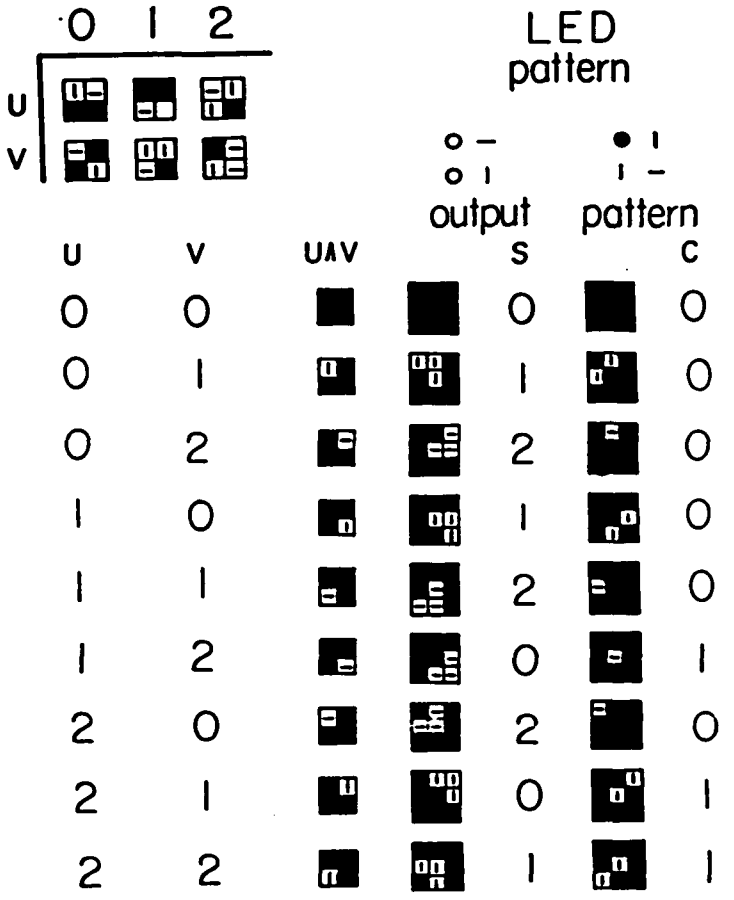


Fig.5.3.2 Optical ternary half-adder operation using polarization encoded pattern logic technique. The output sum values, 0,1 and 2, are encoded as opaque, y - and x - polarized signals, respectively. For the carry, both polarizations are used.

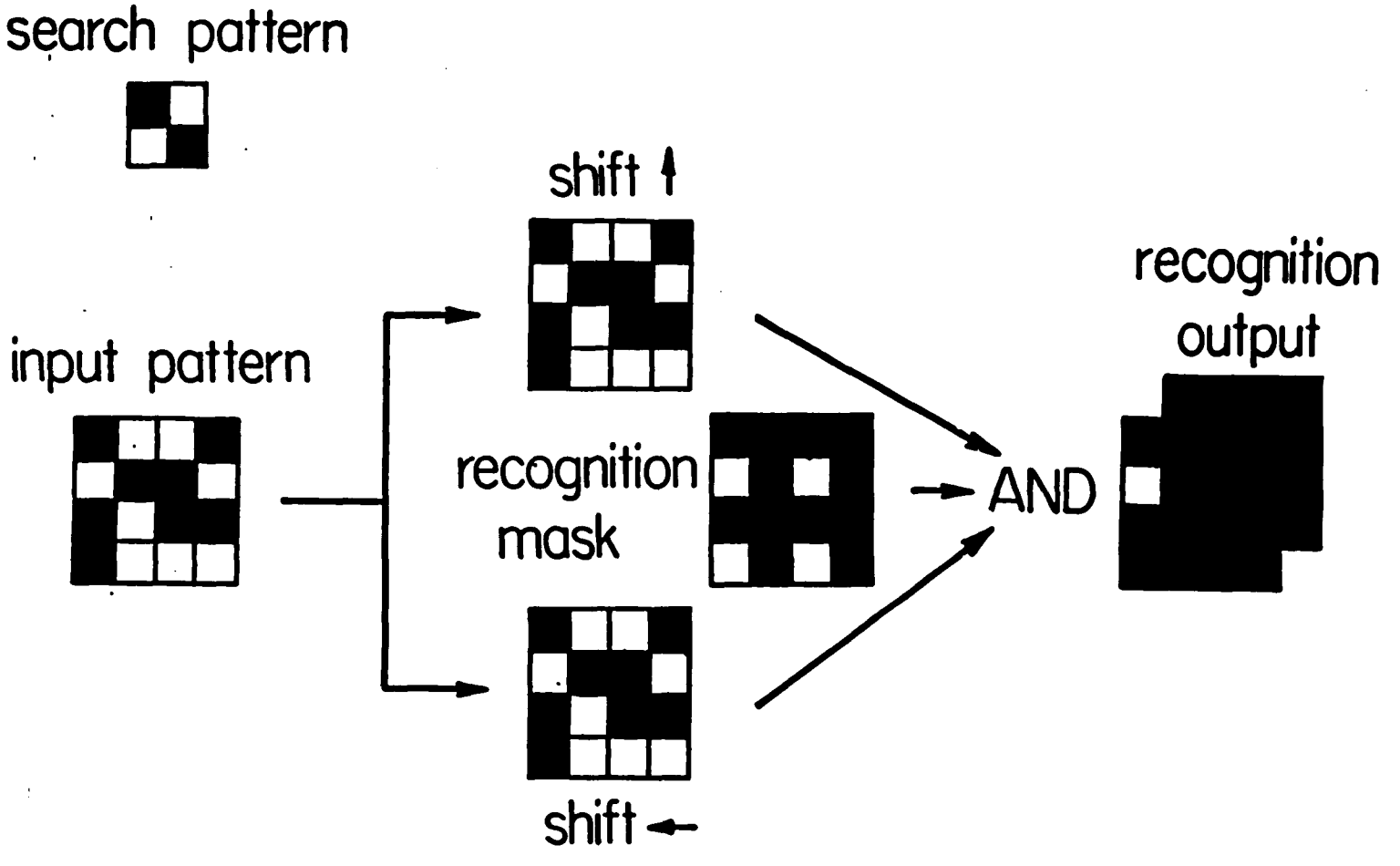


Fig.5.4.1 Example of a four-pixel type-B pattern recognition. To locate the search pattern, two copies of the spatially shifted input are directed, together with a recognition mask, to a three-input parallel AND device.

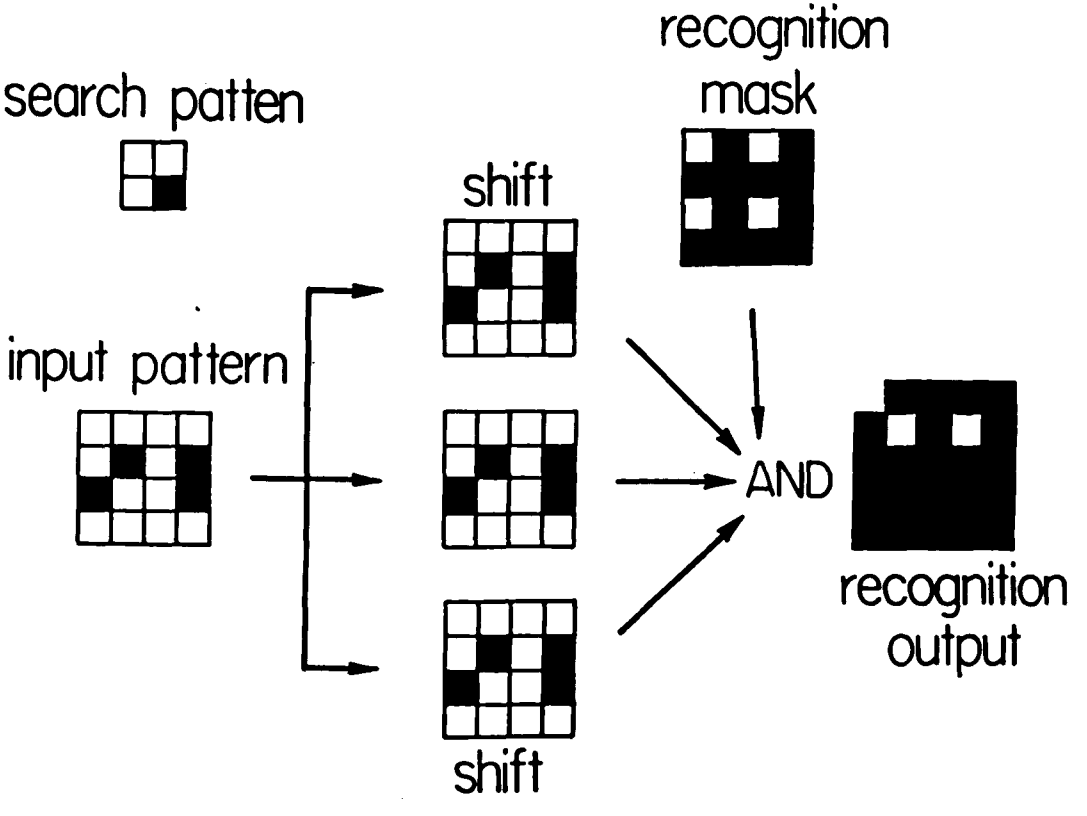


Fig.5.4.2 Example of a four-pixel type-C pattern recognition. To locate the search patter, three copies of the spatially shifted input are directed, together with a recognition mask, to a four-input parallel AND device.

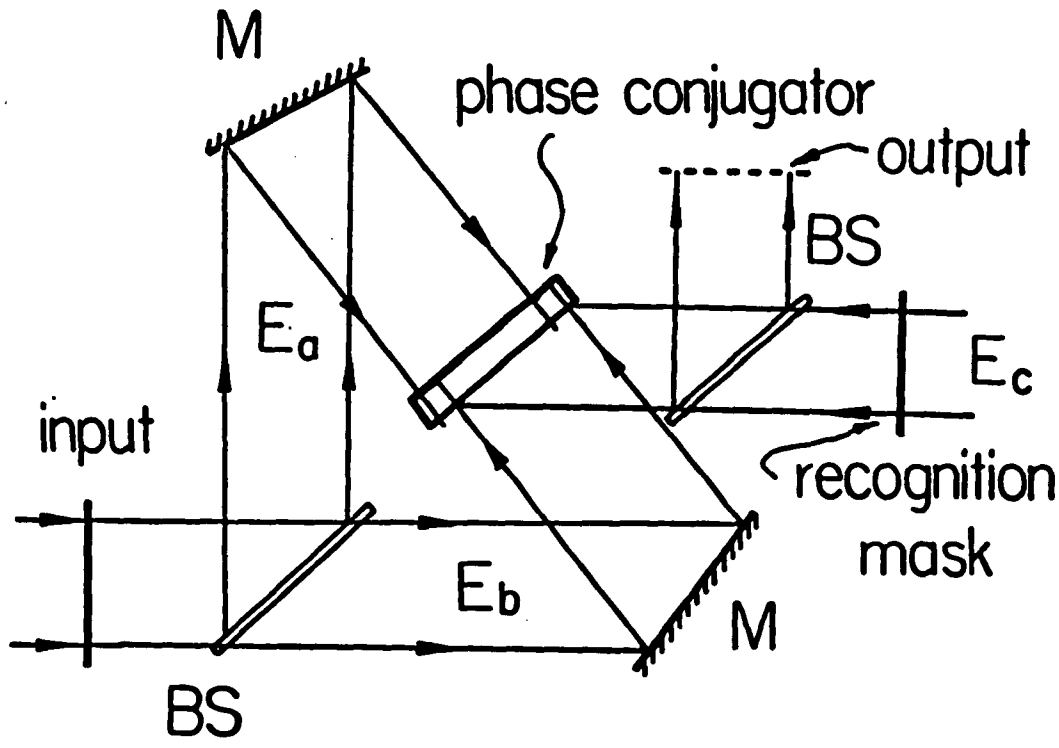


Fig.5.4.3 A schematic ultrafast OPC-based symbolic pattern recognition device. The duplication and spatial shift of the pattern are performed by mirrors and a BS. The recognition mask is inserted in E_C beam. The recognized result is directed by a second BS to the output port.

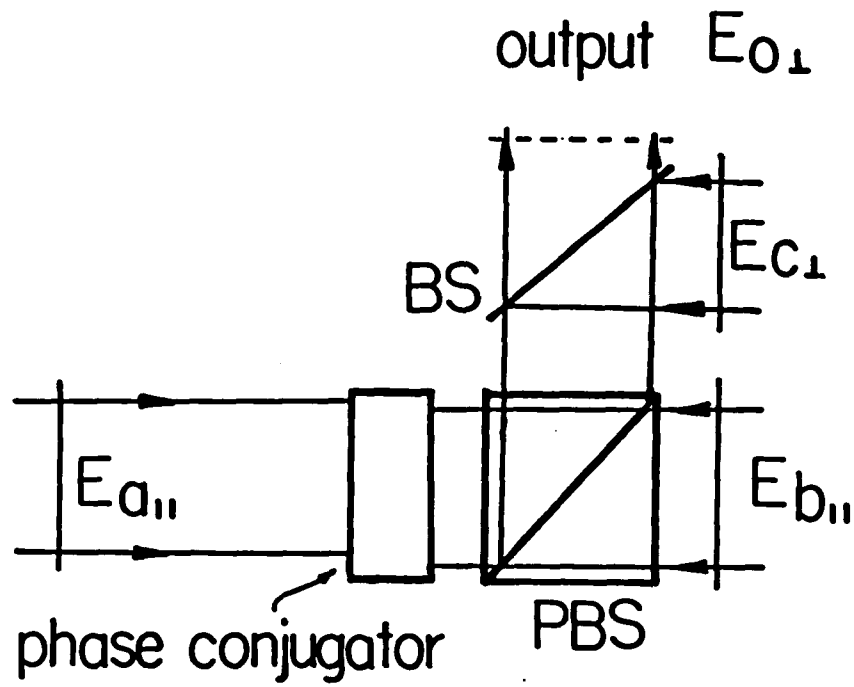


Fig.5.4.4 An alternative optical OPC-based symbolic pattern recognizer. With orthogonal polarizations, input $E_{b\parallel}$ and $E_{c\perp}$ are collinearly directed into the OPC material.

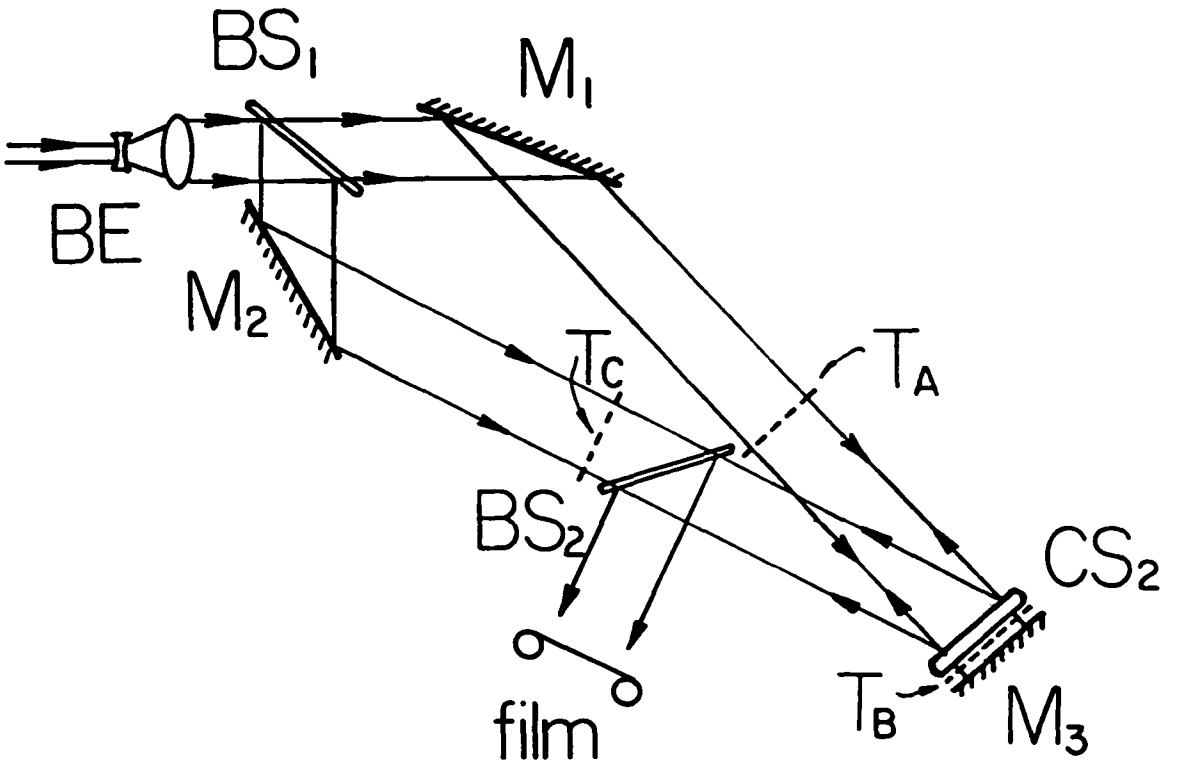


Fig.5.5.1 A picosecond OPC experimental setup. Using a beam expander (BE), a beam-splitter (BS_1) and two mirrors $M_{1(2)}$, two derived beams are guided with about 10° to a CS_2 cell. An end mirror M_3 is used so that the beam A is retroreflected. Three masks mounted on translational stages was inserted at places indicated in the diagram. The OPC signal is directed by BS_2 to a recording camera.

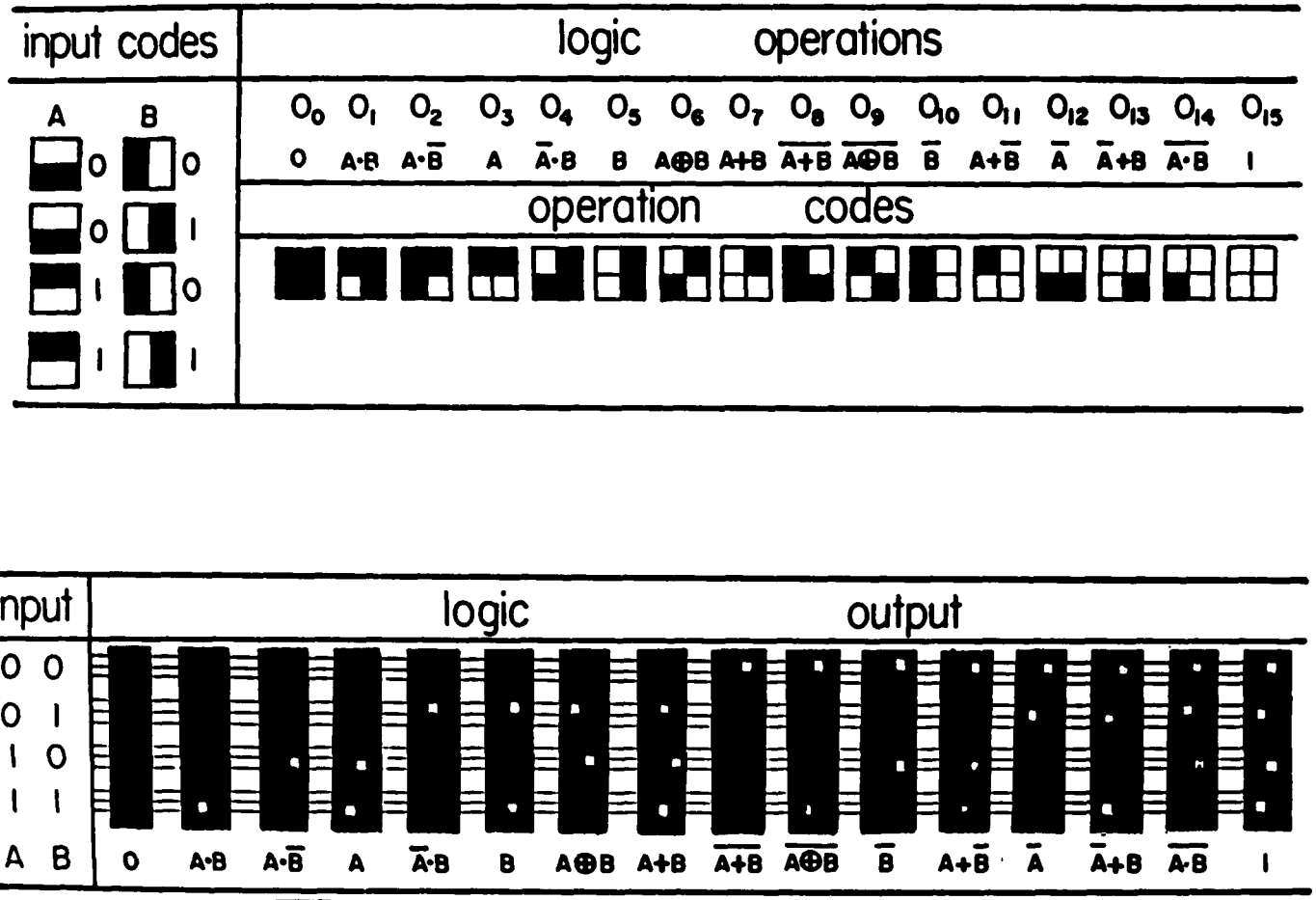
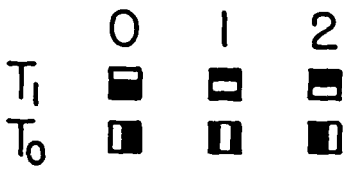


Fig.5.5.2 (a) input and operationl kernel mask encoding schemes for 16 binary two-variable logic operations. (b) the corresponding picosecond experimental results



T_1	T_0	B_2	B_1	B_0
0	0	0	0	0
0	1	0	0	1
0	2	0	1	0
1	0	0	1	0
1	1	0	1	1
1	2	1	0	0
2	0	1	0	0
2	1	1	0	1
2	2	1	1	0

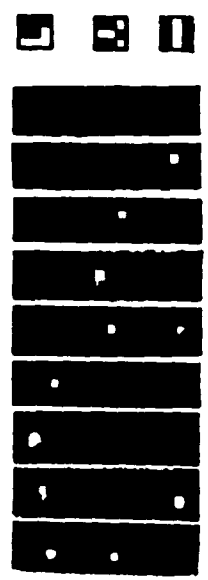


Fig.5.5.3 Truth-table, spatial encoding as well as the picosecond OPC experimental results of a 2-bit ternary-to-binary conversion operation.

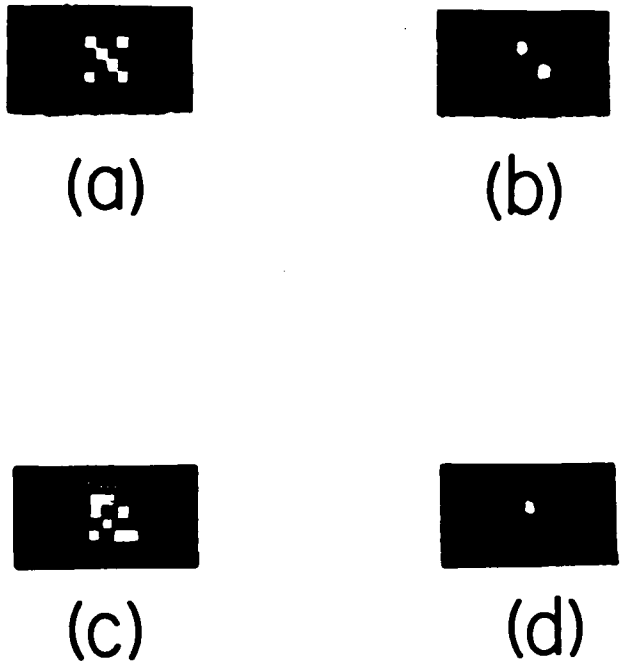


Fig.5.5.4 Experimental result obtained with a 32 ps Nd^{3+} YAG laser source and a 2 mm thick CS_2 cell. The input patterns (type B and C) that are shown in (a) and (C), while the recognized results are shown in (b) and (d), respectively.

VI. FAST OPTICAL INTERCONNECTION DEVICES

6.1, Introduction

In this chapter, we propose and investigate various new optical interconnection techniques. The interconnection is a very important part inside a digital computer. For various computation purposes, these elements serve as links to distribute and convert data between stages of either digital-digital or analog-digital processors. For a fast computation, both fast logi/arithmetic unit and a fast interconnect must be used. It has been indicated that due to some inherent problems, such as signal cross-talk and device interconnection bandwidth, the performance of the electronic interconnect is quite limited. Optics which can offer much larger processing bandwidth and interference-free parallel propagation opens a new door to implement efficient interconnection for digital processing and computing. In the following, a number of new methods to perform efficient optical interconnection for either analog-digital or digital-digital processors will be described. To convert an analog waveform to its digital representation, first, a sampling device is needed. Using the previously described Sagnac interferometric switch (SIS), an ultrafast all-optical sampler[1] is first discussed. To convert the sampled signal to its binary bit string, we propose to use the so-called optical theta-modulation (T-M) effect[2] to implement an EO serial to parallel A/D converter[3]. Following the discussion about optical A/D techniques, new methods to perform optical reconfigurable digital-digital interconnection are presented. In particular, optical implementations of various generalized perfect shuffles[4] and the dynamic cross-bar switching array[5] will be discussed.

6.2, Optical Analog-to-digital (A/D) Devices

6.2.1, SIS-based optical sampler

To translate a physical problem into a language that a digital computer can use, the first thing needed is to take the discrete samples of a continuous analog input waveform. These discrete samples can then be directed to a A/D converter that outputs binary version of these input data. To sample a continuous analog waveform, a switch that opens periodically to chop the input into segments can be used. Using optical Kerr effect, a nonlinear fiber- based optical sampler[6] has been demonstrated. The sampling frequency of this device is limited by the material relaxation time τ_o. Next, using the previously described SIS, a alternative method to implement an optical sampler is described. In principle, with the same material characteristics, the new sampler can operate at a frequency twice as high as that of the original fiber-based counterpart[1].

In Fig.6.2.1, a possible SIS-based sampler implementation is shown. The NLM cell is placed asymmetrically in the SI loop, i.e. with unequal distances from the NLM to the BS. The primary input beam is a continuous analog signal. For a good alignment and a 50/50 BS splitting ratio, and from an energy conservation argument, it can be shown that the cw beam, independent of its input intensity, will be totally retroreflected. That is, the output intensity I_o vanishes. This situation remains until an inducing pulse is incident on the NLM. For this pulse, an induced π phase change will probe two short time portions of the cw traveling wave beam. For each sampling pulse in the SI (see Fig.6.2.2(a)), two optical analog signal samples are obtained; i.e. the two output pulses, with the time interval equal to the traveling time difference, appear at the output O. The cell length is assumed to be shorter than the inducing pulse width, and therefore the overlap length, for two counter-propagating beams, are approximately the same. A train of N/2 sampling pulses results in a train of N discrete samples. The sampling period τ_s should be longer than the material relaxation time τ_o.

Since each sampling pulse generates two samples, the sampling frequency of the sampled analog signal can be twice as high as the input sampling pulse frequency. For a uniformly sampled signal, the NLM should be located in the loop such that the time difference between the NLM and the midpoint of the loop is equal to τ_s / 4. To deduce the condition for which the output signal frequency is equal to the sampling signal frequency, we define the parameter called the sampling signal group period τ_g (see Fig.6.2.2(b)):

$$t_g = 2 l_n / c \tag{6.2.1}$$

where l_n is the distance from the loop midpoint to the NLM cell and c is the velocity of light. The group period implies that there must be a time interval between every two groups of sampling pulse trains. Otherwise, the analog signal will be resampled. To obtain the largest group period, the NLM is placed immediately behind the beamsplitter. The maximum number of samples N_{max} resulting from each group of the sampling pulse is

$$N_{max} = \tau_g / \tau_s \tag{6.2.2}$$

When a high sampling frequency is required, the heating of the NLM due to high repetition of the inducing laser pulse should be considered. To minimize the heating effect, an alternative SIS optical sampler realization can be employed. Here, N uniformly placed NLM cells, located asymmetrically with respect to the BS, i.e. on one side of the loop midpoint in the SI, are used. The advantages of this configuration are that the low repetition rate laser can be used to perform the optical high frequency sampling and each NLM is allowed to have a longer relaxation time.

6.2.2, theta-modulation (T-M) based optical A/D converter

After obtaining samples of a continuous analog signal, in a second step, optical A/D conversion is in order. To keep up the overall optical processing speed, a fast optical A/D converter is needed. An existing electro-optic (EO) interferometric A/D converter[7,8] can perform conversions in the nanoseconds. However, for each single N-bit EO converter, N

waveguide interferometers are needed. Furthermore, because the periodic interferometric output is analog, to generate a digital number, an additional electronic comparator array must be used. In the following, a new approach to perform fast and efficient optical A/D conversion is described. In our approach, a theta-modulation (T-M)-based[3,9] EO device is used. This N-bit converter, that also can have a nano- or even sub-nanosecond response, requires only one active nonlinear element. Therefore, it is more compact and less power-hungry.

The key idea for an A/D conversion is the generation of a parallel set of different period periodic functions [7]. To achieve this goal, the EO interferometric approach uses a parallel set of active nonlinear EO modulators. It can be shown, that using a new T-M A/D converter, instead of using a large number of EO interferometric modulators and comparators, only one active and N parallel passive elements are sufficient.

The active element is a voltage controlled beam deflector that deflects a 1-D input beam to different spatial locations. There are a number of devices available to perform this function. For example, a variable grating mode SLM (VGSLM)[10] can generate, using different applied voltages, various spatial frequency gratings that diffract the incident beam to different 1-D locations. The EO beam deflector[11] uses a voltage tunable index-gradient to deflect the incident light. A streak-camera[12], commonly used for ultrafast laser pulse measurement, can also be modified to be a fast beam deflector. Recently, other fast, efficient and high resolution beam deflection devices, such as the EO internal reflection deflector[13], the waveguide modulator deflector[14], etc., have also been reported. Some of these devices, because of their small capacitances (order of pF), can operate at a high (nano- or even sub-nanoseconds) speed with a low (order of volts) driving voltage[22]. With these devices, the input voltages, corresponding to detected intensity levels, are optically mapped to different spatial locations.

To convert the spatially mapped 1-D light distributions to their binary representations, a parallel set of spatially encoded masks, representing a set of different period

periodic clipping operations, is used. For example, in Fig.6.2.3, for a four bit A/D conversion, four masks are shown. To illuminate the four parallel A/D conversion masks, the deflected optical beams must be focused (expanded) in the vertical (horizontal) dimension (see Fig.6.2.4). For a different horizontal-level bar, the light distribution at the mask output side represents its binary number code. Using a second cylindrical lens, the different level binary codes can be shifted to a common horizontal level where a 1-D detector array can be placed. One advantage of this new A/D conversion approach is that only a single active nonlinear element is required. Thus, in comparison with EO interferometric approach, the power consumption is drastically reduced. Also, electronic comparators are not required. Another advantage is, that by simply changing masks other binary output codes, such as Grey codes, can be obtained. Thus, this approach yields a more flexible A/D conversion scheme. With SLM generated masks, a programmable multi-purpose optical A/D converter can be implemented.

6.3, OPC-based Optical Cross-bar Interconnect

In the previous section, fast optical A/D conversion scheme has been described. The A/D device links between an input analog and an output digital processor. To perform digital computation, another type of interconnection that links between stages of digital processors is also needed. in other word, to perform various kinds of calculations, the output of one digital processor needs to be distributed into one or many subsequent digital processors. For a fast parallel computation, both fast logic and arithmetic processors and fast parallel data distribution or interconnection schemes are required. For digital optical computing, one of the popular parallel interconnection method is to use arrays of holograms each fabricated for a different diffraction angle[15]. For a specific interconnection problem, an array of fixed holograms is employed so that for different purposes, a large set of hologram arrays together with some optical multiplexing scheme are used. To reduce the heavy burden on large memory space, an optical dynamic interconnection device that can be reconfigured in real time to adapt to the changing computational requirements has long

been a research interest. It has been indicated that one way to implement this reconfigurable interconnect is to use the so-called optical cross-bar switch[5]. An N × N cross-bar can link signals between N input and output channels in such a way that any change in one link will not affect any other links (see Fig.6.3.1(a)). A generalized method to implement a free space propagation mode cross-bar switch has been proposed. With an input and an output cylindrical lens, N input and output channels are spatially expanded in one dimension to form perpendicular light bar arrays that arrive from both side to a 2-D N ×N switch array. The switches are controlled by electronic signals. For the physical implementation, an E-O deformable mirror-based cross-bar switch has been implemented[33]. Because the mirrors are physically deformed, the switching speed is limited. Also, this is an E-O approach that uses electronic signal to control optical beam deflections. Next, using an all-optical scheme, an OPC-based cross-bar switch is described.

In Fig.6.3.1(b), an OPC parallel processing device is shown. To form a 8 × 8 cross-bar switching array, eight input ($A_1 \cdots A_8$) and output ($B_1 \cdots B_8$) channels are used. The input beams are expanded vertically into eight light bars incident to the OPC material. Oppositely, an array of 8 × 8 switching beams are directed to the OPC material. The third input that is a full beam size input is used as a power supply. To switch, as an example, the signal from A_1 to B_8, only one switching beam, the one located at the switch array lower left corner, is turned on while all other 63 beams are off. Correspondingly, the OPC signal will be guided, through the output beamsplitter and the cylindrical lens, to the output port B_8. As another example, the switching of the signal from all eight input ports $A_1 \cdots A_8$ to a single output port B_8 is performed. In this case, $A_1 \cdots A_8$ together with all eight bottom switching beams are on. The eight OPC outputs will be guided, through the cylindrical lens, to an identical output port B_8. Compared to the existing scheme, the major advantage of the OPC-based approach is that all-optical reconfigurable interconnection can be performed. Another advantage is that the use of OPC phenomena allows the ultrafast processing speed. In addition, using a slight modification that inter-

changes the power supply port with the input channels, functions of input and output can be interchanged so that two-way cross-bar interconnections can be implemented.

6.4, Optical Generalized Perfect Shuffle Interconnect

To distribute and to interconnect massive amounts of data between stages of parallel processing elements, in addition to cross-bar interconnect, other fast and efficient interconnection networks are also needed. It has been indicated, that for some applications, shuffle-exchange networks[16-18] are very effective in handling such data interconnections. Shuffle-exchange networks are implemented using repeated stages of the so-called perfect shuffle (PS) together with arrays of exchange boxes that can independently either exchange or bypass the adjacent lines. Different combinations of PS and exchange box arrays have found applications in evaluating polynomials, in sorting data, in transposing matrices, as well as in computing the fast Fourier transform.

Given the inherent parallelism of optics, interest has been focused on developing parallel optical computing architectures, and in particular, on the implementation of optical shuffle-exchange networks. Goodman et.al.[19] and Marhic[20] proposed the use of optical fibers or waveguides for an OPS. However, for large data arrays, large bundles of fibers are needed. To take full advantage of the free-space propagation property of optical waves, Marhic[20], Lohmann et. al.[21,22] and Brenner and Huang[23] suggested the use of unguided implementation approaches. An unguided OPS consists of either a hologram or a suitable lens and prism combination. While the holographic OPS requires monochromatic light inputs, the lens/prism based counterpart can also be used with white light illumination. In this section, some more efficient and compact unguided OPS geometries are suggested. Also, an implementation of an optical generalized PS (OGPS) is discussed.

6.4.1, Optical perfect shuffle

The PS $P_N(i)$ is defined as[2]

$$P_N(i) = (2i + [2i/N]) \bmod N \qquad 0 \leqslant i \leqslant N-1 \quad (6.4.1)$$

where $N = 2^j$, i and j are integers and $[2i/N]$ represents the largest integer that is less than or equal to $2i/N$. shown. When binary symbols are used as input line addresses, after a PS permutation, the binary addresses of the output lines represent a right shift operation. Using this PS cyclic shift permutation property together with arrays of exchange boxes, any address configuration can be permuted into any other configuration on the order of $(logN)^2$ steps[18].

In the stretch-mask-add approach[22], the unguided OPS consists of four prism wedges and two positive spherical lenses with focal lengths f_1 and f_2, respectively. Correspondingly, the total length of the system is $2f_1 + 2f_2$. To maintain the same output channel spacing as that of the input, the length f_2 must be twice the length of f_1 leading to a total optical system length $6f_1$.

A more compact OPS, using a new unguided OPS implementation is suggested here. A PS requires that half of the inputs diverge by a factor of two while they interlace with those from the second half inputs. To obtain this divergence, a negative cylindrical lens may be employed. In Fig.6.4.1(a), a negative cylindrical lens based OPS is shown. Here, side by side, two identical aperture (D) and focal length (f) negative lenses are used. For simplicity, the sketch shows plano-concave negative lenses, where the unused portions of the lenses are not shown. Collimated input beams illuminate the plane of the lenses, where the input mask is located. The output beams, at the back focal plane of lenses, represent the shuffled result. For an N-bit input, using geometric optics, the bit or channel period (d) and spot size (a) are determined by

$$d = \frac{D}{N-1} \qquad (6.4.2)$$

and

$$a \leqslant \frac{D}{2(N-1)} \qquad (6.4.3)$$

Because the output spot size is magnified by a factor of two, the input spot size (Eq.(6.4.3)) is constrained to one half of the input bit period - d. For example, if the input bit spot size a and their spacing d is 0.1 mm and 0.25 mm, respectively, a 50×50 mm^2 aperture OPS can optimally handle as many as 40,000 light channels. As compared to the stretch-mask-add approach, this system is more compact since it has only two optical elements while its length is reduced by a factor of six. With this method, the size of the output bit is identical to the stretch-mask-add approach spot size. However, because this OPS generates a divergent output, in a shuffle-exchange network, the exchange boxes must be able to recollimate the optical beam. When a two-port optical waveguide switch is used as the exchange-box, by proper front and back lens adjustments, the beams can be demagnified to their original sizes. This compact OPS can also be implemented with large aperture reflective optical elements, i.e. two identical, side by side, radius R convex cylindrical reflective surfaces (see Fig.6.4.1(b)). If necessary, the output spots can be separated out by a beamsplitter. In either case, the divergence operations are performed by two identical components (lens or mirror).

It is also possible to generate the required operations with only a single negative cylindrical optical element (lens or a mirror). In Fig.6.4.1(c), the use of a single cylindrical lens based OPS is illustrated. First, using a single negative lens, the two divergence operations are performed. Second, using two prism wedges, each half of the diverging results is stretched and interlaced together to generate the final OPS output.

6.4.2, Optical generalized perfect shuffles

Next, an optical implementation of a generalized PS (GPS)[24] is described. The interest in GPS stems from the fact that in many applications, instead of using $N = 2^J$ inputs, the use of other composite integer (M) inputs are required. A GPS ($G_{k,n}(i)$), characterized by the two integers k and n ($k \geq 2, n \geq 2$), such that the total number of inputs M ($M = kn$), is defined as[24]

$$G_{k,n}(i) = k\ i\ + [i/n](1 - M). \tag{6.4.4}$$

In Fig.6.4.2(a), some details of the GPS permutation formula, while in Fig.6.4.2(b), a corresponding permutation example are illustrated. Here, both the input and output ports are divided into k and n groups, respectively. In each of the k input groups, for example, in the j^{th} group, there are n input lines that are to be distributed to a fixed place (the j^{th} line as in the example) in each of the n output groups. Note, that a PS $P_N(i)$ is a special case of GPS, i.e. $G_{2,N/2}(i)$. Since for each of the k input groups an identical magnification divergence operation is performed, for an OGPS implementation, k pieces of either transmisive or reflective optical elements, cut from either identical focal length negative cylindrical lenses or identical radius cylindrical reflective surfaces, can be utilized. In Fig.6.4.3, using transmisive optical elements (a negative cylindrical lenslet array), three OGPS cases: $G_{3,2}(i)$, $G_{3,3}(i)$ and $G_{4,2}(i)$, are illustrated. In general, for each of k identical size elements the aperture A is

$$A = \frac{2D}{M-1} \tag{6.4.5}$$

Because the OGPS output is collected at a distance $(k-1)f$ measured from the input plane, as compared to input, the output diverges by a factor of $k-1$. Thus, the input bit or channel size must be chosen as

$$a \leqslant \frac{D}{(k-1)(M-1)} \tag{6.4.6}$$

While this method can be used for arbitrary k and n, because of the beam divergence, it is only practical for relatively small k's.

6.5, Summary

In this chapter, we have described a number of new optical interconnection schemes. For the interconnection between an analog input and digital output port, optical sampling

and A/D devices are required. In our approach, an nonlinear optical SIS has been modified to perform fast sampling operation. With this device, the highest sampling frequency can be twice as high as that of any existing optical sampling device. We have also described an optical T-M-based A/D converter that uses only one active nonlinear element to perform fast A/D conversion. With this compact, more efficient geometry, sub-nanosecond A/D conversion can be expected. Following the discussions on optical A/D techniques, we have presented an OPC-based parallel reconfigurable interconnect scheme. Compared to the conventional deformable-mirror approach, this new OPC scheme can offer pico- or even sub-picosecond interconnection speed. In the last section, a number unguided optical perfect shuffle geometries have been proposed. Using either a pair of negative cylindrical lenses or convex reflective surfaces, either transmisive or reflective perfect shuffle can be implemented. Compared to the stretch-mask-add approach, this method uses fewer optical elements and a more compact geometry. The method can also be generalized to implement an optical generalized perfect shuffle.

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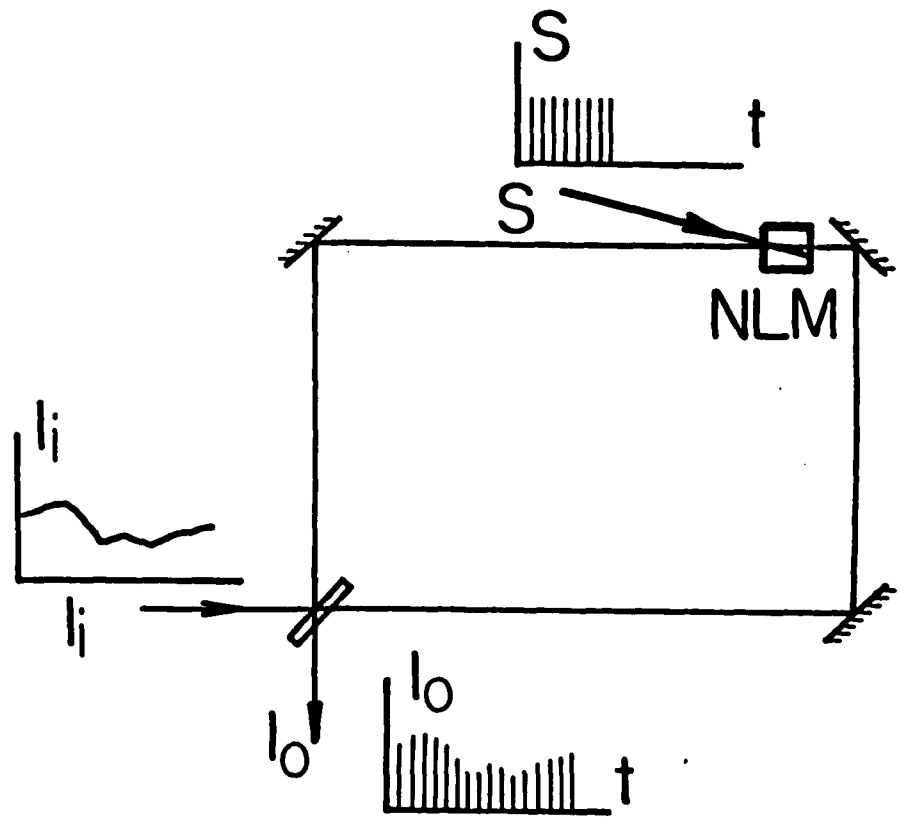


Fig.6.2.1 SI-based optical sampler. I_i, optical analog input signal; S, sampling; I_o, sampled output signal.

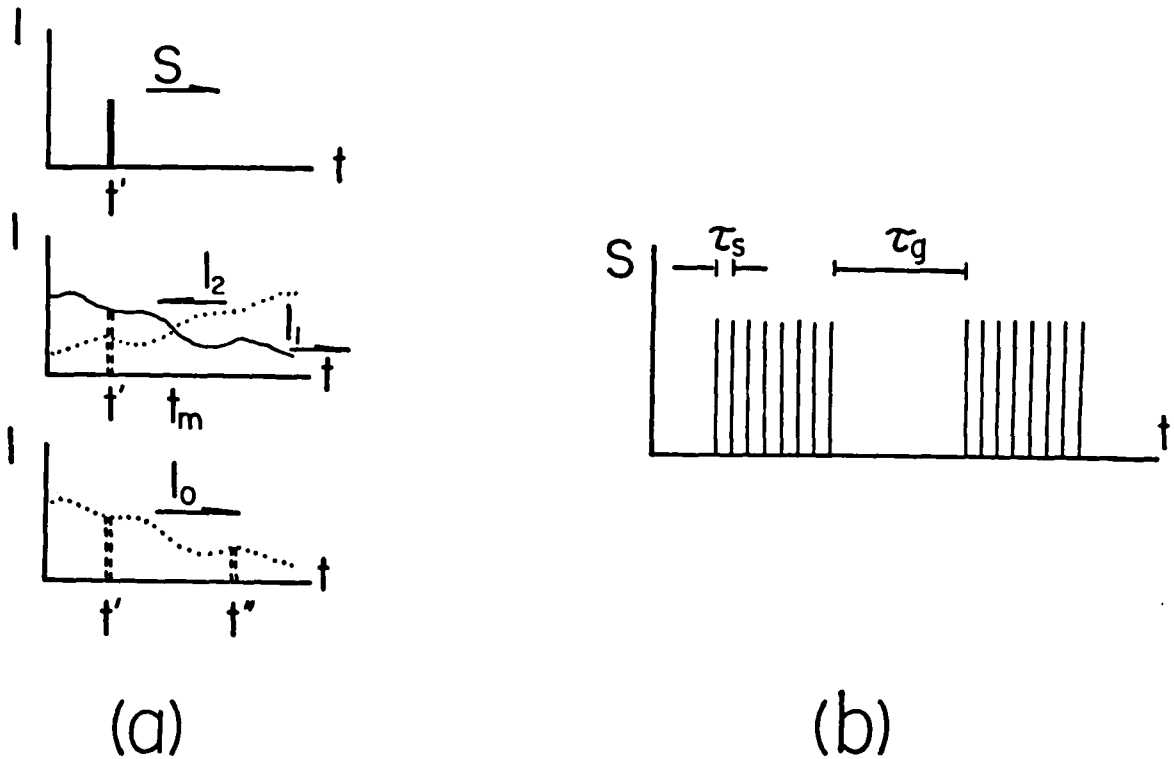


Fig.6.2.2 (a) Time diagram of an SI optical sampler. t', sampling pulse arrival time; $I_{1(2)}$, two counterpropagating analog signal wavefronts in the SI; t_m, time corresponding to the midpoint of the SI loop; I_o, sampled output. (b) sampling pulse sequence with sampling period, τ_s, and sampling pulse group period, τ_g.

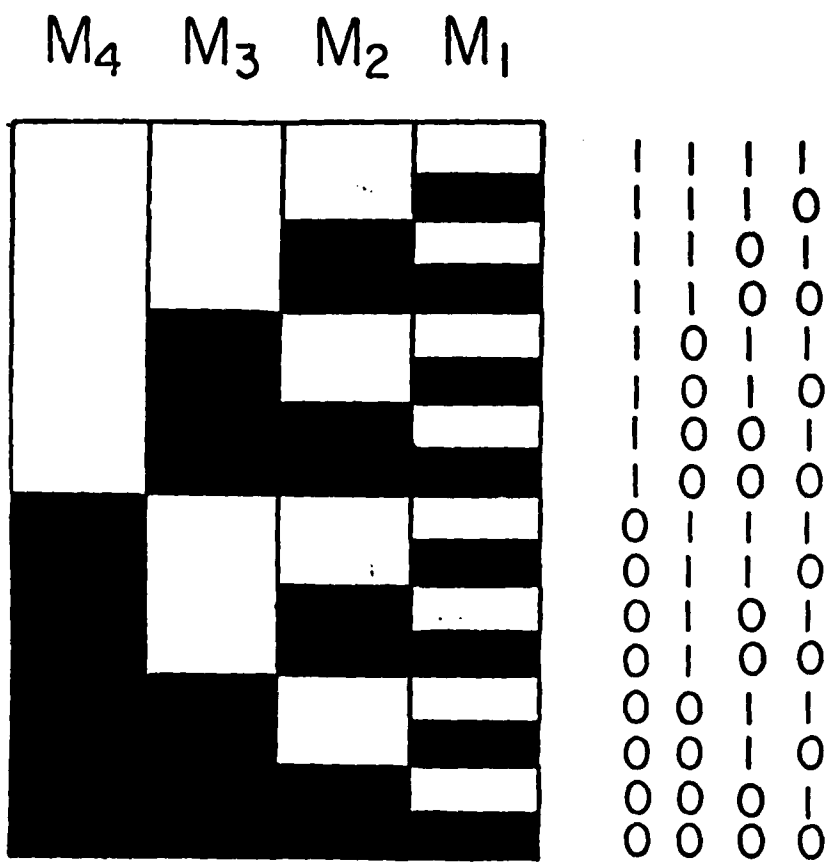


Fig.6.2.3 Four (M_1-M_4) binary masks to be used for a 4-bit optical T-M A/D conversion.

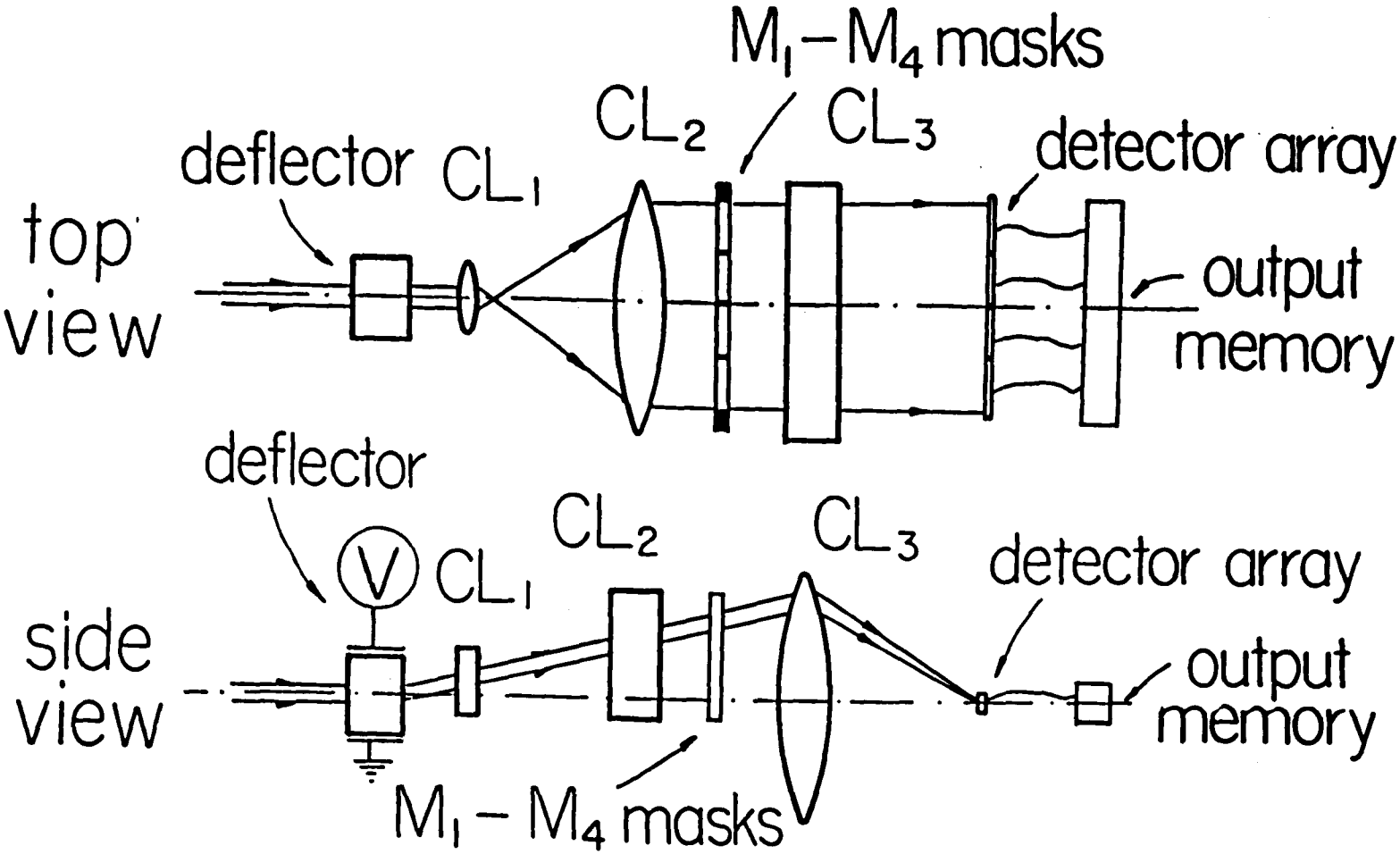


Fig.6.2.4 Schematic diagram of a optical T-M A/D converter. (a) and (b) are top and side view of the device. The beam passing through a voltage controlled beam deflector is expanded in horizontal direction to form a deflected light beam bar to be incident on the binary masks. Using a second cylindrical lens, the converted results are shifted to a common level. At this level, a 1-D detector array

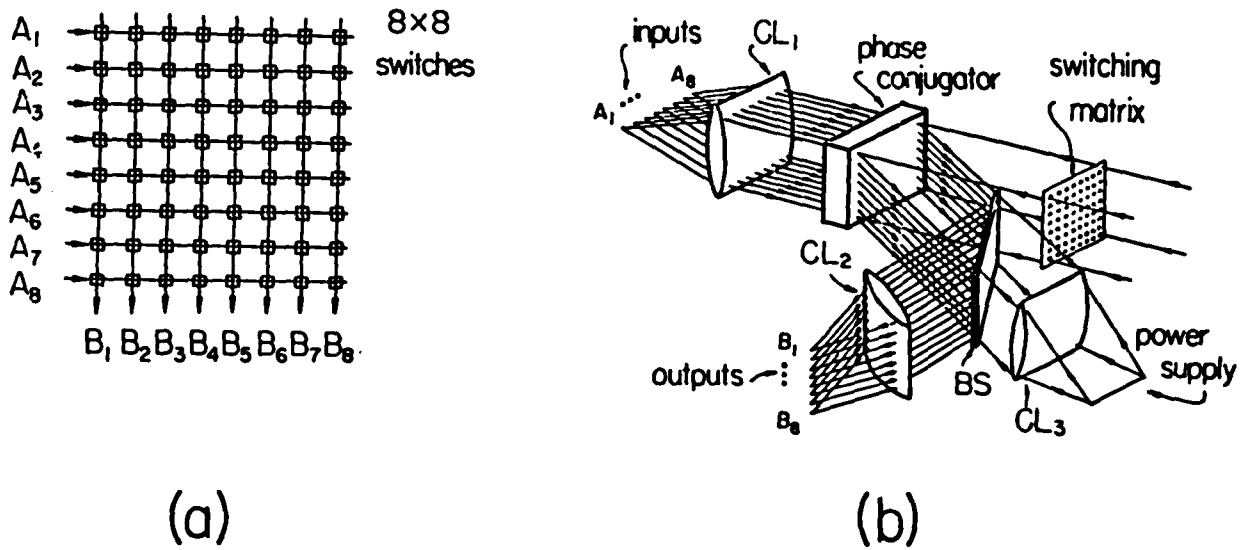


Fig.6.3.1 (a) A 8 × 8 cross-bar interconnect, and (b) its OPC-based optical implementation.

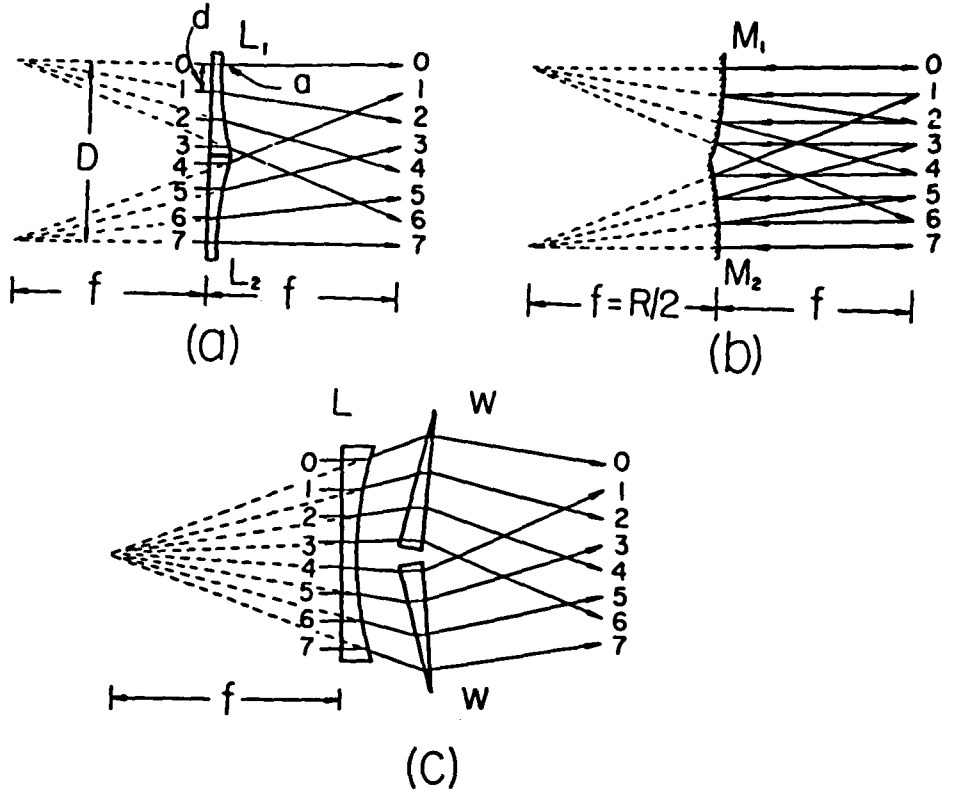
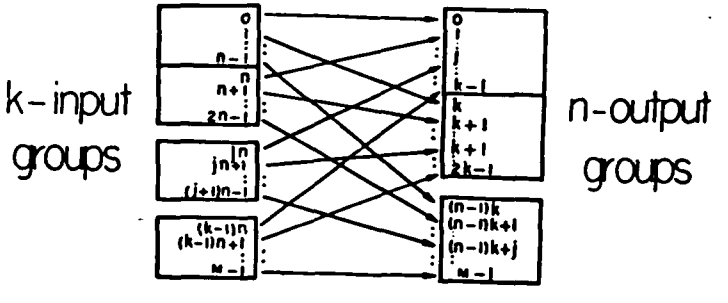


Fig.6.4.1 Schematic diagrams of an OPS where D is the system aperture, a the input channel size, and d the channel spacing. (a) A lens based system. L_1 and L_2, two identical focal length (f) negative cylindrical lenses. (b) A cylindrical mirror based system. R, radius of the cylindrical mirror. Using a beamsplitter, the output can separated. (c) An alternative lens based system where a single negative cylindrical lens together with two identical prism wedges are used.

$$G_{k,n}(i) = \begin{cases} ki & \text{if } 0 \le i \le n-1 \\ ki+1-M & \text{if } n \le i \le 2n-1 \\ \vdots & \vdots \\ ki+j(1-M) & \text{if } jn \le i \le (j+1)n-1 \\ \vdots & \vdots \\ ki+(k-1)(1-M) & \text{if } n(k-1) \le i \le M-1 \end{cases}$$

(a)



(b)

Fig.6.4.2 Generalized PS permutation interconnection. (a) A more detailed input and output relation. (b) A graphical example showing the input and output relation. Note that both the input and output are each divided into k and n groups.

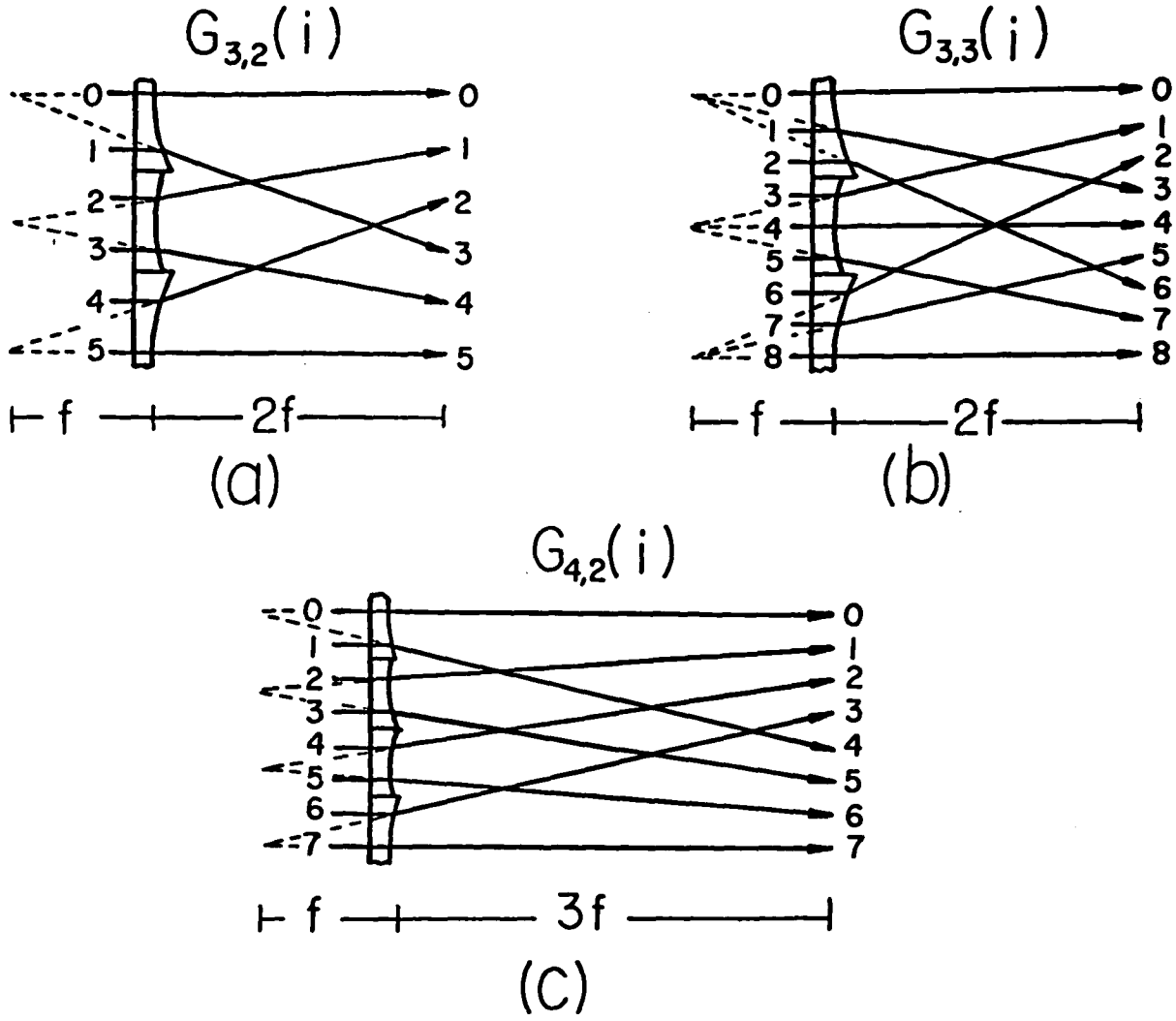


Fig.6.4.3 Three, lens-based, OGPS implementation examples. (a) $G_{3,2}(i)$, (b) $G_{3,3}(i)$, (c) $G_{4,2}(i)$.

VII. OPTICAL BINARY ARITHMETIC PROCESSORS

7.1, Introduction

For arithmetic computation, two fundamental operations are addition and multiplication. Based on these two operations, many useful linear algebraic operations can be implemented. To perform digital optical arithmetic computation, research has been performed to develop optical addition and multiplication methods. In this chapter, we propose a number of new techniques for implementing optical addition and multiplication. In the first section, a two-port Sagnac interferometric switch (TPSIS) based optical full adder[2] is described. Using this full adder, the implementation of an array multiplier[2] will then be described. An alternative method to perform binary multiplication is to use the so-called digital multiplication via analog convolution (DMAC) algorithm[3,4]. In the second section, a number of new DMAC processors for binary scalar multiplication[5,6] will be proposed. Using ultrafast SHG switching array, optical DMAC processors are described. Finally, the SHG-based techniques to perform DMAC-based vector and matrix algebraic operations[7] will also be discussed.

7.2, TPSIS-based Optical Binary Arithmetic Processors

7.2.1, TPSIS optical binary full adder

In this section, the optical TPSIS implementations of a binary adder as well as a binary multiplier are described. The binary full adder logic functions are

$$S_i = A_i \oplus B_i \oplus C_i \qquad (7.2.1a)$$

$$C_{i+1} = (A_i \bullet B_i) \oplus (B_i \bullet C_i) \oplus (C_i \bullet A_i) \qquad (7.2.1b)$$

where notations $\bullet$ and $\oplus$ denote the logic AND and EOR functions, A_i and B_i are i^{th} bits of two input binary sequences, S_i and C_{i+1} are the sum and the carry, generated from the i^{th} bit addition, outputs. In Fig.7.2.1, a schematic diagram of an optical full adder is shown. Although a complete full adder can be implemented using either NAND or NOR gates only, here, its implementation with a combination of EOR and AND gates, is shown. Using the parallel processing property of the TPSIS requires that only two interferometers be employed; one for the generation of the ANDs and another for the generation of the EOR functions. The sum output S_i, specified by Eq.(7.2.1a), is generated at the left TPSIS through a three input EOR function. The other right side TPSIS, performs the three AND functions: $A_i \bullet B_i$, $B_i \bullet C_i$ and $C_i \bullet A_i$. To obtain the carry C_{i+1}, specified by Eq.(7.2.1b), the three optical signals are then guided to the left TPSIS. Finally, the carry is fed back to the input side for the next bit addition, and the sum is stored outside in an optical register. Several half-wave (H) retardation plates are used for polarization matching. Because two linear polarizers are used for the optical retroreflection isolation, there is no feedback signal to the input. Notice, that in this schematic diagram, the optical delay elements necessary for both input and output synchronization are not shown. For the practical device, proper optical delay elements need to be added to our circuit diagrams.

7.2.2, TPSIS optical binary array multiplier

The multiplication of two binary number sequences can be performed in a number of ways. In the indirect multiplication method it is performed by "shift and add" algorithm. To do this, an accumulator for holding the partial sums of the multiplication and a shift register for the left or right shifting, are required. In this section, another method called the array, also called a Brown multiplier[10] for the multiplication of two binary unsigned numbers is described. Using this method, only optical full adders and logic AND gates are needed. The multiplication speed for this device is faster than that for indirect

multiplication. Consider two integers: $A = a_{m-1}\, a_{m-2} \cdots a_0$ and $B = b_{n-1}\, b_{n-2} \cdots b_0$, where the digits are binary integers, with their magnitudes as

$$|A| = \sum_{i=0}^{m-1} a_i\, 2^i \qquad \text{and} \qquad |B| = \sum_{j=0}^{n-1} b_j\, 2^j \tag{7.2.2}$$

The product of the two unsigned numbers can be expressed as

$$|P| = |A \;\; B| = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} (a_i\, b_j)\, 2^{i+j} = \sum_{k=0}^{m+n-1} P_k\, 2^k \tag{7.2.3}$$

where

$$P_k = \sum_{i+j=k} (a_i\; b_j)$$

To perform a binary array multiplication, only binary full adders and AND gates are required. It can be shown that for a $m \times n$ bit product, $m\,(n-1)$ identical full adders and mn AND gates are needed. As an example, an optical TPSIS implementation of a 3×3 binary array multiplier is discussed. In Fig.7.2.2(a and b), a flow diagram and its TPSIS implementation are shown, respectively. On the left side of Fig.7.2.2(b) are six input lines, three for multiplicands: a_0, a_1, a_2 and the other three for multipliers: b_0, b_1, b_2. Next to these input lines are nine AND gates arranged in three groups. Nine AND outputs from top to bottom are $a_0 \bullet b_0$, $a_0 \bullet b_1$, $a_0 \bullet b_2$; $a_1 \bullet b_0$, $a_1 \bullet b_2$, $a_1 \bullet b_1$ and $a_2 \bullet b_0$, $a_2 \bullet b_1$, $a_2 \bullet b_2$. These nine outputs are then guided into the right side full adder array. To satisfy power-matching conditions, the fan-out for these AND gates must be pre-calculated. Here, we assume each of the gates has enough power to drive subsequent full adders. Since a detailed illustration of an optical full adder has already been discussed, therefore, for simplicity, only the block diagrams of these full adders are depicted. Symbols X, Y and C_i are for two input signals and input carry, respectively. The output symbols S and C_o denotes the sum and carry-out results. On the right side of the full adder array, there are six lines

denoted by P_0 - P_5. These are the output channels represent the final multiplication result. Notice that since the structure is regular and only binary full adders and AND gates are used, the method is very suitable for optical VLSI design.

7.3, SHG-based Optical Scalar Multiplication Processors

7.3.1, DMAC algorithm

The magnitude of the product of two N-bit binary numbers, $A = \sum_{i=0}^{N-1} a_i\ 2^i$ and $B = \sum_{j=0}^{N-1} b_j\ 2^j$, can also be expressed in two steps as[4]

$$| P | = | A\ B | = \sum_{i=0}^{2(N-1)} C_i\ 2^i \qquad (7.3.1a)$$

where

$$C_i = \sum_{k=0}^{i} a_k\ b_{i-k} \qquad (0 \leqslant k \leqslant N-1) \qquad (7.3.1b)$$

is the i^{th} digit weight of resulting product in a mixed-binary format[2]. Eq.(7.3.1b) can also be interpreted as a i^{th} digit result from the two number sequence convolution. To obtain this multiplication, the conventional approach uses a shift and add scheme. To perform the digital multiplication of two N-bit numbers, after forming partial products, N-1 parallel adders are used. The additions can be performed in $[\log_2 N]$ stages, where $[x]$ denotes the smallest integer that is larger than x. With the digital multiplication via analog convolution (DMAC)[3,4] algorithm, after performing a digital convolution on the two numbers and converting, using an A/D element, the mixed-binary partial product to its binary form, only $[\log_2(N+1)]$-1 parallel adders in $[\log_2(\log_2(N+1))]$ stages are needed. As a numerical example, in Fig.7.3.1, the multiplication of two 7-bit numbers, A=1011011 and B=1111111, is illustrated. The convolution of the two bit strings yields the mixed-binary partial result C=1123345443221. Since the maximum weight is less then or equal to a seven, an array of 3-bit optical A/D converters are required. In the middle part of Fig.7.3.1, the converted

results are shown. When this result is properly grouped, only two parallel addition stages are required. With these stages, the final multiplication result C=1011010010010 will be generated. In principle, the DMAC algorithm offers a faster processing speed. Since optics offers ultrafast processing speed and parallelism, optical DMAC processors have been proposed With a conventional optical serial DMAC processor, to perform an optical digital convolution, two acousto-optic (AO) deflectors, actuated by electronic pulse trains representing the binary serial inputs, are used. Because of the serial input format, the convolution of two N-bit numbers requires 2N temporal cycles, cycles that are limited by the acoustic wave propagation speed and the AO material response time. For example, the convolution of two 16-bit numbers[10], with the currently available AO cells takes approximately 64 nanoseconds. After the convolution, to convert the mixed-binary result to binary number strings, parallel A/D converters are needed. An electro-optic (EO) interferometric A/D converter[11,12] can perform conversions in the nanoseconds. However, for each single N-bit EO converter, N waveguide interferometers are needed. Furthermore, because the periodic interferometric output is analog, to generate a digital number, an additional electronic comparator array must be used. Because for an N-bit serial-input digital multiplication, the DMAC algorithm requires an array of 2N-3 A/D converters resulting in a large number of active EO waveguide elements.

In the following, a number of new optical parallel DMAC (P-DMAC) processors are proposed. These processors consist either a time- or a space-integrating convolver[5-7], a fast theta-modulation EO A/D converter and an array of fast carry look-ahead adders.

7.3.2, SHG-based optical time-integrating data convolver

To perform a time-integrating DMAC preprocessing, a previously described SHG switching network can be used. As an example of this SHG-based time-integrating DMAC processor, consider the schematic setup shown in Fig.7.3.2. Let the two decimal numbers to be multiplied be A =13 and B =10. Their equivalent binary numbers are A =1101 and B =1010. The two spatially coded four channel binary numbers A and B arrive from the

left and bottom part of the network. In the diagram, the hollow arrow indicates the order of the number sequence progressing from the least significant (LSB) to the most significant bit (MSB). Since at each intersection a SH AND operation is performed, and since all the sixteen AND outputs (denoted by broken lines) are automatically aligned into seven output spatial channels (due to symmetric SH input and output channels), these SH output pulses yield the multiplication result C =1112010. This MBR output corresponds to the decimal number C =130.

To insure that at each AND gate the pulsed signals overlap, an input oblique time wavefront angle

$$\theta = \sin^{-1}[n_o(\lambda)\sin(\phi/2)] \tag{7.3.2}$$

is needed. Here, the use of negative uniaxial crystal where the ordinary index of refraction n_o is larger than the extraordinary index of refraction n_e is assumed. To obtain an oblique wavefront, either a diffraction grating or a composite prism[7] can be used.

For the multiplication of two N-bit inputs with bit spacing D and size d, a crystal thickness L, where

$$L = \frac{D(N-1)+d}{\tan(\phi/2)}, \tag{7.3.3}$$

is required. A material with a large ϕ reduces the required crystal thickness. Since the time interval, in the same channel, between two consecutive SH output pulses is the travel time difference between the input and the SH signals for the two autochannelized AND gates, the multiplication cycle time T for two N-bit numbers is

$$T = \frac{(N-1)D\,n_o(\lambda)\sin(\phi/2)}{c} \tag{7.3.4}$$

where c is the velocity of light in vacuum. With a KDP crystal and input wavelength λ=1064 nm, ϕ=20.3°, $n_o(\lambda)$=1.494, and choosing $D_i = 1mm$, the multiplication time for

two unsigned 16 bit numbers is about 14 ps. The actual multiplication cycle time depends on the used input pulse duration. Since the temporal width of a SH pulse is always shorter than the fundamental, the use of ultrashort laser pulses can lead to parallel, ultrafast processing.

Since the SHG uses an electronic nonlinearity and and assuming a pure crystal, there will be no appreciable induced thermal effect. Because this type of optical network leads to an input power depletion, to obtain N distinguishable output levels, a condition

$$\frac{(2k-1)}{2N}[1-(1-a)^N] > [1-(1-a)^{k-1}], \quad k = 1,2, \cdots N \qquad (7.3.5)$$

where a is the SHG conversion efficiency, needs to be satisfied. For example, for an 8-bit error-free multiplication, a maximum 6% SHG conversion efficiency is allowed. To prevent channel cross-talk, the SH output angular divergence must be restricted. For a input pulse with a bandwidth $\Delta\nu$, the SH output divergence angle β is[13] $\beta = p\,\Delta\nu / c$ where $p = (4.8 \pm 0.5) \times 10^{-5}$ rad/cm^{-1} and c is the velocity of light in vacuum. For a 10 ps pulse, this angle is a few mrad. As a single-stage parallel algebraic processor, the SHG-based approach is more compact and much faster than any of the existing E-O and A-O DMAC schemes.

For multi-stage operations, since it is necessary to convert the SH signal back to its fundamental frequency, a parametric frequency down-conversion and amplification scheme can be employed. It is well known[14], that to convert and amplify a weak SH signal back to its fundamental frequency and power using a parametric scheme, a strong third-harmonic (TH) pump beam is needed. The TH power density is[15]

$$\frac{P}{A} = \frac{1}{8}\left[\frac{n_1 n_2 n_3}{d_{ij}^2}\right]\frac{(\epsilon_0 c)^3 g^2}{\omega_1 \omega_2} \qquad (7.3.6)$$

where the subscripts 1,3 and 2 denote the weak SH, the strong TH input and the amplified idler output signals, while g and d_{ij} are the crystal gain and the second order

nonlinearity, respectively. To convert and amplify SH signals from 6% back to 100% power using a 1 cm thick $LiNbO_3$ ($d = 5\times10^{-21} MKS$) cell, about 50 MW/cm^2 pump power density is needed. To decrease this power density, a higher figure of merit M ($M = d^2/n^3$) crystal, such as an organic NPP[16] or a KNbO[17] crystal (where M is an order of magnitude larger than $LiNbO_3$) can be used.

To demonstrate the operational principle, in Fig.7.3.3(a), an experimental setup for the digital optical multiplication of two 2-bit binary numbers is shown. The inputs were 6-ps mode-locked Nd-glass laser pulses. A 1024 channel EG&G linear photodiode array was used to record the SH output. As the SHG material, a 1 cm thick KDP crystal with a 1 × 2.5 cm^2 rectangular aperture was utilized. For the binary encoding, two masks, each with two slits, were used. To ensure the correct overlap, the slit width and spacing were chosen as 0.5 mm and 1.2 mm, respectively. To minimize diffraction effect[13], both the input masks and the signal detection diode array were placed very close to the crystal surfaces. The array was covered both with a 1064 nm absorbing and neutral density filters. The detected signals were scaled and displayed on an oscilloscope. With all the four input slits open, a 3-bit output with intensity levels (1, 2, 1) was observed. In Fig.7.3.3(b), an oscilloscope trace showing the experimental result is illustrated. Due to some misalignment and convolution envelope function errors, the width of the center peak is somewhat larger than the two side peaks. Since for KDP ϕ is only 20.3°, with the current crystal, smaller bit size ($d = 100\,um$) and spacing ($D = 200\,um$) scheme can be used to process a longer bit string ($N = 8$). Also, crystals with larger ϕ, such as $LiIO_3$ ($\phi = 39.4°$ at $\lambda = 1064$ nm), can be used.

7.3.3, SHG-based optical space-integrating data convolver

Fast convolution can also be implemented with an optical outer-product processor followed by a space-integrator[6]. To optically represent the two multiplicands, two superposed, spatially encoded (with logic one (zero) as a transparent (opaque) pixel, respectively) masks are utilized. As an example, consider the multiplication of the two decimal numbers

A = 11 and B = 15. Their binary equivalents are A = 1011 and B = 1111. In Fig.7.3.4(a and b), the two spatially encoded masks, representing the numbers A and B, are shown. Here, between every two consecutive bits, an opaque pixel guard bit is used. To generate the two input vector binary outer-product, these two masks are cross-overlapped. The 2-D pixel array shadowgram formed behind the overlapped masks (see Fig.7.3.4(c)) represents the two input vector outer-product. To obtain the convolution, using a cylindrical lens aligned with the shadowgram's diagonal direction, the pixel light intensities are summed. The presence of the guard bit between every two consecutive data bits prevents cross-talk between the adjacent data channels. In Fig.7.3.4(d), the light intensity pattern slightly off the lens back focal plane is shown. The number of bars in each of the seven channels signifies the mixed-binary product C =1232211. In a practical implementation, a 1-D diode detector array is placed in the lens back focal plane. In that case, instead of counting the number of bars, the focal plane intensity levels represent the mixed-binary number (see Fig.7.3.4(e)). It is interesting to note, that for a coherent illumination, this detected signal is the dc component of the two 1-D data cross-ambiguity function[18]. The side lobe of the cross-ambiguity function may be used for error detection.

For the ultrafast optical implementation of this convolver, the SHG effect can also be used. Parallel encoded inputs are first spatially expanded to form 1-D light bars. Two light bar arrays representing two input numbers are then cross overlapped at the SHG plate to form the corresponding outer-product. The SH outer-product pulses can finally be summed with a 1-D lens to form the final convolution result.

7.3.4, The generation of final multiplication result

After performing optical convolution on two input multiplicands, the obtained multilevel convolution mixed-binary result can be directed to the previously described fast T-M A/D converter array. In Fig.7.3.5, a proposed real-time 4-bit optical digital multiplier is shown. Here, a SHG-based 4-bit parallel-input optical convolver is used to perform an ultrafast, optical digital convolution. At each convolution output channel, the mixed-

binary result is separately detected. The detected voltage signals are then used to modulate a beam deflector array. To convert the deflected beams to their binary representations, an array of A/D conversion masks are used. Finally, to generate the digital multiplication result, the partial results are directed to a fast carry look-ahead adder array. Recently, a new optical carry look-ahead addition algorithm was proposed[19] where using optical multiple reflections, the carries are generated optically with a light propagation speed. With this algorithm, a complete N-bit carry look-ahead addition needs only four operational cycles. Thus, using a set of cascadable ultrafast parallel optical logic switches[20], the implementation of a sub-nanoseconds optical carry look-ahead adders can be expected.

As mentioned earlier, for the multiplication of two N-bit binary numbers, $[\log_2(N+1)]$-1 additions in $[\log_2(\log_2(N+1))]$ stages are needed. With the DMAC scheme, the overall multiplication time is $T_C + T_{A/D} + [\log_2(\log_2(N+1))]\ T_A$, where the subscripts C, A/D, and A denote the convolver, the A/D converter, and the adder, respectively. Compared to the conventional multiplication scheme, the time needed for the last, the addition, part is drastically reduced. Compared to the serial-input DMAC scheme, this P-DMAC saves the convolution preprocessing time Using the proposed parallel vector outer-product-based optical convolver, an EO-based waveguide T-M A/D converter and a fast optical carry look-ahead adder array, the digital multiplication of two 32-bit numbers on the order of nanoseconds should be possible.

7.4, SHG-based Optical DMAC Vector And Matrix Multiplication Processors

The conventional method to multiply two binary numbers requires three operations: a logic AND, a shift, and an arithmetic sum operations. With the DMAC scheme, the multiple shift and sum operations are bypassed by using a mixed-binary representation. The mixed-binary representation allows the successive addition of several numbers before a final A/D conversion. More complicated algebraic operations, such as matrix algebra can also be decomposed into several multiplications and additions that can then be performed in parallel. For performing digital optical matrix algebra, several DMAC-based architectures

have been proposed[10,21,22]. In this section, using DMAC algorithm, various optical binary algebraic operations, such as vector-vector, matrix-vector as well as, matrix-matrix multiplications, are described.

7.4.1, optical vector-vector inner product processor

Given two N-dimensional (N-D) column vectors

$$A = \begin{vmatrix} a_1 \\ a_2 \\ \cdot \\ \cdot \\ a_N \end{vmatrix}, \qquad B = \begin{vmatrix} b_1 \\ b_2 \\ \cdot \\ \cdot \\ b_N \end{vmatrix} \tag{7.4.1}$$

the inner or scalar (dot) product of the two vectors is defined as

$$C = A^T B = [a_1 a_2 \cdots a_N] \begin{vmatrix} b_1 \\ b_2 \\ \cdot \\ \cdot \\ b_N \end{vmatrix} \tag{7.4.2}$$

$$= a_1 b_1 + a_2 b_2 + \cdots a_N b_N$$

Assuming all a_i (b_j) where $i, j \in (1,2,\ldots N)$ are either a zero or a one, Eq.(7.4.2) can be implemented with N number of AND gates and a summer. As an example, in Fig.7.4.1, the inner product of two 3-D vectors is considered. Two 3-bit parallel inputs are directed to a SHG crystal. The three intersection AND gates are aligned so that their outputs can be routed into a single channel. Using a time-integrating output detector, the detected inner product result is in a mixed binary form. This result can then be converted, using an A/D device, to its binary form.

7.4.2, optical vector-vector outer-product processor

The vector outer product of two N-D binary vectors, A and B, is defined as the matrix

$$[C] = A\ B^T = \begin{bmatrix} a_1 \\ a_2 \\ \cdot \\ \cdot \\ \cdot \\ a_N \end{bmatrix} [b_1\ b_2\ \cdots\ b_N] = \begin{bmatrix} c_{11} & c_{12} & \cdots & c_{1N} \\ c_{21} & c_{22} & \cdots & c_{2N} \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ \cdot & \cdot & \cdots & \cdot \\ c_{N1} & c_{N2} & \cdots & c_{NN} \end{bmatrix} \qquad (7.4.3)$$

where $c_{ij} = a_i\ b_j$. To perform this vector outer product multiplication, N^2 AND gates are needed. In Fig.7.4.2, a schematic network illustrating the multiplication of two 3×3 vectors is shown. To expand the input light dots into either horizontal or vertical light bars to cross and overlap at the SHG plate, two additional cylindrical lenses are employed. The SH signals emanating from the nine intersections are considered as the outer-product outputs.

7.4.3, Optical matrix-vector multiplication processor

The matrix-vector product of a N × N binary matrix [A] and a N-D column vector B is defined as

$$D = \begin{bmatrix} a_{11} & a_{12} & - & a_{1N} \\ a_{21} & a_{22} & - & a_{2N} \\ \cdot & \cdot & - & \cdot \\ \cdot & \cdot & - & \cdot \\ a_{N1} & a_{N2} & - & a_{NN} \end{bmatrix} \begin{bmatrix} b_1 \\ b_2 \\ \cdot \\ \cdot \\ b_N \end{bmatrix} = \begin{bmatrix} a_{11}b_1 + a_{12}b_2 + \cdots + a_{1N}\ b_N \\ a_{21}b_1 + a_{22}b_2 + \cdots + a_{2N}\ b_N \\ \cdots\cdots\cdots\cdots\cdots\cdots \\ a_{N1}b_1 + a_{N2}b_2 + \cdots + a_{NN}\ b_N \end{bmatrix} \qquad (7.4.4)$$

Note that a matrix-vector product can be decomposed into several parallel vector inner product operations. In Fig.7.4.3, by combining with an additional input cylindrical lens, three Fig.7.4.1 type networks, a SHG-based 3-D vector optical matrix-vector multiplier is shown.

7.4.4, Optical matrix-matrix multiplication processor

Compared to the previously described algebraic operations, an optical matrix-matrix multiplication is more complicated. As an example, consider the multiplication of two 2 × 2 binary matrices [A] and [B]

$$[E] = \begin{vmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{vmatrix} \begin{vmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{vmatrix} \tag{7.4.5}$$

$$= \begin{vmatrix} a_{11}b_{11} + a_{12}b_{21} & a_{11}b_{12} + a_{12}b_{22} \\ a_{21}b_{11} + a_{22}b_{21} & a_{21}b_{12} + a_{22}b_{22} \end{vmatrix} = \begin{vmatrix} e_{11} & e_{12} \\ e_{21} & e_{22} \end{vmatrix}$$

There are two methods to evaluate a this matrix-matrix product. Using a vector outer product decomposition, the matrices are first decomposed into vectors and then are sequentially entered into a physical vector outer product multiplier. With a properly decomposed synchronized temporal sequence, the previously described outer product processor (see Fig.7.4.2) can be used for the matrix-matrix product generation. Using a vector inner product decomposition in combination with an SHG AND gate-based network, provides a faster optical matrix-matrix multiplier. In Fig.7.4.4, a vector inner product-based SHG matrix-matrix multiplier is shown. Unlike the previous examples, here, both a 3-D network and unequal input channel spacings are used. In this network instead of entering the data sequentially as in the case of a vector outer product multiplier[23], a fully parallel input format is used. Because of the parallel format, it possesses an inherently faster multiplication speed. To collect the channelized multiplication results, at the output an additional cylindrical lens is used.

7.5, Summary

In this chapter, various new all-optical binary arithmetic processing methods have been described. Using two optical SIS cells, an optical full adder has been described. Based on the full adder, an optical SIS Brown multiplier was proposed. As alternative methods for performing optical binary multiplication, optical SHG-based DMAC processors to handle various binary scalar, vector as well as matrix multiplications have also been described. First, these proposed new devices use parallel inputs to generate mixed binary partial products. With fast T-M A/D converters and carry look-ahead adders, the multiplication final results can be obtained. The major advantages of SHG-based DMAC operation are: (1) it uses an instantaneous nonlinear optics effect so that ultrafast processing speed can be

achieved, (2) it adapts a symmetric input-output format for array interconnection, so that no additional delay elements are needed, (3) both input and output are optical quantities, and (4) a SHG AND element based lattice array can be integrated monolithically on a single SHG crystal.

7.6, References

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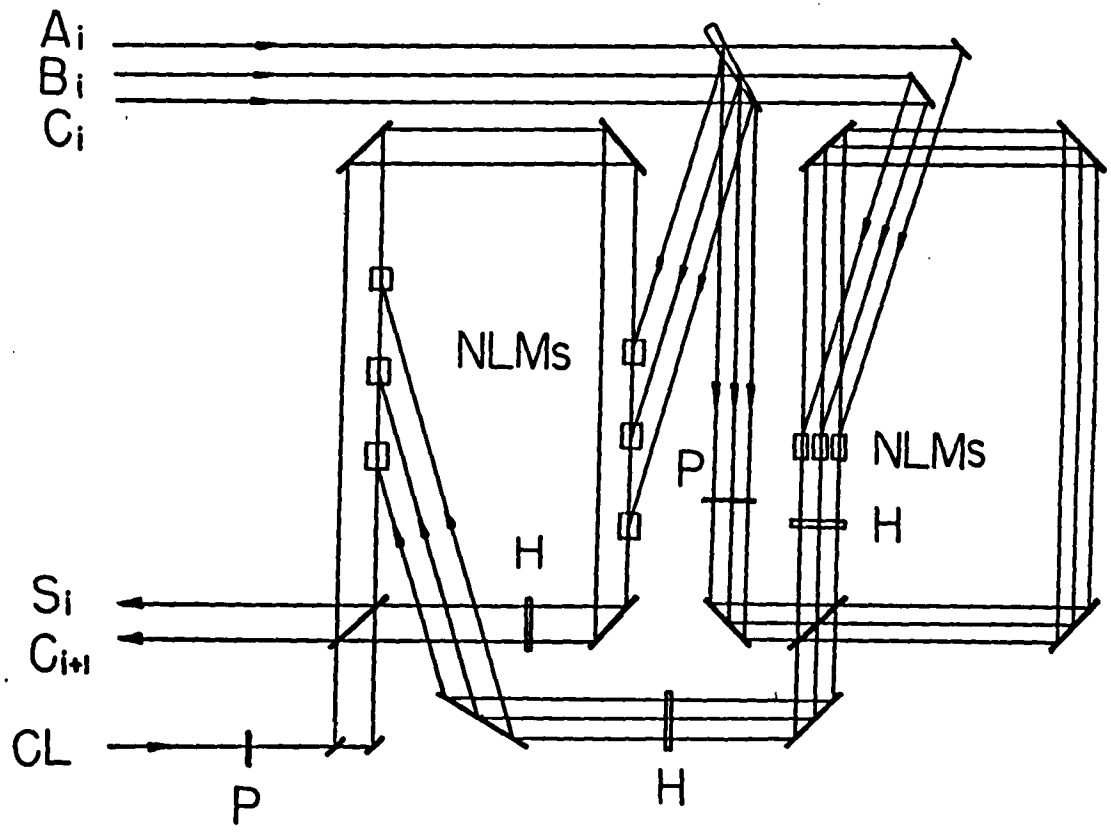

Fig.7.2.1 Optical SIS implementation of a binary full adder. A_i and B_i, two i^{th} input signals; C_i, i^{th} carry; S_i, i^{th} carry; S_i, i^{th} output of summation; CL, clock, and RP, retardation plate.

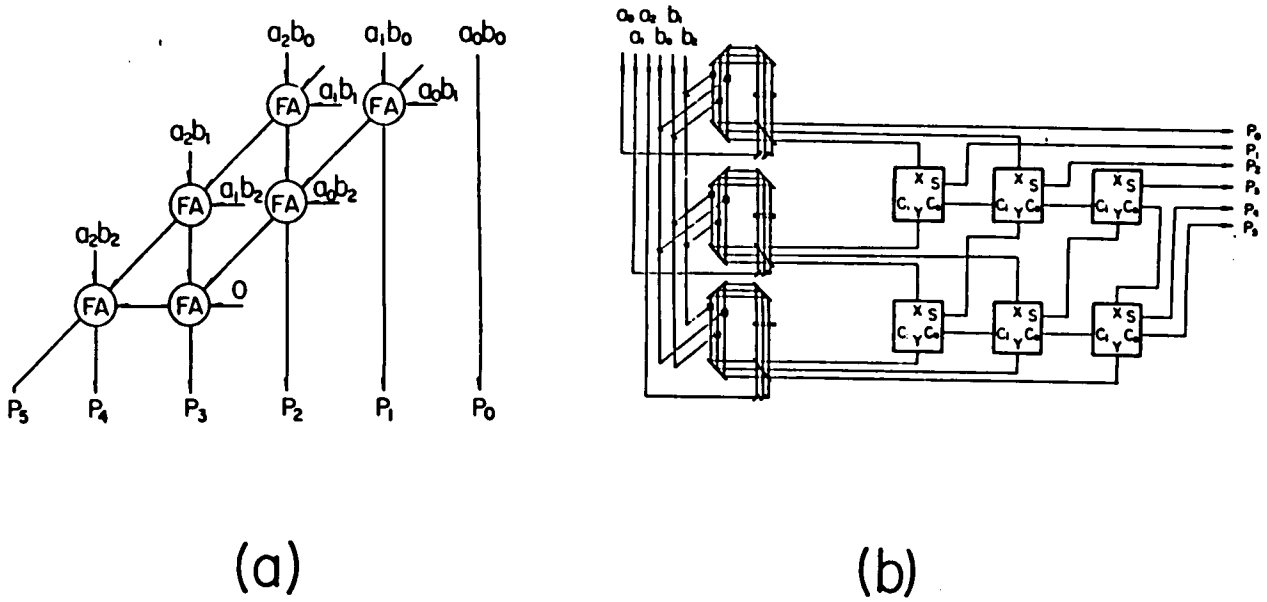

Fig.7.2.2 (a) Data flow diagram, and (b) the SIS implementation of a 3-bit optical binary array multiplier.

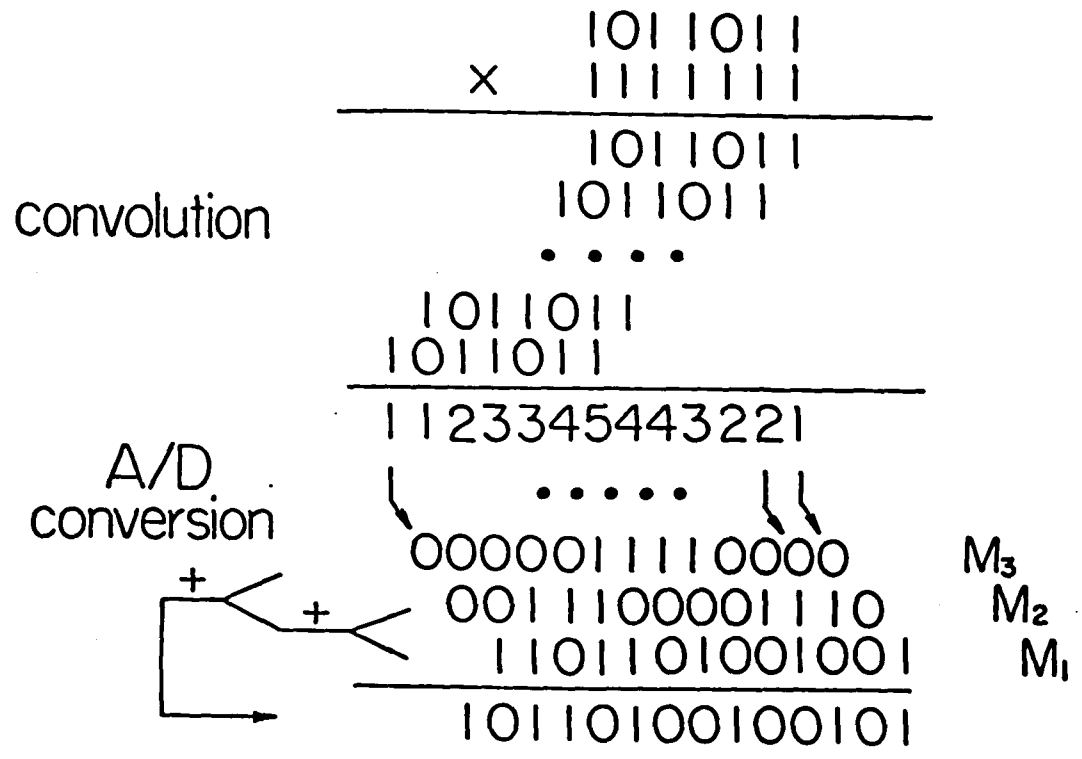

Fig.7.3.1 A DMAC multiplication example in which multiplication of two 7-bit numbers is illustrated. Instead of the usual six adders in three parallel stages; this scheme uses three adders in two parallel stages.

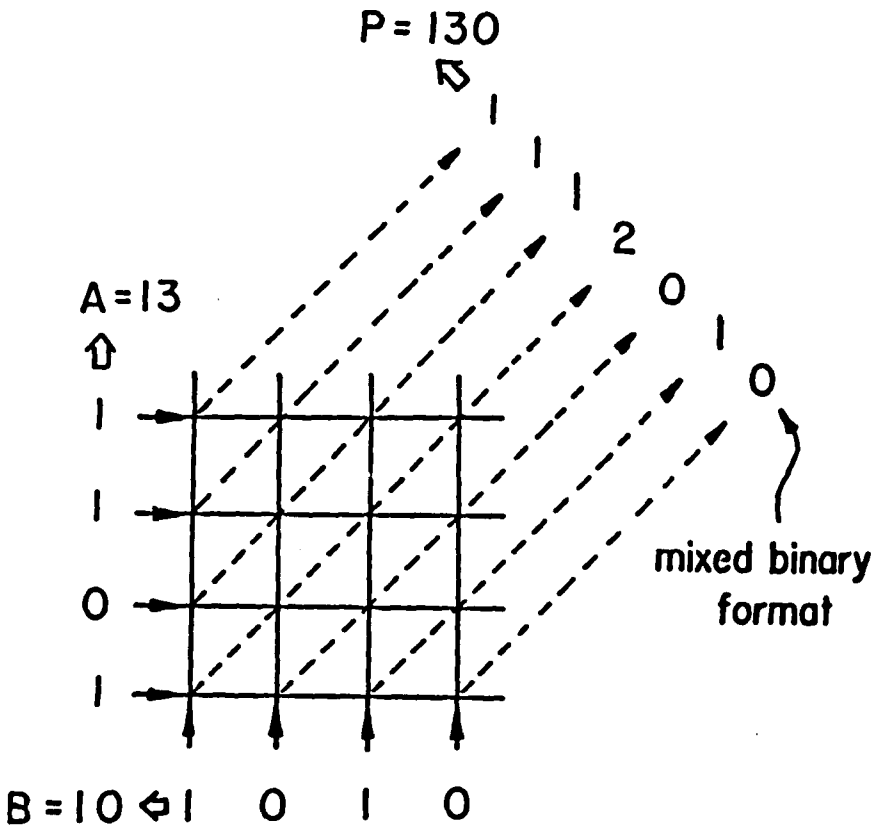

Fig.7.3.2 A SHG-based time-integraing multiplication preprocessing architecture. Parallel, spatially encoded inputs enter from the left and the bottom part of diagram. Outputs generated at each AND gate beam intersection are used to form the mixed-binary multiplication result.

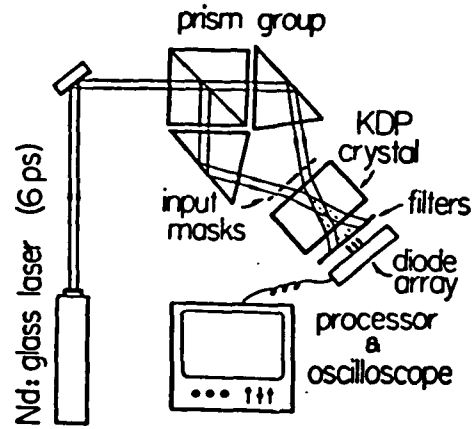

Fig.7.3.3 (a) A SHG-based digital optical multiplication experimental setup. M, mirror; BS, beamsplitter; P, composite prism; KDP, SHG crystal; I, input mask; N, ND filter; C, color filter; D, linear diode array; O, oscilloscope. (b) The oscilloscope trace of a three bit output corresponding to a two-bit binary unsigned multiplication.

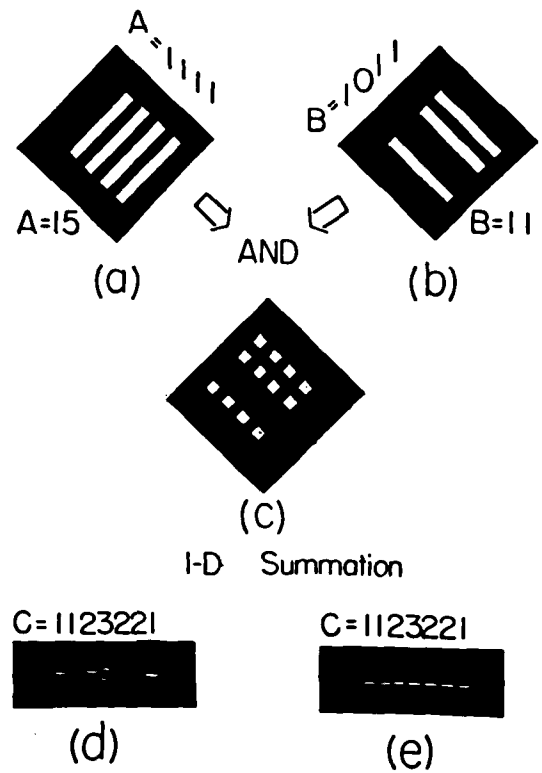

Fig.7.3.4 Results of a space-integrating optical binary multiplication preprocessor. (a) and (b) are two masks representing the two binary numbers (A=15 and B=11) to be multiplied. An opaque pixel, sandwiched between every two consecutive bits, is the guard pixel, (c) is the outer-product shadowgram formed by cross-overlapping the two masks, (d) is the result of 1-D channel-wise summation of light intensities in a plane slightly shifted from the lens focal plane, and (e) is the same result obtained right on the lens back focal plane. Both represent a mixed-binary multiplication result C=165.

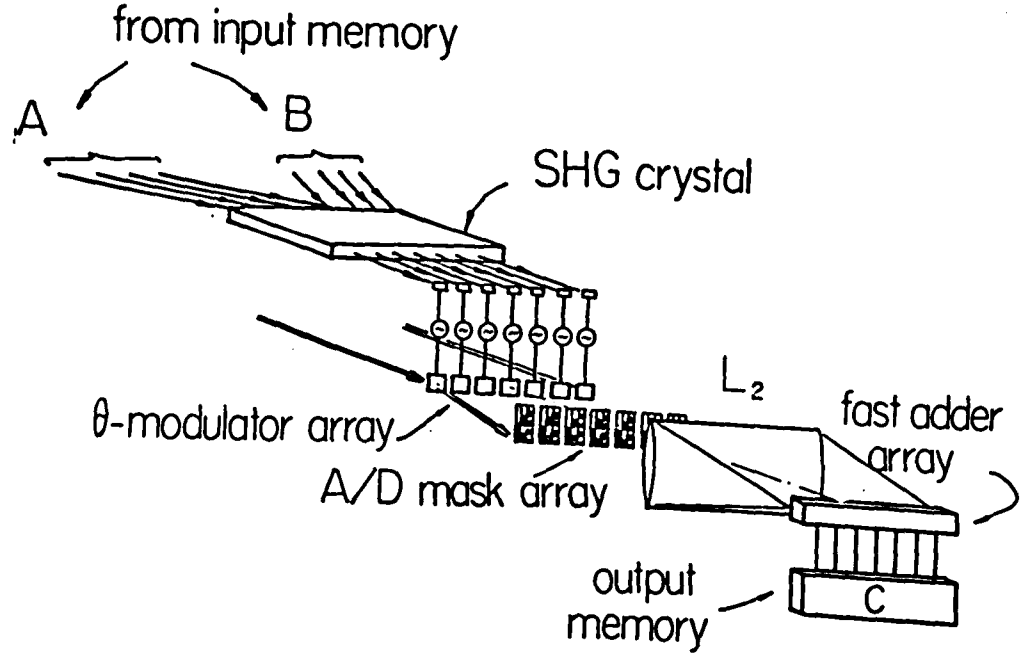

Fig.7.3.5 A proposed real-time time-integrating 4 bit optical digital multiplication system. To generate a mixed-binary convolution result, two spatially coded 4-bit parallel inputs are directed to a SHG crystal. Using a set of beam deflectors and fast time-integrating detectors, the detected voltages are mapped to various 1-D spatial locations. Using A/D conversion masks, their corresponding binary codes are obtained. To form the final multiplication result, the generated binary signals are directed into a fast carry look-ahead adder array.

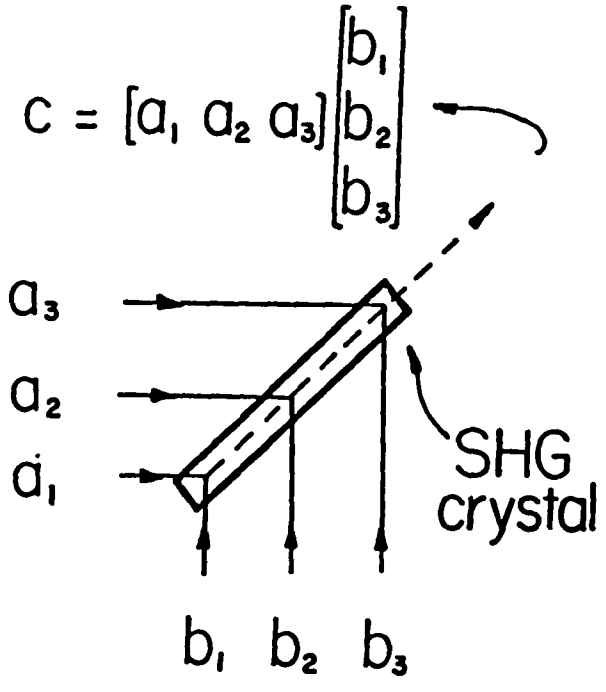

Fig. 7.41 A SHG-based optical 3-D vector inner product processor. Three AND gate outputs are aligned in a single output channel.

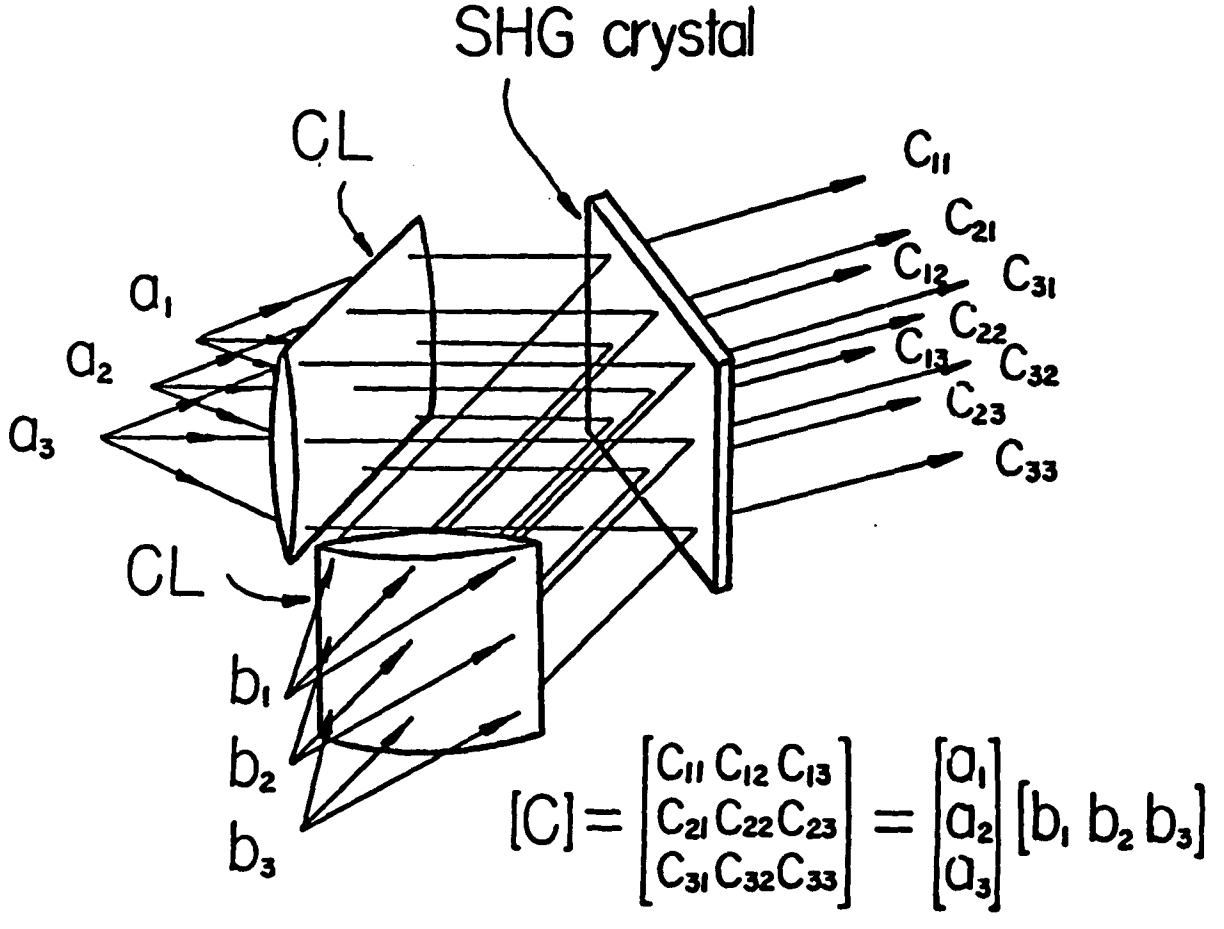

Fig.7.4.2 A SHG-based optical 3-D vector outer product processor. In addition to nine SHG AND gates, two input prisms are used for interconnections.

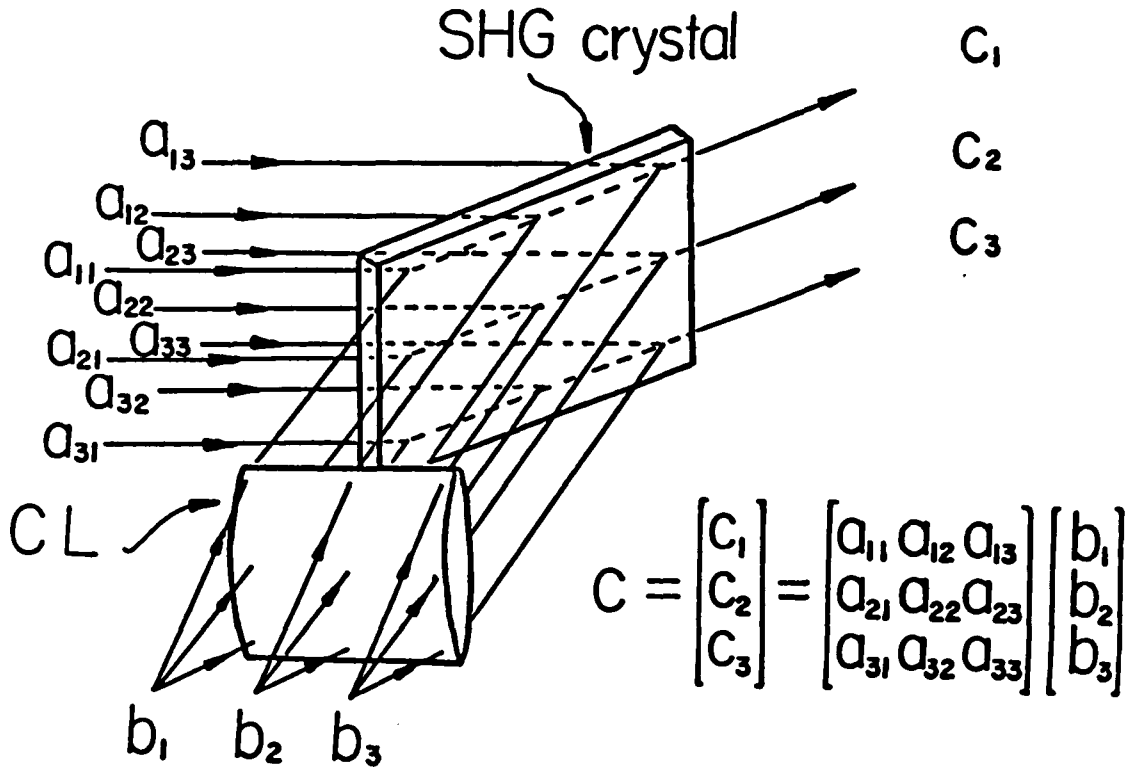

Fig.7.4.3 A SHG-based optical matrix-vector multiplier. Three 3-D parallel vector inner product processors together with a input prism are used.

$$[C] = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix}$$

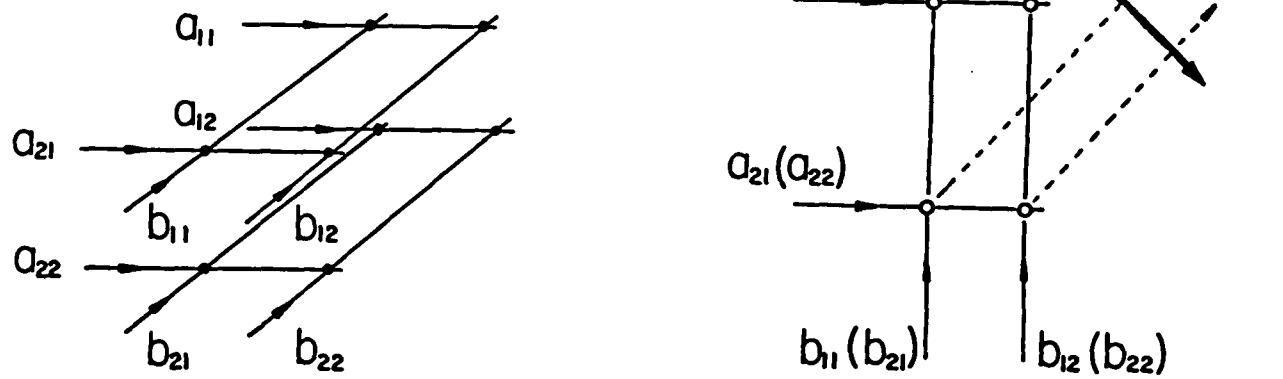

Fig.7.4.4 A SHG-based matrix-matrix multiplier. Parallel input spacings for [A] and [B] are different so that four output channels (after a lens space-integration) are obtained.

VIII. OPTICAL BINARY-CODED TERNARY ARITHMETIC PROCESSORS

8.1, Introduction

Recently, there has been a revival of interest in non-binary the so-called multiple-valued logic computing. The interest is due to the fact that the increase of logic density can provide additional processed information through each connection[1,2]. It has been indicated that an efficient way to implement multiple-valued logic is to use a mosaic of ultrafast, large aperture optical elements[3]. Since for some optical materials the switching time is on the order of picoseconds and most optical beams can intersect without interaction, very high-bandwidth parallel optical signal channels can be established. For these reasons, a combination of multiple-valued computing and ultrafast optical switching may lead to the realization of a future generation of ultrafast digital optical computer.

In this chapter, a number of ternary representation methods[4] are introduced. Ternary number system is optimum in terms of storage complexity[2]. Two ternary number representations, to be used for optical computing, the ordinary ternary (OT) and the binary balanced ternary (BT) representations, respectively, are discussed[5]. Since in practice an efficient and ultrafast tristable switch is difficult to realize, a practical method to synthesize the three logic states is to use binary encoding techniques. Here, each ternary symbol is encoded into a pair of binary symbols. The arithmetic or logic operations thus performed are based on binary elements. Using binary coded OT (BCOT), and binary coded BT (BCBT) representations various arithmetic and multiple-valued logic operations are discussed. A number of BCT arithmetic and logic implementation examples, based on the two-port Sag-

nac interferometric switches[6,7], are presented.

8.2, Ternary Numbers and Representations

8.2.1, Ternary number systems

In a radix N (N > 2) number system, N usually takes on the set of positive integer (0,1,...N-1) values. When N is odd, a symmetrical set of numbers ($-\frac{N-1}{2}$, ... -1, 0, 1 ... $\frac{N-1}{2}$) can also be used[2]. A radix three is called the ternary number system. In the ternary system, the positive integer set (0, 1, 2) is called the OT while the symmetrical number set (-1, 0, +1) is called BT set. Using either set, an unsigned ternary number A can be represented by an ordered string of symbols

$$A = (a_n\ a_{n-1} \cdots a_0 \cdots a_{1-m}\ a_{-m}) = \sum_{i=-m}^{n} a_i \times 3^i \qquad (8.2.1)$$

where a_i is either a OT or a BT symbol. Since BT is a signed digit form[8], it is suitable to represent a signed number. In this chapter, for both BCT representations, only integer numbers are considered.

8.2.2, Binary-coded ternary representations

To optically encode a non-binary number system, an optical multistable switch can be used. However, in practice, it is more difficult to implement a fast and efficient optical multistable switch than its binary counterpart. For this reason, there is a considerable interest in implementing non-binary numbers using binary elements. In one approach, in the so-called pulse-position coding technique[9], the N signal channels represent N logic or number levels. The presence or absence of a binary signal in a specific channel implies a particular logic or number value. Using a two-dimensional binary switch array, pulse-position coding has been used to perform residue arithmetic[10]. For either OT or BT number representations, this three-channel coding method can be used. In this chapter, a new

binary coded ternary (BCT) pulse-position coding approach is introduced. In this approach, the three logic or number values are encoded into a pair of binary digits. In turn, a ternary number is decomposed into two binary strings. The advantage of this approach is, that by combining BCT with pulse-position coding, each ternary symbol requires only two signal channels. Also, with this approach, various binary optical arithmetic and logic devices can directly be used to synthesize ternary logic and arithmetic operations.

The binary coded OT (BCOT) set is chosen as

$$\begin{aligned} 0_{OT} &= [\,0,0\,]_{BCOT} \\ 1_{OT} &= [\,1,0\,]_{BCOT} = [\,0,1\,]_{BCOT} \\ 2_{OT} &= [\,1,1\,]_{BCOT} \end{aligned} \tag{8.2.2}$$

Here, the ternary OT digit is the sum of two binary digits present in the two channels. A clever way to choose the binary coded BT (BCBT), since it is a signed number representation, is to assign the positive (negative) number parts to different signal channels, i.e.

$$\begin{aligned} -1_{BT} &= [\,0,1\,]_{BCBT} = \bar{1}_{BT} \\ 0_{BT} &= [\,0,0\,]_{BCBT} = [\,1,1\,]_{BCBT} \\ +1_{BT} &= [\,1,0\,]_{BCBT} \end{aligned} \tag{8.2.3}$$

Using the BCBT form, a negative number can be obtained from its positive expression by interchanging the channel positions of the two binary symbols. To represent a negative OT number, similar to the binary 2's complement representation, a 3's complement method can be used[5].

As an example, the decimal number 47_{10} is represented in OT, BCOT, BT and BCBT forms as

$$47_{10} = (\,1202\,)_{OT} = [\,1101,0101\,]_{BCOT} \tag{8.2.4a}$$

$$47_{10} = (\,1\bar{1}\bar{1}1\bar{1}\,)_{BT} = [\,10010,01101\,]_{BCBT} \tag{8.2.4b}$$

8.3, Arithmetic Computing Using BCT Representations

8.3.1, Auxiliary BCT logic functions

Before presenting a detailed description of the BCT arithmetic operations, three auxiliary BCT logic functions are discussed. The logic functions are the mutually exclusive equivalent pair (MEEP), the minor pair (MP) and the negation pair (NP) operations. To insure a unique BCBT output after some arithmetic operations (see Eq.(8.2.3)), the MEEP function is employed to convert the resultant [1,1] to its equivalent [0,0] form while leaving other pairs [1,0] and [0,1] alone. On the other hand, to insure a unique arithmetic result in the BCOT representation, the MP function is used to convert a [0,1] to a [1,0] pair while leaving other pairs [0,0] and [1,1] alone. Both the MEEP and the MP functions satisfy the addition relation

$$f_1 \text{ "+" } f_2 = x_1 \text{ "+" } x_2 \tag{8.3.1}$$

where"+"denotes the arithmetic sum, and x_i (f_i) are the MEEP or MP inputs (outputs), respectively. The final auxiliary BCT logic function, the NP takes a positive number string pair and converts it to its corresponding negative number string pair. The NP function realization is different for the two different, the BCBT and the BCOT, representations. The results for the Boolean logic design for the BCT MEEP and MP as well as for the BCBT NP are summarized in Table 8.3.1.

Using these three auxiliary BCT logic operators and a binary full adder, BCT arithmetic operation can be performed. Using BCT addition, other arithmetic operations, such as subtraction and multiplication, can also be implemented. For example, using the addition algorithm, with an additional NP operation, the subtraction of two BCT numbers can be performed. Using an NP operator, first, the subtrahend is negated. A BCT adder is then used to add the negated subtrahend to the minuend. Using a number of BCT addition and shift operations, BCT multiplication of two numbers can also be performed. For the two BCT inputs (number strings) represented as

$$(x_1)_T = [x_{11}, x_{12}]_{BCT}, \qquad (x_2)_T = [x_{21}, x_{22}]_{BCT}, \quad (8.3.2)$$

the BCT arithmetic or logic function f ( ) can be obtained as

$$f = [f_1, f_2]_{BCT} \quad (8.3.3)$$

where

$$f_1 = g(x_{11}, x_{12}, x_{21}, x_{22}), \qquad f_2 = h(x_{11}, x_{12}, x_{21}, x_{22})$$

and g ( ) and h ( ) are either binary arithmetic or logic functions. Since the simultaneous use of four input strings can lead to a complicated operation, the use of two BCT partial additions is preferred [5]. For a BCT partial addition, the fact that

$$(x_1)_T \text{ "+" } (x_2)_T = [x_{11}, x_{12}]_{BCT} \text{ "+" } [x_{21}, 0]_{BCT} \text{ "+" } [0, x_{22}]_{BCT} \quad (8.3.4)$$

is used. Thus, for the full addition of two BCT number strings, two BCT partial addition operations are performed. Since each BCT partial addition involves only three number strings, it is simpler to process.

8.3.2, BCOT addition algorithm

To add two BCOT numbers, first, using the MP operation, the given string pair x_{11}, x_{21} is replaced by the string pairs y_{11}, z_{21}. Then, another MP replacement is performed to convert x_{12}, z_{21} to y_{12}, y_{21}. This operation[5] replaces all unwanted [0,1] with the desired [1,0] pairs. Next, the first BCOT partial addition is performed

$$A = [A_1, A_2]_{BCOT} = [y_{11}, y_{12}]_{BCOT} \text{ "+" } [y_{21}, 0]_{BCOT} \quad (8.3.5)$$

where A_1 and A_2 are mixed (arithmetic and logic) binary functions. To save space, A_1 and A_2 definitions[10] are given in Table 8.3.1. To unify the partial result, another MP operation is used.

Using the partial result $[A_1, A_2]$ and the remaining $[0, x_{22}]$ string, by repeating the previous partial addition steps, the full BCOT addition is obtained.

$$\begin{aligned} S &= x_1 \text{ "+" } x_2 \\ &= [\, A_1, A_2 \,]_{BCOT} \text{ "+" } [\, 0, x_{22} \,]_{BCOT} \\ &= [\, A_1, A_2 \,]_{BCOT} \text{ "+" } [\, x_{22}, 0 \,]_{BCOT} \end{aligned} \tag{8.3.6}$$

Notice that in the last line in Eq.(8.3.6), an interchange between the strings in the two signal channels is indicated. This operation is guaranteed by the OT representation.

As a numerical example, consider the BCOT addition of the two decimal numbers $x_1 = 59_{10}$ and $x_2 = 19_{10}$. In this case, the BCOT numbers are $x_1 = [1011, 1001]$ and $x_2 = [0101, 0100]$. The first BCOT partial addition is

$$[\, A_1, A_2 \,]_{BCOT} = [\, 1011, 1001 \,]_{BCOT} \text{ "+" } [\, 0101, 0000 \,]_{BCOT} \tag{8.3.7a}$$

This expression, after the two consecutive MP replacements, becomes

$$[\, A_1, A_2 \,]_{BCOT} = [\, 1111, 1001 \,]_{BCOT} \text{ "+" } [\, 0001, 0000 \,]_{BCOT} \tag{8.3.7b}$$

After some binary arithmetic and logic operations, the values A_1 and A_2 are evaluated as

$$[\, A_1, A_2 \,]_{BCOT} = [\, 1110, 1010 \,]_{BCOT} \tag{8.3.7c}$$

Since this is a MP, the result $[A_1, A_2]$ remains the same after the next MP operation. In the second part of the full addition, the partial addition

$$S = [\, S_1, S_2 \,]_{BCOT} = [\, 1110, 1010 \,]_{BCOT} \text{ "+" } [\, 0100, 0000 \,]_{BCOT} \tag{8.3.7d}$$

is performed. The MP replacements give

$$S = [\, S_1, S_2 \,]_{BCOT} = [\, 1110, 1110 \,]_{BCOT} \text{ "+" } [\, 0000, 0000 \,]_{BCOT} \tag{8.3.7e}$$

The use of the Table 8.3.1 BCOT A_1, A_2 and MP operations reduces this to

$$S = [\, 1110, 1110 \,]_{BCOT} = (\, 2220 \,)_{OT} = 78_{10} \tag{8.3.7f}$$

8.3.3, BCBT addition algorithm

The BCBT full addition algorithm, for two BCBT number strings $[x_{11}, x_{12}]$ and $[x_{21}, x_{22}]$ is given as follows. First, the number strings x_{11}, x_{21} are replaced, using a MP logic operator, with the strings y_{11}, y_{21}. Next, the first BCBT partial addition is performed as

$$A = [A_1, A_2]_{BCBT} = [y_{11}, x_{12}]_{BCBT} \text{ "+" } [y_{21}, 0]_{BCBT} \quad (8.3.8)$$

where the A_1, A_2 expressions can be found in Table 8.3.1. To remove the ambiguity due to possible [1,1] pairs, a MEEP function is used. Unlike the BCOT full addition, the BCBT full addition can not be obtained by two straightforward BCBT partial additions. This is so because

$$[0, x_{22}]_{BCBT} = NP([x_{22}, 0]_{BCBT}) = [x_{22}, 0]_{BCBT} \quad (8.3.9)$$

Thus, to obtain the final sum, an additional NP operation is required. The BCBT full addition of the two BCBT numbers

$$\begin{aligned} S &= [S_1, S_2]_{BCBT} = [A_1, A_2]_{BCBT} \text{ "+" } [0, x_{22}]_{BCBT} \quad (8.3.10) \\ &= NP([A_2, A_1]_{BCBT} \text{ "+" } [x_{22}, 0]_{BCBT}) \end{aligned}$$

Here, as a BCBT full addition example, the previous numerical example of the sum of the decimal numbers 59_{10}"+"19_{10} is given. The corresponding number strings now are x_1 = [10100, 01011] and x_2 = [01001, 00100]. In the first step, the MP replacement leads to

$$[A_1, A_2]_{BCBT} = [11101, 01011]_{BCBT} \text{ "+" } [00000, 00000]_{BCBT} \quad (8.3.11a)$$

After the BCBT A_1, A_2 binary arithmetic and logic operations, the result becomes

$$[A_1, A_2]_{BCBT} = [11101, 01011]_{BCBT} \quad (8.3.11b)$$

To unify the result, the use of the MEEP operator generates

$$[A_1, A_2]_{BCBT} = [10100, 00010] \tag{8.3.11c}$$

In the second part of the operation, the partial addition

$$[B_1, B_2]_{BCBT} = [00010, 10100]_{BCBT} \text{ "+" } [00100, 00000]_{BCBT} \tag{8.3.11d}$$

is performed. Repeating the described steps, yields

$$[B_1, B_2]_{BCBT} = [00110, 10100]_{BCBT} \tag{8.3.11e}$$

This expression reduces, after a MEEP operation, to

$$[B_1, B_2]_{BCBT} = [00010, 10000]_{BCBT} \tag{8.3.11f}$$

Finally, an NP function is used to obtain the final full addition result

$$\begin{aligned}[S_1, S_2]_{BCBT} &= NP([B_1, B_2]_{BCBT}) \\ &= [10000, 00010]_{BCBT} = (100\bar{1}0)_{BT} = 78_{10}\end{aligned} \tag{8.3.11g}$$

8.4, TPSIS-based BCT Optical Arithmetic

In this section, using the BCT representations and with the previously described TPSIS as the binary optical elements, optical implementations of various BCT arithmetic and logic operations are discussed. Other approaches, however, with different optical switch elements, such as the bistable devices[11], the liquid-crystal light valve spatial light modulators[12], etc. are also possible.

8.4.1, TPSIS implementation of BCT auxiliary logic functions

First, optical implementations of ternary arithmetic operations are discussed. For the BCT addition, three BCT auxiliary logic elements (MEEP, MP and NP) as well as a binary full adder are required. To generate the MEEP function, two parallel binary AND functions are used. These two AND functions can easily be obtained using two TPSISs. In

Fig.8.4.1(a), the TPSIS MEEP implementation is depicted, where the left (right) TPSIS generates the BCT f_1 (f_2) output. Similarly, in Fig.8.4.1(b), using a TPSISs as an AND element and a BS as an OR element, an optical BCT MP is implemented. The NP operator is different in the two, the BCOT and the BCBT, representations. Because there exist a number of ways to represent negative numbers in BCOT, the discussion of an optical BCOT NP is omitted. The BCBT NP, on the other hand, is uniquely defined. For the BCBT NP generation, the interchange of the input signal channels will lead to the desired output. This can be accomplished with passive optical elements, such as prisms, mirrors, gratings, waveguides, etc.

8.4.2, TPSIS-based BCT adder circuits

To perform BCT arithmetic addition, two BCT partial adders are needed. The key element in a BCT partial adder is a binary full adder which we have described in chapter 7.

To explain the BCT optical full adder implementation, first, consider a BCT partial adder design. Since the optical implementations of the three auxiliary BCT logic operators as well as a binary full adder have already been described, only the block diagram of these elements are indicated. In Fig.8.4.2(a) the BCOT partial adder signal flow diagram is shown. It contains three parts with each corresponding to an algorithm step. The input signals arrive at the top black box that performs the two MP logic functions. The outputs are then injected to the middle box where the partial adder A_1, A_2 functions (see Table 8.3.1) are performed. In Fig.8.4.2(b), this part of the diagram is drawn separately, where in addition to a binary full adder, three TPSIS AND gates are used. To unify the results, the bottom box of Fig.8.4.2(a) is used to perform the final partial addition operation. Based on two such BCOT partial adders, a BCOT full adder can be obtained. In Fig.8.4.3, using an array of N+1 full adders, an N-digit TPSIS BCOT adder is shown. Similarly, in Fig.8.4.4(a), a BCBT partial adder is depicted. Again, three different sections are shown. For clarity, in Fig.8.4.4(b), the middle part, that corresponds to the BCBT partial adder A_1, A_2 operations (see Table 8.3.1), is drawn separately. For the full BCBT addition, two BCBT partial

adders and an additional BCBT NP operator are used. In Fig.8.4.6, the N-digit BCBT arithmetic adder connection diagram is shown. Using these adders, BCT subtractions can also be performed. However, for the preparation of inputs for the two number subtraction, an additional NP logic element is needed.

8.5, Summary

In this chapter, TPSIS based ternary optical computing has been discussed. Two, OT and BT, ternary number representations are used. While the OT is suitable for unsigned, the BT, is suitable for both signed and unsigned number representation. To represent a ternary number, binary encoding techniques were discussed where each ternary digit is represented by a binary signal channel pair. Compared to other multiple-valued optical encoding methods, one advantage of the optical BCT is that it conserves the system's space-bandwidth product. Another advantage is that the ternary optical computing elements can be directly synthesized using binary optical switches. As examples of BCT arithmetic computing, both BCT type addition algorithms were given. Based on the algorithm other BCT arithmetic operations such as subtraction and multiplication can also be performed.

8.6, References

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MEEP	$f_1 = X_1 \cdot \overline{X_2}$	$f_2 = \overline{X_1} \cdot X_2$	BCT
MP	$f_1 = X_1 + X_2$	$f_2 = X_1 \cdot X_2$	BCT
NP	$f_1 = X_2$	$f_2 = X_1$	BCBT
$[A_1, A_2]$	$f_1 = \overline{((\overline{X_{21} \text{ "+" } X_{12}}) \cdot X_{12})} \cdot X_{11}$		
	$f_2 = (X_{12} \text{ "+" } X_{21}) \cdot \overline{X_{21}}$		BCOT
	$f_1 = (X_{11} \text{ "+" } X_{21}) \cdot \overline{X_{21}}$		
	$f_2 = \overline{(X_{11} \text{ "+" } X_{21})} \cdot X_{11} + X_{12}$		BCBT

Table 8.4.1 Auxilary functions needed for BCT arithmetic operations. $[A_1, A_2]$ functions are in a mixed format where binary full-additions followed by several logic operations need to be performed.

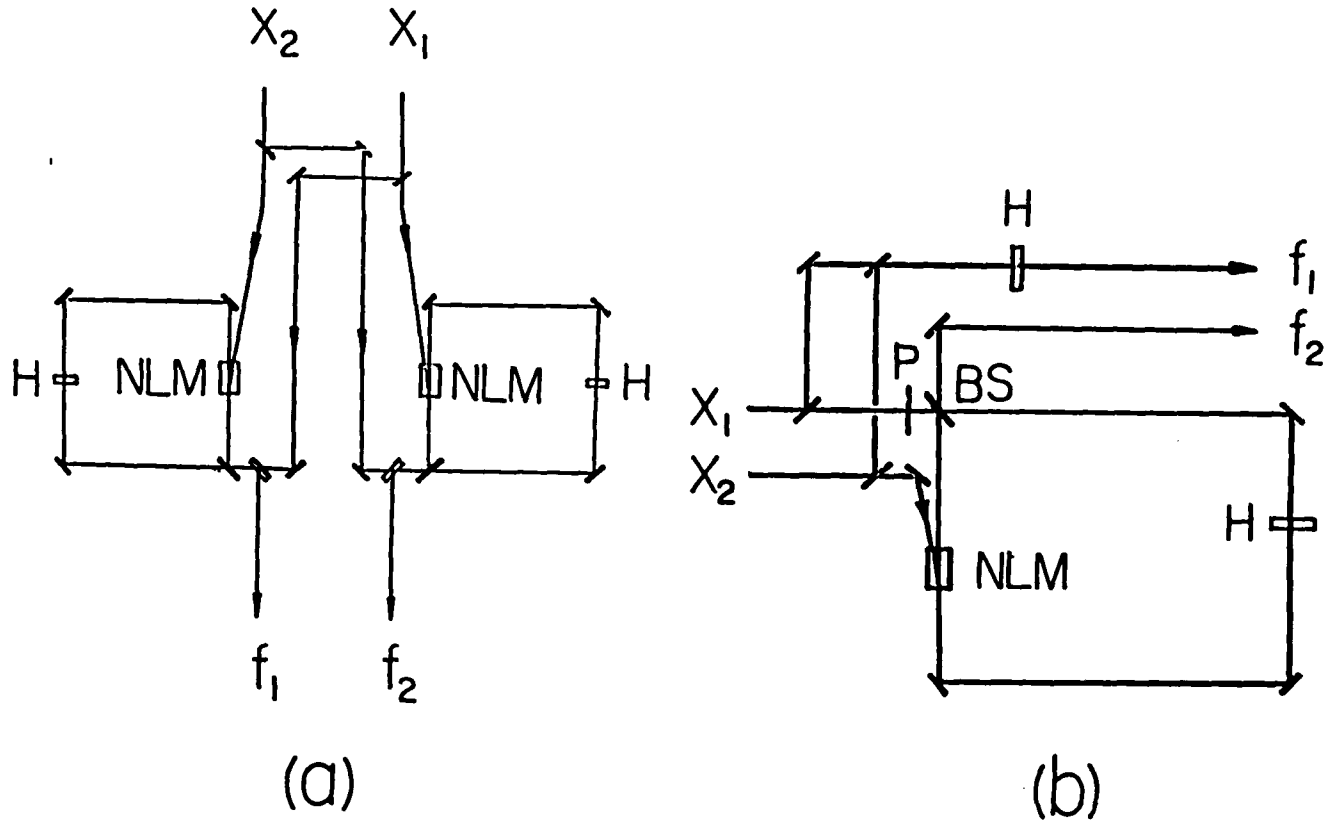

Fig.8.4.1 (a): TPSIS MEEP and (b): TPSIS MP function generations, P, linear polarizer; x_1, x_2 and f_1, f_2 are the two input and output BCT channels.

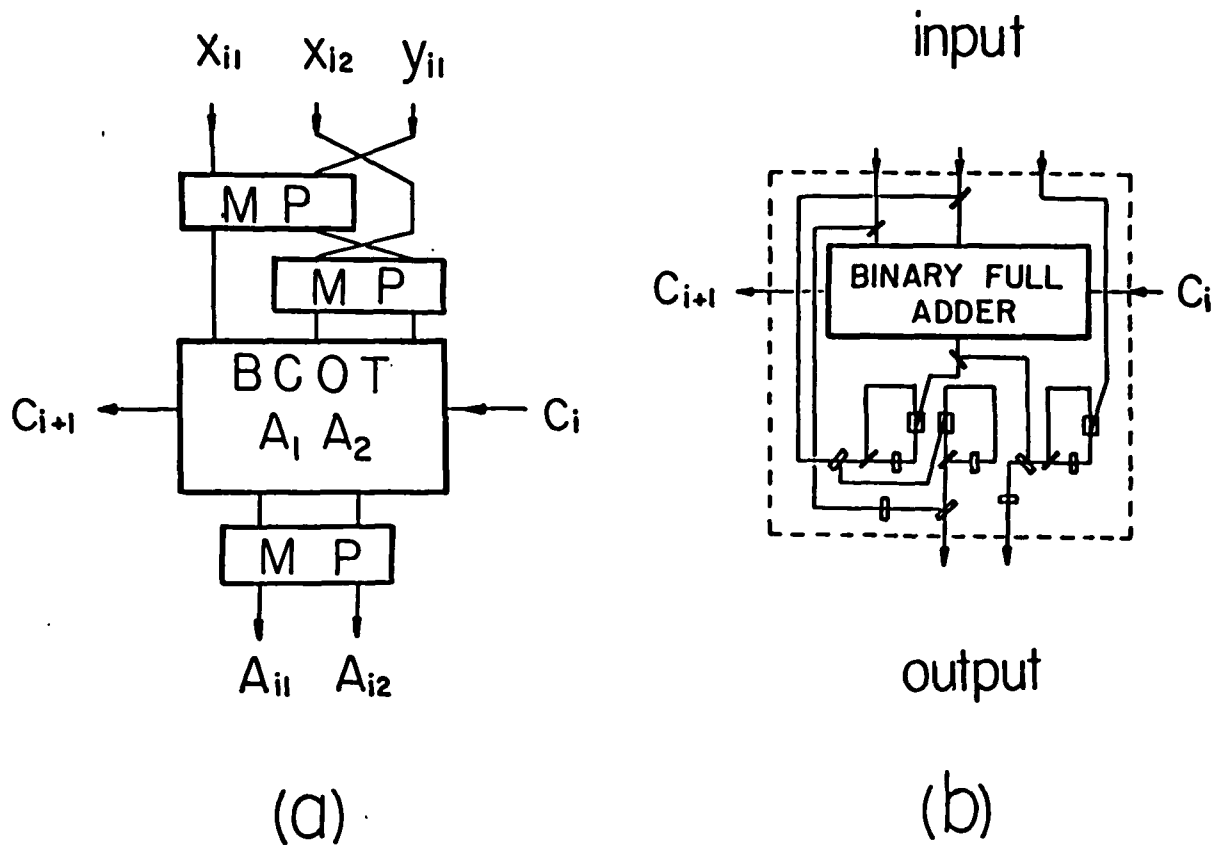

Fig.8.4.2 (a): BCOT partial addition signal flow diagram for adding i^{th} digits of $[x_1, x_2]_{BCOT}$ and $[y_1, 0]_{BCOT}$, all mirror schetches are omitted, (b): BCOT A_1, A_2 function generation, a binay full adder, three AND and one OR gates are used.

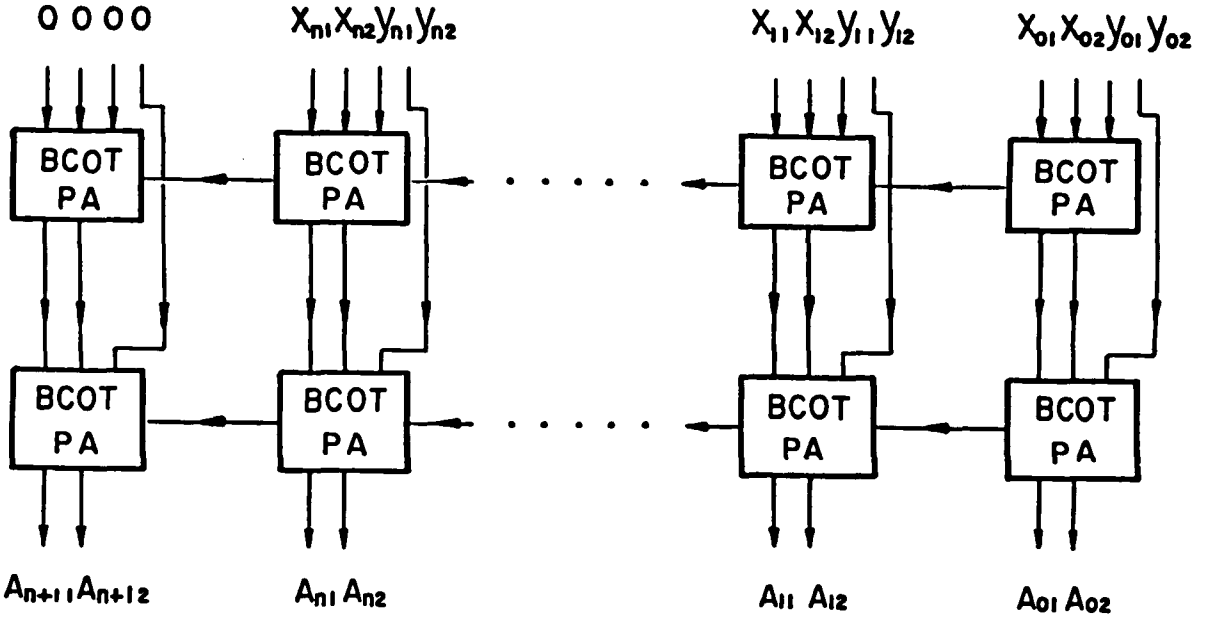

Fig.8.4.3 An N-digit BCOT adder for two N-digit input numbers $x = [x_1, x_2]_{BCOT}$ and $y = [y_1, y_2]_{BCOT}$.

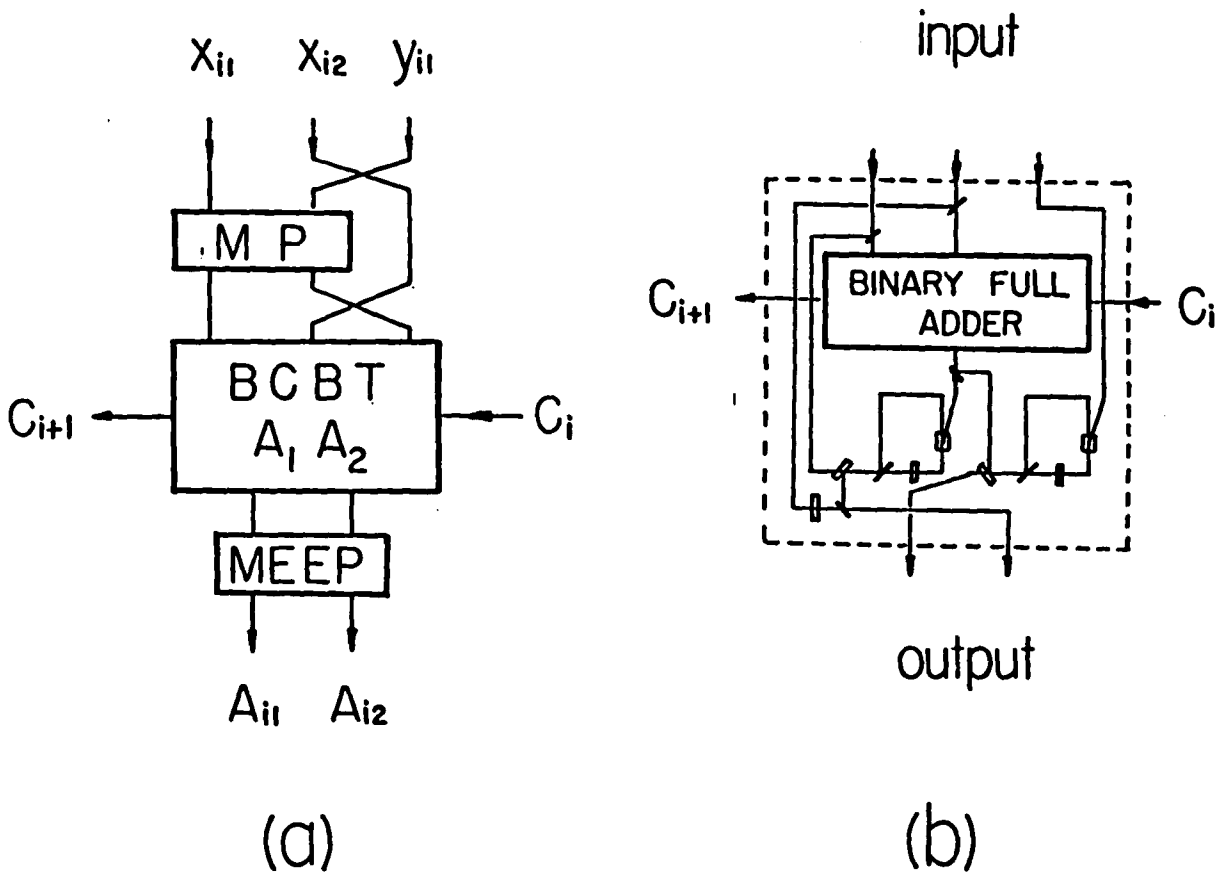

Fig.8.4.4 (a): BCBT partial addition signal flow diagram for adding i^{th} digit of $[x_1, x_2]_{BCBT}$ and $[y_1, 0]_{BCBT}$, (b): BCBT A_1, A_2 function generation, a binary full adder, two AND and one OR gates are used.

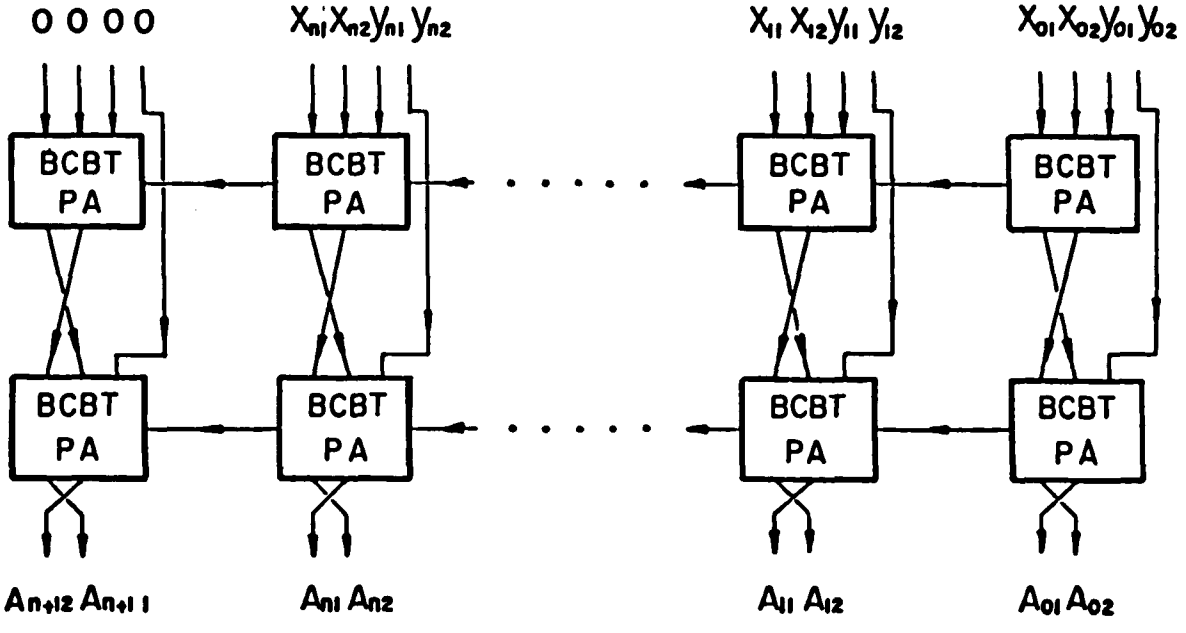

Fig.8.4.5 An N-digit BCBT adder for two N-digit input numbers $x = [x_1, x_2]_{BCBT}$ and $y = [y_1, y_2]_{BCBT}$.

IX. ADDITIOANL OPTOCAL NON-BINARY ARITHMETIC COMPUTING TECHNIQUES

9.1, Introduction

In the last chapter, an optical method to perform non-binary optical arithmetic computing was introduced. Although the case of ternary was discussed, the binary encoding method, however, can be used for other non-binary computing purposes. As stated earlier, the use of non-binary number system can increase the computation speed by either transmitting and processing data more efficiently or taking advantages of its parallel processing capability. In this chapter, additional new methods to perform optical non-binary computing are proposed. In the first proposed scheme, using a residue number system[1,2] optical carry-free arithmetic is performed. The residue method decomposes an arithmetic operation into a number of independent suboperations to be performed by different prime modulo-based logic elements. Using an ultrafast SHG network, parallel monolithic SHG-based optical residue processors[3] will be described. Following the description about optical residue processing, another non-binary, the so-called modified sign-digit (MSD)[4,5], number system for parallel arithmetic processing will be introduced. For the optical implementation, the content-addressable memory (CAM)[6,7] method and its holographic processing techniques are presented.

9.2, Parallel Optical Residue Arithmetic

9.2.1, residue number system

The residue number system is based on a K-tuple of integers $(m_1, m_2, \ldots m_K)$. Each of these integers is a modulus. These integers should have no common factors. To represent a number X, a set of K integers (also called residues) r_i, $i = 1, 2, \ldots K$ that satisfy the relation[1,2]

$$r_i = [X]_{m_i} = X \bmod m_i, \qquad i = 1, 2, \cdots K \tag{9.2.1}$$

where r_i denotes the least positive integer remainder of the division of X by m_i, will be used. The expressable range of X is

$$0 \leqslant X \leqslant \left(\prod_{i=1}^{K} m_i \right) - 1 \tag{9.2.2}$$

The major attraction of residue number system is its carry-free arithmetic operation capability. Specifically, the basic operations, such as addition, subtraction and multiplication of two numbers A and B using residue methods are performed according to

$$[A \mid B]_{m_i} = [[A]_{m_i} \mid [B]_{m_i}]_{m_i} \tag{9.2.3}$$

where $\mid$ denotes the above mentioned operations. Thus, an operation is divided into K sub-operations and performed separately in parallel. To form an optical residue processor, a group of prime integer modulo processing units needs to be employed. In each of these units, residue mapping based on a specific modulo is performed. By suitably combining the partial results generated from each processing unit, the final result is formed. As examples, in Table 9.2.1, using three prime integers 4, 7, and 9, addition, subtraction and multiplication of A = 16 and B = 12 are presented.

9.2.2, SHG-based ultrafast residue mapping units

Thus, a specific modulo processing unit is the key element to implement a residue-based numerical processor. Using electro-optic waveguide switches, different modulo residue mapping units have been proposed[2,7-9]. These proposed systems, however, has a common drawback that the speeds of supporting switches are very limited. Next, we propose a number of SHG-based ultrafast all-optical residue mapping units. These proposed structures can monolithically be integrated on a single SHG plate and therefore is suitable for circuit implementation.

In a mod N residue number system, addition is a circulant operation with the number of integral shifts determined by the value of addend. Similarly, subtraction is also a circulant operation where the subtrahend is added but in an opposite direction. To illustrate this principle, consider a mod 5 addition/subtraction truth table (see Fig.9.2.1(a)). To implement this table, a 2-D optical mapping network must be constructed. In Fig.9.2.1(b), using a SHG crystal, such a OIAP network is shown. For both the summand (minuend) and the addend (subtrahend), pulse-position coded inputs are used. The mapping operation is controlled by the summand (minuend) signals. The thus generated signals share five output channels. The crystal is cut and oriented so that desired total internal reflections can be achieved. Here, at any given time only one of the five addend (subtrahend) channels contains a signal. In other words, for a pair of input pulses, a SH output can only be generated at a single intersection. Again, using an oblique input isochronous wavefront, the inputs are auto-synchronized and thus no additional delay elements or clocks are needed.

In addition to residue addition/subtraction, using an OIAP, mod N residue multiplication can also be performed. A mod 5 multiplication truth table, for example, is shown in Fig.9.2.2(a). Since the multiplication by a zero results in a zero, only operations that map the other numbers, i.e. 1, 2, 3, and 4, are necessary. For this reason, to implement a mod 5 multiplication truth table, the use of a mod 4 adder has been suggested[7]. In general, multiplication in mod p, where p is prime, can be decomposed into addition in mod $p-1$ with

suitable pre- and post-permutation networks. In Fig.9.2.2(b), using a SHG based OLAP network, an SHG-based residue mod 5 multiplication unit is shown. In addition to three input (output) permutation elements, two separate SHG units, one for implementing mod 4 add and another for dealing with zeros, are employed. Although a multiplier uses more elements than a corresponding add unit, compared to other methods, this is a faster and more compact unit.

9.2.3, SHG-based residue matrix multiplication scheme

In many real-time scientific and engineering problems, it is necessary to solve a large number of algebraic and differential equations. For the solution of these equations, large amount of matrix manipulations are needed. With a digital optical computer, it is essential to be able to perform fast matrix multiplication. In previous sections, using the DMAC algorithm, an AND element-based binary matrix multiplication preprocessor was described. In this section, using residue arithmetic, an alternative integer matrix-matrix multiplication approach is proposed. Using a residue number system, integer matrix multiplication can be decomposed into a set of parallel, relative prime modulo-based residue matrix multiplications. Thus, solving a set of linear equations using residue matrix algebra can increase the computational speed. Details on the solution of integer-valued linear equations using residue matrix algebra are available[10,11].

The multiplication of two identical prime modulo-based matrices is similar to decimal case. In the residue case, both multiplication and addition are evaluated in the specific modulo residue system. A conventional matrix-matrix multiplier that performs the multiplication of two NXN matrices ($[C] = [A][B]$) contains a 2-D square array of N^2 identical processing elements each performing an arithmetic/logic operation that adds to its past contents the multiplication results of two present inputs. For the multiplication of two mod p NXN matrices, each of the N^2 cells, for example C_{ij} where $i, j \in (1,2,...N)$, executes recursively, for $k = 1,2,...N$,

$$[C_{i,j}^{(k)}] = [C_{i,j}^{(k-1)} + a_{ik} \bullet b_{kj}] \quad mod \ p \tag{9.2.4}$$

where a_{ik} (b_{kj}) are the ik^{th} (kj^{th}) element of the matrix $[A]$ ($[B]$). As an example, consider the multiplication of two 4×4 mod 5 matrices $[A]$ and $[B]$ where

$$[A] = \begin{bmatrix} 1 & 2 & 0 & 3 \\ 4 & 1 & 0 & 2 \\ 3 & 0 & 2 & 4 \\ 2 & 2 & 1 & 0 \end{bmatrix} \quad \text{and} \quad [B] = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 2 & 4 & 0 & 2 \\ 3 & 0 & 1 & 3 \\ 2 & 3 & 4 & 1 \end{bmatrix} \quad mod \ 5 \tag{9.2.5}$$

Each of the sixteen processing units performs identical arithmetic operations, i.e. mod 5-based multiplications and additions. It can be shown, that the corresponding matrix multiplication result is

$$[C] = [A][B] = \begin{bmatrix} 1 & 3 & 3 & 2 \\ 0 & 4 & 2 & 4 \\ 2 & 0 & 1 & 0 \\ 4 & 0 & 3 & 2 \end{bmatrix} \quad mod \ 5 \tag{9.2.6}$$

To implement this 4 × 4 residue matrix multiplication, using a OIAP, the array shown in Fig.9.2.3(a) may be used. Input arrays A and B enter from the left and the top part of the processor. To guarantee the isochronous data arrival, a number of zero's are used. In Fig.9.2.3(b), an individual processing element, a mod 5 multiplier/accumulator, is depicted. White and black arrows represent the input and the SH beams. The residue multiplier performs on the two present inputs a mod 5 multiplication. Its result is first converted, from a SH to a fundamental frequency, and then added, using a mod 5 adder, to the adder's previous content. The optical delay line is adjusted so that the residue adder previous content arrives isochronously with the present multiplier output. After four recursions, at each element C_{ij} the desired output is generated. Using such residue OIAPs as building blocks, an all-optical matrix residue processor may be constructed.

9.3, Parallel Optical MSD Arithmetic

One problem with the residue number system is that it creates a nonsymmetrical computing structure because the hardware complexity for different modulo processors is

different. To synchronize, various optical delay lines must be used that reduces the computation speed. Thus, other number systems suitable for parallel computing have been sought. It has been indicated that the modified signed-digit (MSD) number representation is a candidate for fast, parallel digital optical arithmetic processing operations. The MSD, originally proposed by Avizienis[4] and introduced to optics community by Drake, Bocker and coworkers [5], uses a redundant binary representation that, after several parallel transfer and weight operations, leads to carry-free addition and subtraction. To optically synthesize both the transfer and weight logic functions, Drake et.al. proposed a location-addressable memory (LAM) logic. Bocker et.al.[12] generalized this method by using several symbolic substitution rules. With either method, addition (subtraction) can be performed in three (four) logic steps. Recently, Mirsalehi and Gaylord (M-G)[6] proposed, for the MSD addition, a direct truth-table look-up content-addressable memory (CAM). However, since for each output bit 56 Fourier holograms need to be stored, implementation difficulties, such a the practical holographic crystal multiplexibility and read-out efficiency, may be encountered. In this section, we first propose a set of new symbolic substitution rules that uses, instead of bit-wise substitution, a pair of reference bits for conditional bit-wise symbolic substitutions. With this method, both addition and subtraction operations can be implemented in two logic steps. For the optical synthesis of the required MSD logic elements, a holographic CAM technique is employed. With our method, for each logic output bit only a storage of up to 12 reference holograms is required. Compared to the M-G's approach, the burden on the high-density holographic storage is relaxed.

9.3.1, MSD numbers and algorithms

The MSD is a redundant radix-two number representation. Using a MSD, a number A can be represented as a string of symbols

$$A = \sum_i a_i \, 2^i \tag{9.3.1}$$

where the digits are $a_i \in [-1,0,+1]$. Here, only MSD integer arithmetic operations are discussed. With its balanced weighting factors, the MSD can represent both positive and negative numbers. For example, the decimal numbers $A = 11_{10}$ and $B = -11_{10}$ in the MSD system are

$$A = 1\bar{1}1\bar{1}_{MSD} \tag{9.3.2a}$$

$$B = \bar{1}1\bar{1}1_{MSD} \tag{9.3.2b}$$

where $\bar{1}$ denotes a negative one. A negative number can be obtained from its positive counterpart by taking bit-wise logic complement. For this reason, the MSD-based subtraction operation can be performed using a complement and add operation.

First, the MSD addition algorithm is discussed. For a MSD bit-wise addition, the six possible bit pairs to be added (see also Table 9.3.1) are (1,1); $(\bar{1},\bar{1})$; (0,0); $(1,\bar{1})$; (0,1) and $(0,\bar{1})$. The first two cases will generate a non-zero carry to its next higher level bit position, while the third and fourth bit pairs will, on the other hand, produce a zero carry to its left neighbor. The fourth case is particularly interesting since it can be used to stop carry propagation. The last two bit pairs can give redundant results where either no carry or a different signed carry is generated, i.e. either

$$0 + 1 = 1 + 0 = 01_{MSD} \quad \text{and} \quad 0 + \bar{1} = \bar{1} + 0 = 0\bar{1}_{MSD} \tag{9.3.3a}$$

or

$$0 + 1 = 1 + 0 = 1\bar{1}_{MSD} \quad \text{and} \quad 0 + \bar{1} = \bar{1} + 0 = \bar{1}1_{MSD} \tag{9.3.3b}$$

Using either Eq.(9.3.3a or 3b) together with the other four mentioned cases, two symbolic bit-wise substitution rules can be formed. By repeatedly using these two rules, in three substitution steps[12], both the result of MSD addition and its complement can be obtained. Specifically, the first two substitution operations rearrange the two add bit strings so as to eliminate, at the same bit position, the (1,1) and $(\bar{1},\bar{1})$ pairs. These two steps guarantee that

the last addition step is carry-free. It can be shown that the same state (i.e. no identical non-zero bits at the same position) can be reached via a single-step substitution, where instead of using two different rules for rearranging data, a compound rule is used.

9.3.2, Conditional symbolic substitution rules for MSD arithmetic

In our conditional symbolic bit-pair substitution method, in addition to the bit pairs to be substituted, the next lower level bit pair is used as the reference bits. Correspondingly, to prevent the generation of conflict bit-pairs, (i.e. (1,1) or $(\bar{1}\bar{1})$) in the rearranged results, all the $3^4 = 81$ possible bit combinations need to be considered. The conditional bit-wise substitution results for the bits (x_i, y_i), where the 81 possible combinations are reduced to 36 outcomes, are summarized in Table 9.3.2(a). This reduction is based on the fact, that for addition, its summand and addend can be interchanged. Each possible outcome is further sub-divided into two parts, a transfer (T_+) and a weight (W_+) function. Using this single-step conditional substitution rule, there will be no conflict bit pairs generated at the same bit position. To obtain the final addition and its complement results, the rearranged numbers are then added using a second substitution rule (see Table 9.3.2(b)). Note that Table 9.3.2(b) also contains two truth-tables; one for the addition (A) and another for its complement (C) operators, and as the result of the first step substitution, there are no input bit-pairs (1,1) and $(\bar{1},\bar{1})$.

As a numerical example of the new symbolic substitution rule, the addition of 1433_{10} + 758_{10} = 2191_{10} is performed. In the MSD representation, this addition is

$$\begin{array}{ll} & 10\bar{1}\bar{1}1010\bar{1}011\bar{1} \\ + & 1\bar{1}\bar{1}100\bar{1}10110 \end{array} \qquad (9.3.4)$$

After the conditional substitution, the addition of Eq.(9.3.4) becomes

$$\begin{array}{ll} & 1\bar{1}\bar{1}01000011\bar{1}\phi \\ + & \phi0100\bar{1}001\bar{1}\bar{1}01 \end{array} \qquad (9.3.5)$$

where two padding zeros, denoted as ϕ, are introduced. Using the second substitution rule, the final result is

$$1\bar{1}001\bar{1}00100\bar{1}1 \qquad \text{for } \textit{the addition result} \tag{9.3.6a}$$

and

$$\bar{1}100\bar{1}100\bar{1}001\bar{1} \qquad \text{for } \textit{the complement of addition} \tag{9.3.6b}$$

Eqs. (9.3.6a and 6b) are the MSD representations for the positive and negative number $\pm 2191_{10}$.

The conventional MSD subtraction operation uses a complement followed by an addition substitution rules. This method uses four logic steps[12] that consumes both processing time and logic elements. Since with the MSD arithmetic, a single-step full-adder does not exist, this four-step method is inefficient. To increase the MSD subtraction speed, next, a new two-step conditional symbolic substitution method is suggested. Using a combination of MSD logic complement and the above mentioned addition number rearrangement rule, the first three of the four conventional processing steps can be combined. In Table 9.3.3, where the operators T_- and W_- denote the transfer and weight functions, respectively, a conditional bit-wise subtraction substitution rule is summarized. Because with subtraction operation, the minuend and subtrahend can not be interchanged, a 9×9 truth-table is used. After this substitution rule, and using the previously defined A and C operators (see Table 9.3.2(b)), the rearranged numbers are added to generate the final result and its complement. Taking the previously used numbers as a subtraction example, we have

$$\begin{array}{ll} & 10\bar{1}\bar{1}10\bar{1}0\bar{1}1\bar{1} \\ - & 1\bar{1}\bar{1}100\bar{1}10110 \end{array} \tag{9.3.7}$$

After the T_- and W_- operations, the new bit strings are

$$\begin{array}{ll} & 000\bar{1}101\bar{1}\bar{1}00\bar{1}\phi \\ + & \phi0100\bar{1}0011\bar{1}01 \end{array} \tag{9.3.8}$$

where again, two padded zeros are used. Using the A and C operators, the two results are added to produce

$$00\bar{1}\bar{1}\bar{1}\bar{1}0\bar{1}\bar{1}\bar{1} \qquad \text{for } \textit{the subtraction result} \qquad (9.3.9a)$$

and

$$00\bar{1}\bar{1}\bar{1}\bar{1}1\bar{0}\bar{1}\bar{1}\bar{1} \qquad \text{for } \textit{the complement of subtraction} \qquad (9.3.9b)$$

Therefore, instead of the four step substitution, the new method generates the carry-free parallel subtraction in two successive substitution steps.

In Fig.9.3.1, using this two step substitution algorithm for $X \pm Y$, a MSD addition/subtraction flow diagram is shown. In the first substitution step, either T_+, W_+ or T_-, W_- operations are performed, while in the second step, the logic functions A and C are used. In the second step, the two A logic gates indicated by dashed line boxes can be omitted. Thus, to perform a two N-bit word parallel addition/subtraction, NT , NW , (N-1) A as well as (N+1) C logic gates are required. Since it is a very regular structure, it can easily be extended to perform both addition and subtraction for any size numbers. Using additional shift operators, MSD multiplication can also be performed. With the shift operators, first the partial products are formed. The parallel adders, forming a tree structure, are then used to add the intermediate results to yield the final product[9,10].

9.3.3, MSD content-addressable memory logic Processing

For the MSD operation, Drake et.al. employed a LAM method[10]. To implement each of the four LAM logic functions, twenty seven optical elements, including, arrays of holograms, etalons as well as prisms, are needed. It has been indicated that a CAM is more efficient than its LAM counterpart[6,13-15]. With a CAM, the truth-table outputs are first classified as to their logic levels. For each output level, corresponding to different input combinations, either a sum of product or a product of sum expression is obtained. With the aid of a Karnaugh map, a reduced logic expression (a reference pattern), is generated. These

patterns are then stored in an optical memory. By classifying and addressing its content rather than its truth-table location, the number of memory elements can be reduced. Using a CAM, direct binary truth-table look-up parallel addition and multiplication techniques have been proposed[13]. However, for long bit strings, a large truth-table (even after minimization) must be constructed. To alleviate this problem, a residue arithmetic-based CAM has also been utilized[13-14]. With a residue-based CAM, for example, for the addition of two 16-bit numbers, the truth-table is dramatically reduced, i.e. from the order of billion to only few hundred elements[15]. However, for either method, the storage complexity is not proportional to the size of the bit string. On the other hand, for MSD arithmetic, the storage complexity is linearly proportional to the bit string size. It has been shown, that using a direct CAM, for each MSD addition output bit, the storage of up to 56 holograms is required. In this section, to optically implement the above-mentioned conditional symbolic MSD logic operators, a new CAM method is described. Using two stages of these operators, either MSD addition or subtraction operation can be implemented. With this approach, by reducing the bit-wise memory storage density, practical optical construction will become possible.

The first CAM construction step is the minimization of the truth-table grouped logic expressions. To express our truth-table results, the sum of product form is chosen. Among the three $(\bar{1},0,1)$ possible groups, only two groups are of interest[15]. For the $\bar{1}$ and 1 output groups, using Karnaugh logic minimization maps together with the Tables 9.3.2 and 3, in Table 9.3.4, the reduced logic expressions are shown. Here, for the don't care bits, the notation is either an X for the completely don't care of $(\bar{1},0,1)$, or, a $X_{0,\bar{1}}$, $X_{0,1}$ or $X_{1,\bar{1}}$ for the a partial don't care for the pairs $(0,1)$ $(0,\bar{1})$ and $(1,\bar{1})$, respectively. In each four variable minterm, the two first (second) column bits denote the variables X_i, Y_i (X_{i-1}, Y_{i-1}), respectively. In the case of Table 9.3.3, instead of addressing 81 LAM outputs, only 6 CAM patterns are needed. It can be shown, that with the Takagi et.at. MSD addition truth-table [4], instead of our eighteen, with a less compact representation, more logic minterms are gen-

erated. Also, with this approach, a regular grouping, i.e. three (six) reduced minterm expressions for the T (W) function, for either MSD addition or subtraction, can be obtained. In comparison with M-G's single-step CAM method, and as a result of using the two steps, the addition speed decreases. However, in each step, the storage complexity is drastically reduced. For example, for the addition of two 16-bit numbers, while the M-G's method[6] requires a storage of 822 minterms, with the new two-step method, only 340 minterms are needed. Thus, the new method has the potential to process long bits-strings. In Table 9.3.5, a comparison between this and some of other methods are presented. It is noted, while in terms of processing speed, the single step method is the fastest, however, in terms of the product of the speed and number of reduced minterms, the two-step method is the optimum. Another advantage of the two-step method is, that since the complement of addition (subtraction) can easily be generated, it can be used for error-detection.

9.3.4, Optical Fourier hologram-based implementation

After this truth-table reduction, an optical memory is constructed. Here, an optical holographic technique[15], is used. In Fig.9.3.2, a CAM based MSD holographic logic recording and reconstruction system is shown. Each digit is spatially encoded with two vertical pixels. Transparent top (bottom) pixel indicates a logic level 1 ($\bar{1}$), while both opaque pixels indicate a logic level zero. For our conditional substitution rule, four ($X_i\ Y_i\ X_{i-1}\ Y_{i-1}$) parallel input bits are used. The other inputs are the general reference $R_{i(w)}$ and the reference transfer R_T and weight R_W logic bits, respectively. The optical memory consists of a thick Fourier hologram that is able to store a large number of angularly multiplexed spatial Fourier transform patterns. For each of the required minterms, three recording steps are used. For example, in Fig.9.3.3, the recording of the pattern ($1\bar{1}\bar{1}$x) for the T operator is indicated. During the first exposure, with the reference bit R_T, the complement pattern ($\bar{1}11$x) is recorded. In the second step, with a π phase shifted R_T, the input ($1\bar{1}\bar{1}$x) is recorded. In the last step, with the zero phase R_T the general reference R_i pattern is recorded. If with the first two recordings the bit-wise exposure (E) is identical, then, the

last step exposure should be mE where m is the number of second step nonzero signal digits. These three steps complete the recording process.

For logic operation, the R_T pixel is off while the signal and R_t pixels are on. For a prerecorded input, the light diffracted by the second and third step recorded patterns cancel (due to their identical magnitude and opposite phase) forming a dark pattern in the detected area. With a different input, the detected residue light is considered as a the input mismatch. To record a group of patterns, an angular multiplexing method that employs a group of reference pixels, e.g. the dotted squares in Fig.9.3.4, is needed. It can be shown that the don't care digit can be assigned to the patterns as shown in Table 9.3.6 where, in the last column, n denotes the number of don't care bits. To perform MSD logic operations, both the spatially encoded bit-strings and reference bit arrays are used. In Fig.9.3.5, a holographic CAM logic device for implementing the MSD addition (subtraction) operators $T_{+(-)}$ and $W_{+(-)}$ is shown. For each of the three (six) required patterns (see Table 9.3.4) for $T_{\pm}(W_{\pm})$, using this and a spatially encoded reference pixel pattern R_T (R_W), an angularly multiplexed hologram is formed. Also, for the recording and later reading, an array of general reference $R_{t(w)}$ pixels are used. At the output side, two detector arrays, D_T and D_W, with each divided into two parts for detecting a 1 and $\bar{1}$ are used. The absence of light in one part of a detector indicates a nonzero while the presence of light on both detectors assigns a zero to the output. These output signals can be used to generate inputs for a next stage logic function.

9.4, Summary

To summarize, in this chapter, two additional optical non-binary arithmetic processing techniques are proposed. In the first scheme, parallel processing using optical residue arithmetic was performed. Optical SHG switching arrays were used to form various mapping units that performs specific modulo addition and subtraction. We also presented a SHG mod-p multiplier based on a mod-(p-1) addition unit. Using residue multiplication units together with some additional interconnection schemes, a residue matrix-matrix multiplier

was also described. The major advantages of these proposed devices are first the ultrafast processing speed can be reached and second the device can easily be monolithically integrated. an altern the second part of this chapter, an alternative method to perform the MSD arithmetic was proposed. A set of new MSD addition and subtraction symbolic substitution rules were presented. Instead of using three and four processing steps to implement MSD addition and subtraction, the new methods use only two steps. For an optical implementation, a CAM processing technique was used. First, to obtain a reduced logic (in a sum of minterm form), or equivalently a reduced reference pattern, logic minimization is performed. To record these reduced reference patterns, an angularly multiplexed thick Fourier hologram recording setup was described. The stored holograms optically implement the required logic substitution elements.

9.5, References

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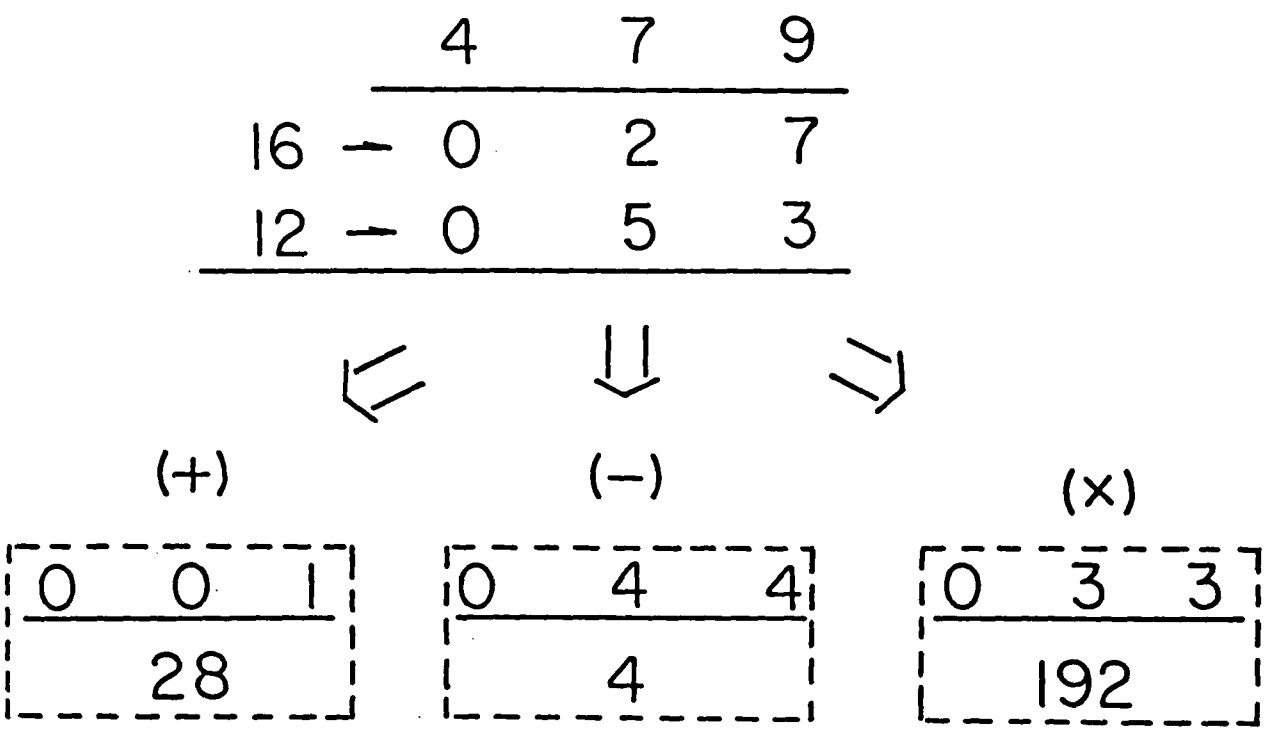

Table 9.2.1 Examples of Residue addition, subtraction and multiplication of two unsigned integers. Integers 4, 5, and 9 are chosen as moduli.

	1	$\bar{1}$	0	1		0			0			
+	1	$\bar{1}$	0	$\bar{1}$		1			$\bar{1}$			
carry	1	$\bar{1}$	0	0	1	or	$\bar{1}$	$\bar{1}$	or	1		
sum	0	0	0	0	0		1	0		$\bar{1}$		

Table 9.3.1 MSD addition six possible bit-pair carries and sums.

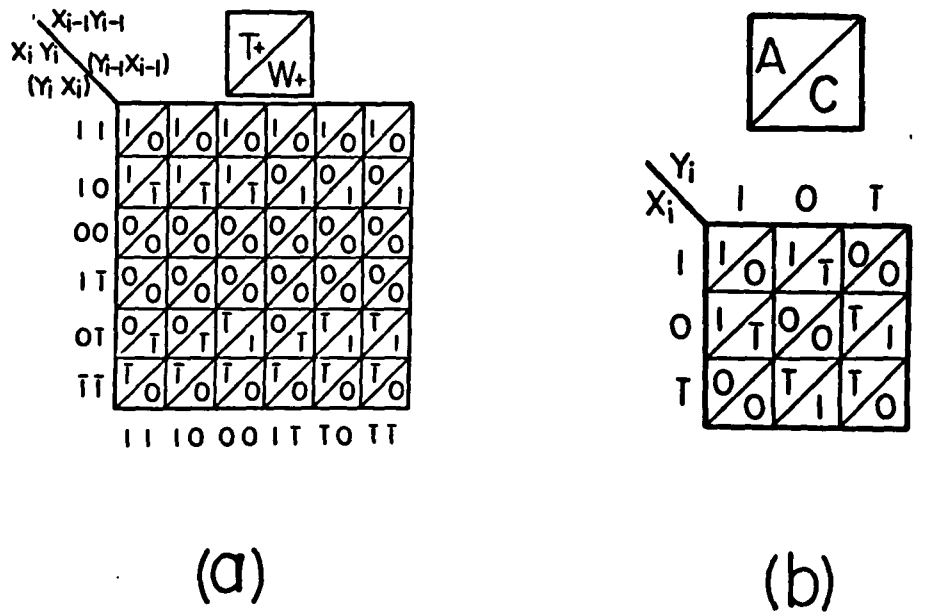

Table 9.3.2 (a) First MSD addition conditional symbolic substitution rule truth table for rearranging data: T_+ (W_+), the corresponding transfer (weight) operator. (b) Second MSD addition bit-wise symbolic substitution rule truth table: A (C), the sum (complement of the sum) operator.

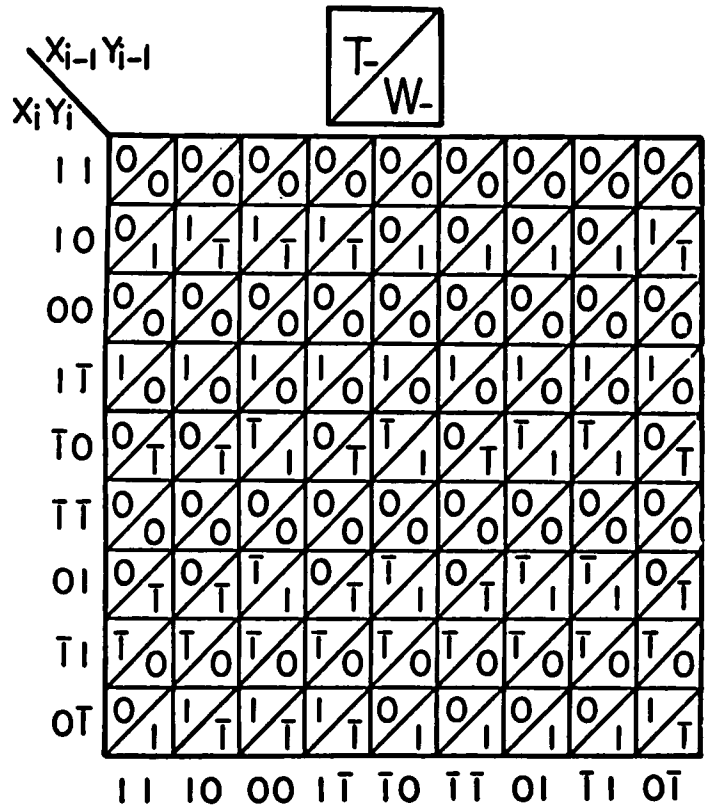

Table 9.3.3 First MSD subtraction conditional symbolic substitution rule truth table (converting the subtraction to addition operation and rearranging the addition data: $T\_(W\_)$, the corresponding transfer (weight) operator).

MSD logic	bit	reduced minterm	MSD logic	bit	reduced minterm
T_+	1	$1X \quad 1X_{01} \quad 0X_{01}$ $1X, \quad 0X_{01}, \quad 1X_{01}$	W_+	1	$1\bar{1} \; 1X \; 0\bar{1} \; 0X \; \bar{1}X_{0\bar{1}} \; 0X_{0\bar{1}}$ $0X, 0\bar{1}, \; 1X, 1\bar{1}, \; 0X_{0\bar{1}}, \bar{1}X_{0\bar{1}}$
	$\bar{1}$	$\bar{1}X \quad \bar{1}X_{0\bar{1}} \quad 0X_{0\bar{1}}$ $\bar{1}X, \quad 0X_{0\bar{1}}, \quad \bar{1}X_{0\bar{1}}$		$\bar{1}$	$\bar{1}1 \; \bar{1}X \; 01 \; 0X \; 1X_{01} \; 0X_{01}$ $0X, 01, \; \bar{1}X, \bar{1}1, 0X_{01}, 1X_{01}$
T_-	1	$1X \quad 1X_{01} \quad 0X_{01}$ $\bar{1}X, \quad 0X_{0\bar{1}}, \quad \bar{1}X_{0\bar{1}}$	W_-	1	$1\bar{1} \; 1X \; 0\bar{1} \; 0X \; \bar{1}X_{0\bar{1}} \; 0X_{0\bar{1}}$ $0X, 01, \; \bar{1}X, \bar{1}1, 0X_{01}, 1X_{01}$
	$\bar{1}$	$\bar{1}X \quad \bar{1}X_{0\bar{1}} \quad 0X_{0\bar{1}}$ $1X, \quad 0X_{01}, \quad 1X_{01}$		$\bar{1}$	$01 \; 0X \; \bar{1}1 \; \bar{1}X \; 1X_{01} \; 0X_{01}$ $1X, 1\bar{1}, 0X, 0\bar{1}, 0X_{0\bar{1}}, \bar{1}X_{0\bar{1}}$
A	1	$1 \quad X_{01}$ $X_{01}, \quad 1$	C	1	$0 \quad \bar{1}$ $\bar{1}, \quad 0$
	$\bar{1}$	$\bar{1} \quad X_{0\bar{1}}$ $X_{0\bar{1}}, \quad \bar{1}$		$\bar{1}$	$0 \quad 1$ $1, \quad 0$

Table 9.3.4 The reduced logic minterm expressions for the implementation of the MSD addition and subtraction operations. The X denotes a don't care as specified in Table 9.3.6. The four variable minterm is grouped as $\begin{bmatrix} x_i & x_{i-1} \\ y_i & y_{i-1} \end{bmatrix}$.

methods	No. of gates	No. of refs. for each gate	total No. of refs.	normalized speed
1-step	N+1	$\leqslant 56$	56N-74	T
2-step	3N-1	$\leqslant 12$	22N-4	2T
3-step	5N-3	$\leqslant 4$	18N-10	3T

Table 9.3.5 A comparison among the one-, two- and three-step N-bit CAM MSD addition schemes. In terms of processing speed, the 1-step method is the fastest, while in terms of the product of the speed and total number of references, the 2-step method is the optimum.

don't care type	patterns to be recorded 0-phase	patterns to be recorded π-phase	$R_{1(\bar{w})}$-bit exposure
X	■	■	mE
$X_{0\bar{1}}$	□	■	mE
X_{01}	□	■	mE
$X_{\bar{1}1}$	■	□	(m+n) E

Table 9.3.6

Various MSD don't care types and their corresponding spatial encoding: m, n and E denote the number of non-zero, the number of don't care bits and the single general reference bit exposure, respectively.

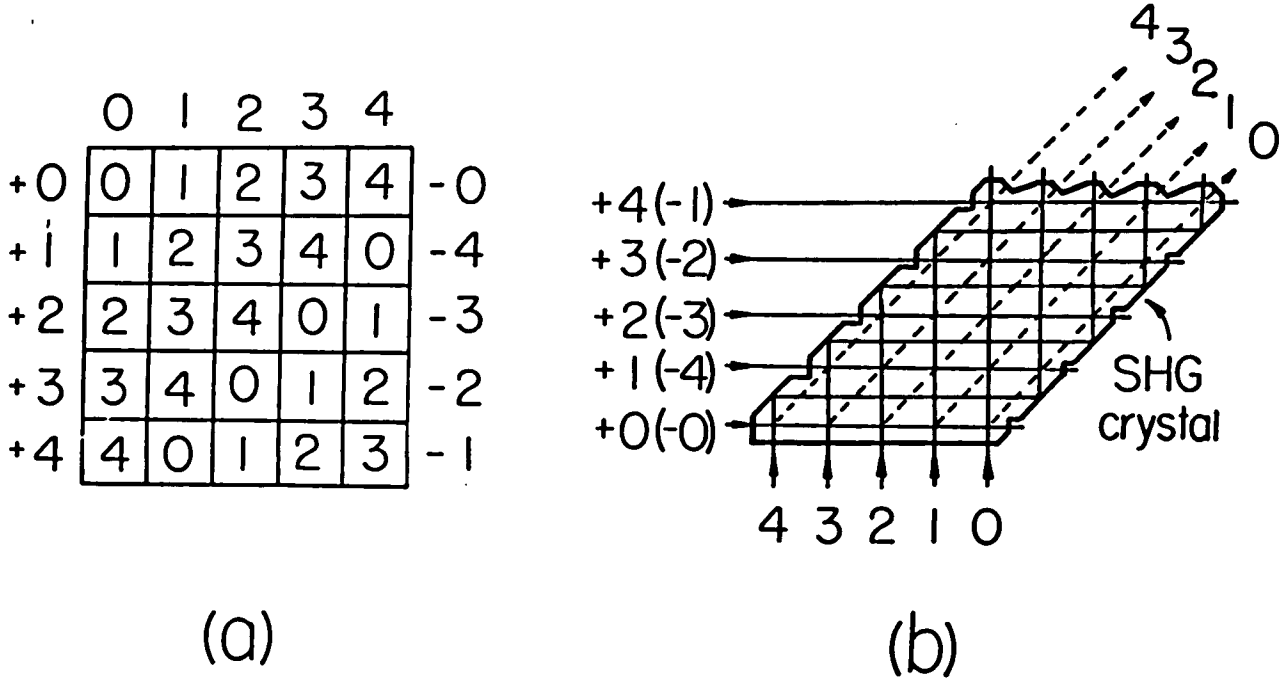

Fig.9.2.1 (a) Mod-5 residue addition (subtraction) truth table. (b) A SHG-based mod 5 residue optical adder implementation. At the interfaces, total internal reflections are used.

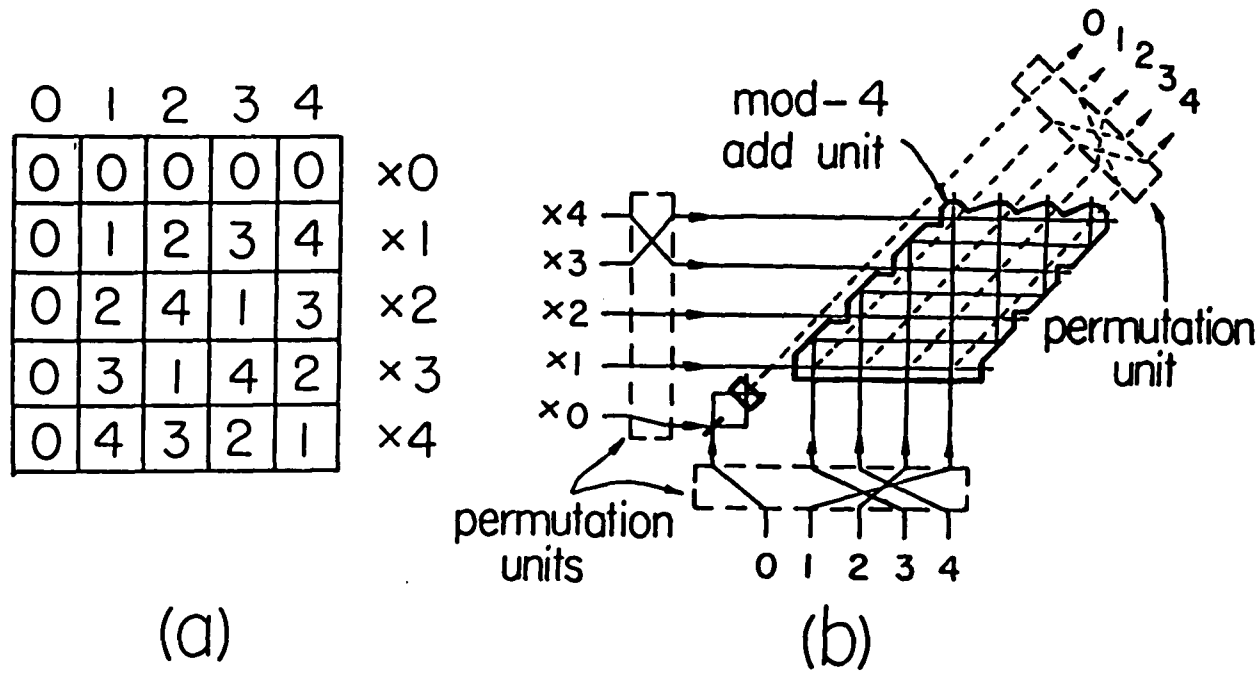

Fig.9.2.2 (a) Mod-5 residue multiplication truth table. (b) A SHG-based mod 5 optical multiplication implementation. Two SHG crystals, one for a mod 4 addition and another to handle the zero, are shown. Also, a pre- and a post-permutation devices are also used.

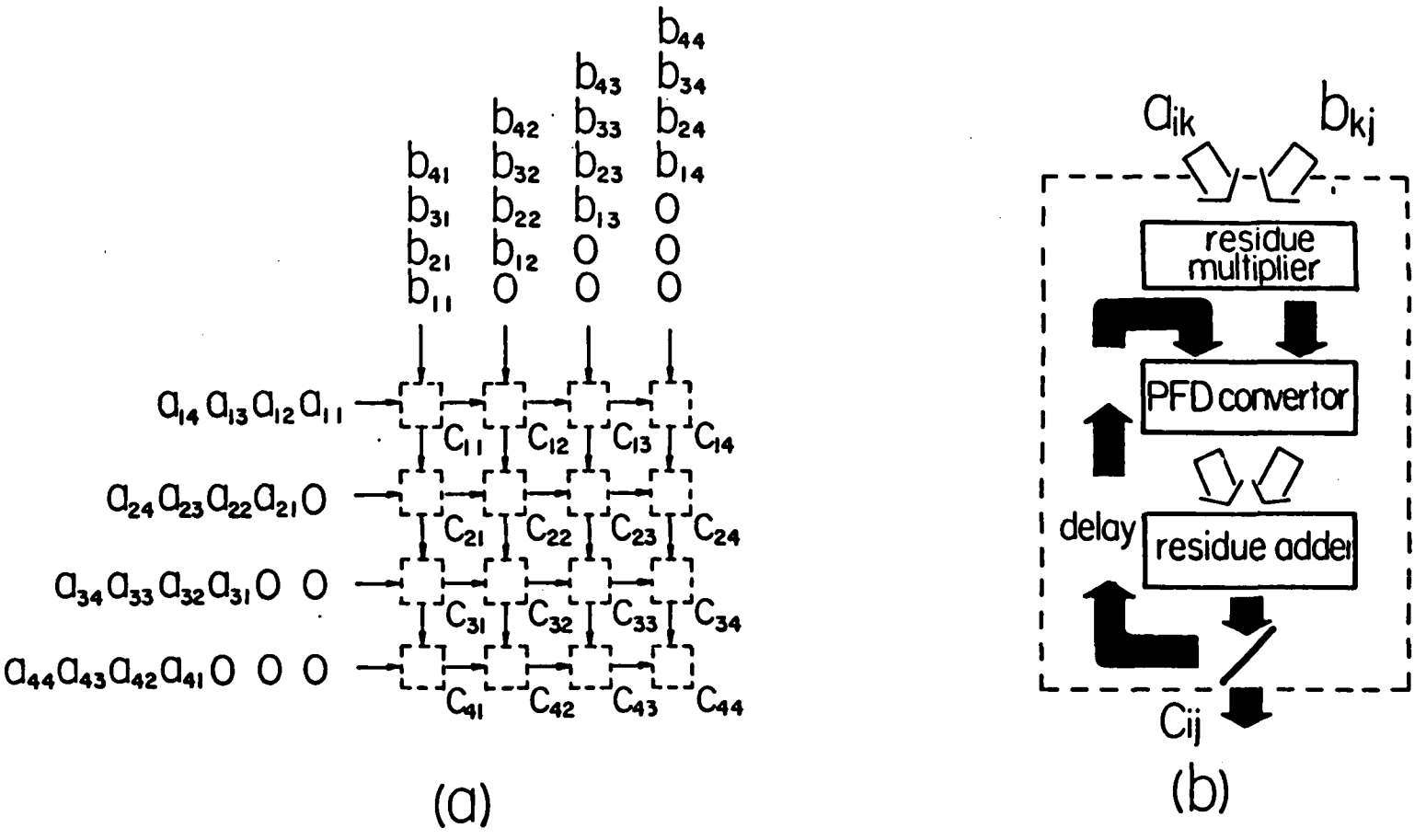

Fig.9.2.3 (a) A 4×4 residue matrix-matrix multiplier with sixteen identical arithmetic processing cells C_{ij}. (b) A SHG-based C_{ij} cell that employs a mod 4 multiplier and a mod 4 adder. Black and white arrows represent the SH and the fundamental frequency beams. In addition to the adder and multiplier, a PFD conversion device is needed.

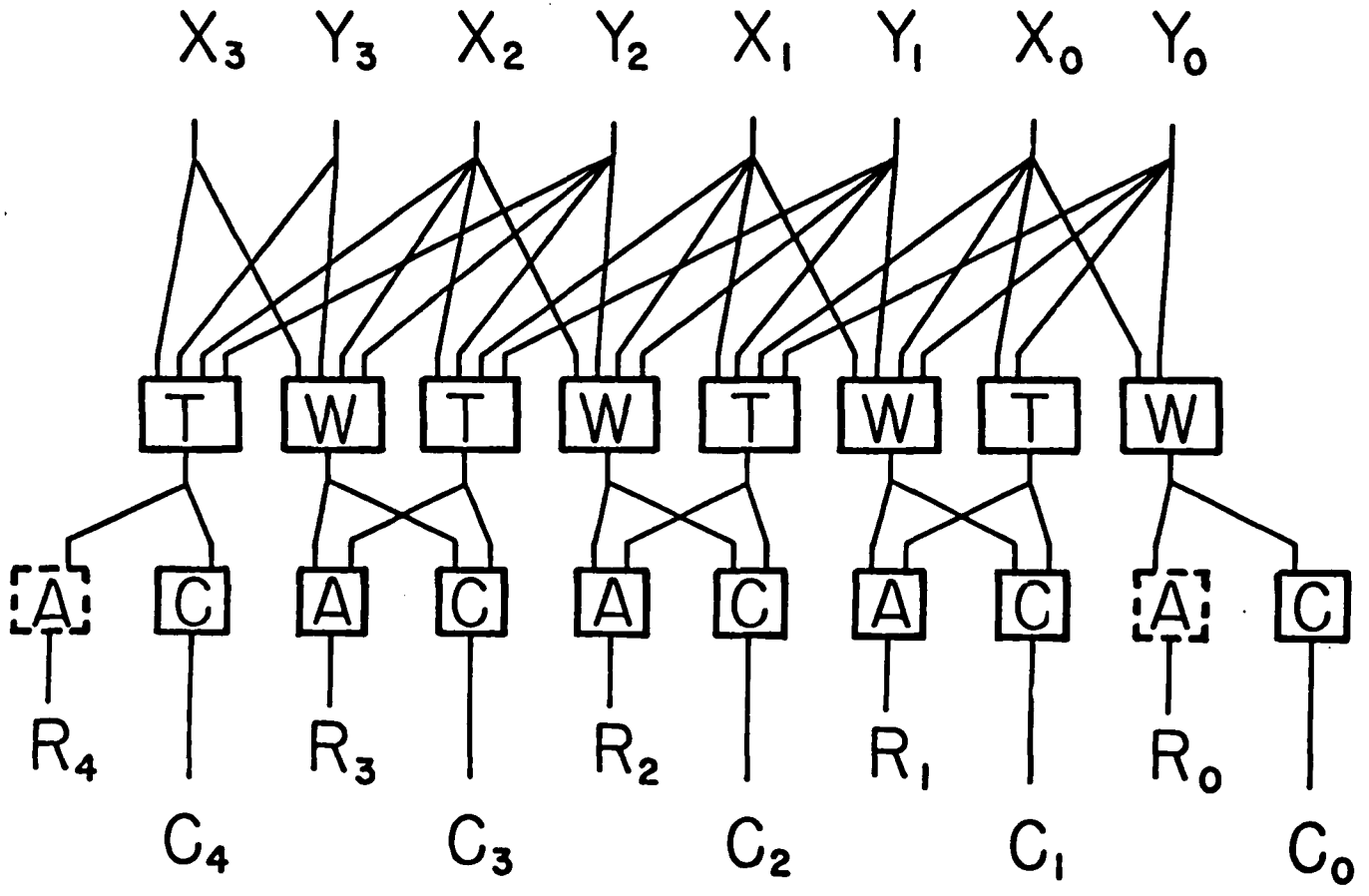

Fig.9.3.1 A four digit MSD addition (subtraction) network. X (Y), input strings; T (W), transfer (weight) operators for addition or subtraction; A (C), operators to obtain the final addition (subtraction) result R and its complement (C). The operators indicated within the dashed boxes may be deleted.

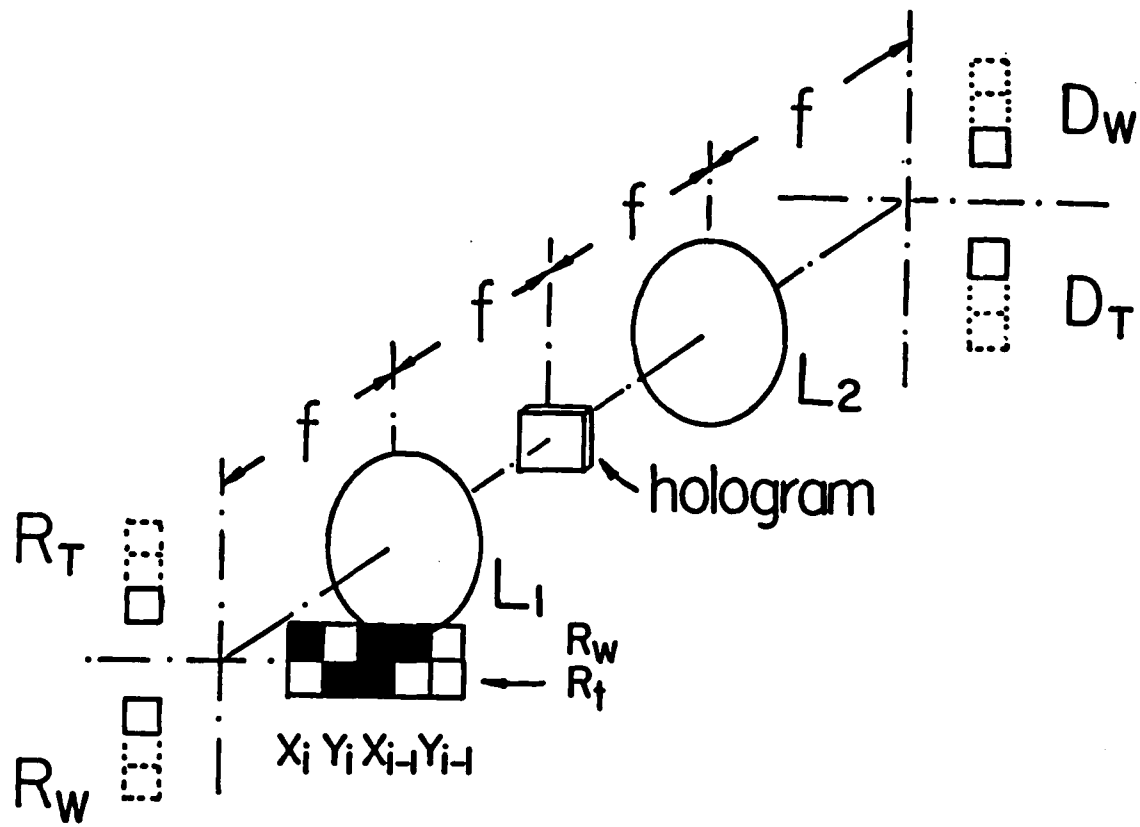

Fig.9.3.2 A holographic CAM recording and logic processing unit. X (Y), the input variables; $R_{t(w)}$ and $R_{T(W)}$, the general reference and the reference for the transfer (weight) operations, respectively; $D_{T(W)}$, detector array for logic T (W) operation.

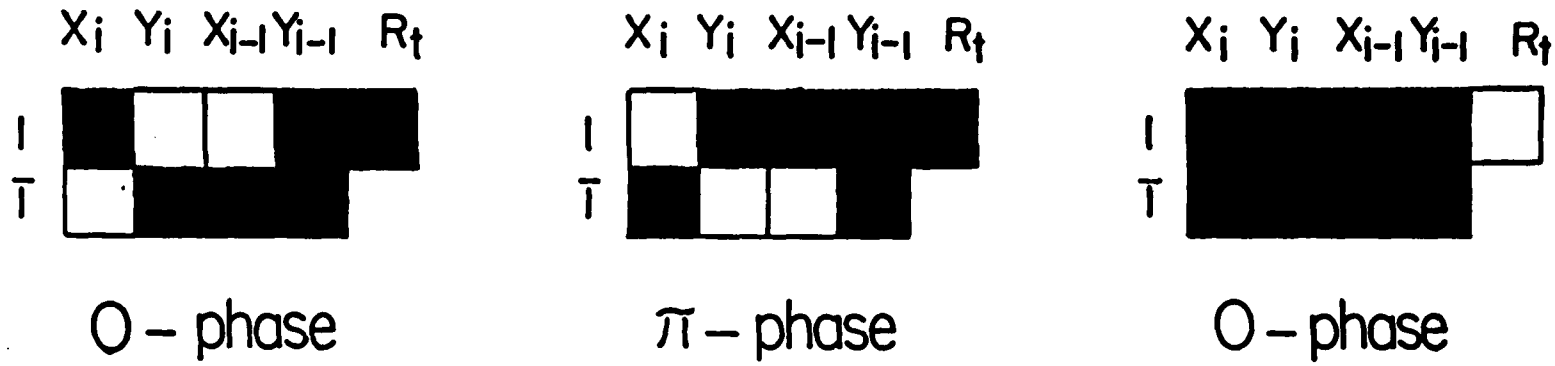

Fig.9.3.3 Holographic CAM-based MSD processing for the pattern $1\bar{1}1X$. Three recording steps are used.

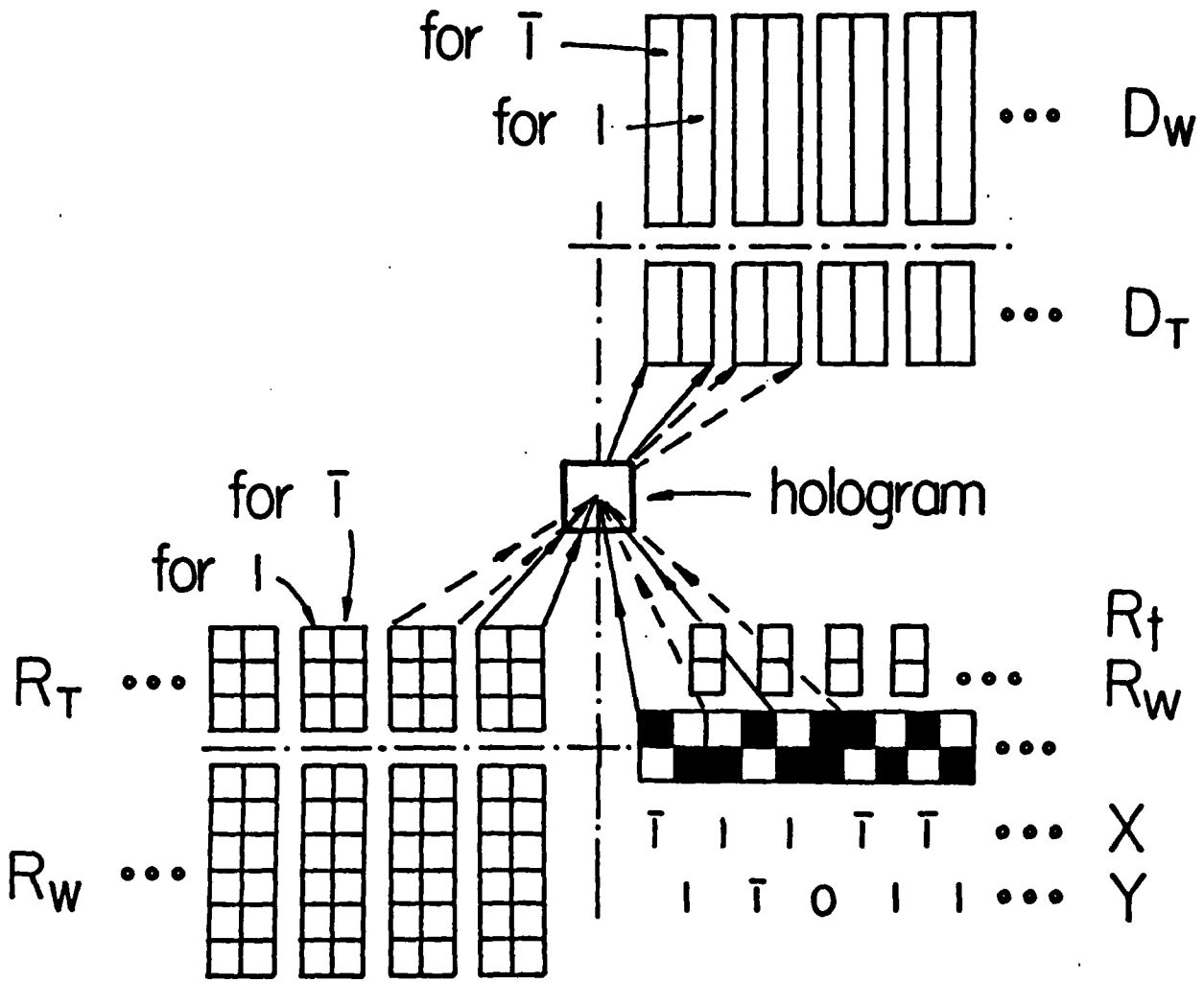

Fig.9.3.4 A schematic setup for implementing the MSD T and W logic operations using a holographic CAM-based system.

X. SUMMARY AND FUTURE DIRECTIONS

10.1, Summary

In this thesis, various new schemes to implement optical digital computation elements and processors have been described. Some of them have been demonstrated. For the optical implementation of ultrafast logic gates, interferometric approaches have been used. The proposed ultrafast Sagnac interferometric logic switches have a better mechanical stability over other two beam interferometric switching geometries. Using nonlinear materials in a Sagnac loop, various binary and multiple-valued optical logic elements have been proposed. In this thesis, alternative optical logic switching geometries have also been studied. Using a optical phase conjugation cell, an ultrafast optical pattern logic scheme has been proposed and demonstrated. The major advantage of this type of optical logic elements is that together with a transparent/opaque logic code, it can perform all sixteen two-input Boolean logic functions. With other, such as polarization, encoding methods, optical implementation of multiple-input binary as well as multiple-valued logic operations have also been studied. In addition to optical logic elements, the implementation of an optical sampler, an A/D converter, a dynamic cross-bar, as well as perfect shuffles, have been described. Most of these elements use the parallel and ultrafast processing advantages of optics. Using a Sagnac interferometric sampler, the sampling frequency can be doubled with respect to other existing sampling geometry. Using the proposed theta-modulation-based optical A/D converter, a fast (nano- and subnanosecond), compact and flexible A/D conversion can be performed. Compared to other existing parallel data shuffling geometries, the implementation methods described in this thesis is more compact and efficient. Also, using the proposed phase-conjugation-based dynamic cross-bar, the parallel interconnection speed has been

increased from microsecond to picosecond region. In this thesis, for the optical numerical processing, various binary and non-binary computing structures have also been investigated. In the binary case, using a number of cascaded Sagnac interferometers, the optical implementations of a full adder and an array multiplier have been described. The optical multiplication using the digital multiplication via analog convolution algorithm has also been studied. Using ultrafast noncollinear second harmonic generation effect, the ultrafast data convolution pre processing has been discussed. The proposed method is generally suitable for ultrafast pre-processing involving scalar, vector and matrix multiplication operations. In the non-binary optical numerical processing case, a number of new processing methods have been described. Using Sagnac interferometer-based approach, the optical binary coded ternary adders have been proposed. Based on residue arithmetic, using optical second harmonic generators, a number of ultrafast optical residue computing structures were presented. Finally, a new approach to implement a content-addressable memory-based modified sign-digit addition and subtraction elements have been described.

10.2 Future Direction

Among various proposed processors, OPC- and SHG-based schemes, because of their ultrafast speed and parallel processing nature, can have numerous scientific and engineering applications in the future. For the practical use of these processors, further research on the following areas should be carried on. These areas include the development of (1) faster and more efficient nonlinear materials, (2) real-time parallel input encoding schemes, (3) proper signal amplification and frequency conversion schemes, and (4) device integration and miniaturization techniques. These are discussed.

10.2.1 Processing speed

In the OPC-based computing experiments presented above using CS_2 nonlinear material with 2 ps response time and 32 ps YAG laser pulses, the speed in generating a page of parallel outputs are limited by the input pulse width. For faster operation, faster

third-order nonlinear materials and shorter laser pulses must be used. The combination of femtosecond dye-laser pulses and the future new ultrafast nonlinear optical materials, such as multiple-quantum-well microstructured semiconductors[1], semiconductor-doped 0-D glasses[2] and layers of organic polymers[3], offers a much faster OPC operation. Although femtosecond processing speed can be reached with the use of SHG-based computation structures, efficiency of most second-order nonlinear material is low. To increase the efficiency, new materials, such as KTP, KNO_3 and PTS, may be helpful. Any way, to make a reliable and efficient optical computing device, development of new fast and efficient materials is the most important subject for future research.

10.2.2 Real-time input and output modulators

For a fast device operation, in addition to a fast gate or processor, a fast input and output modulation scheme must also be implemented. With present technology, the available optical spatial light modulators can only modulate input in microseconds. This speed, compared to our gate processing speed, is too slow. To keep up the overall computation efficiency, at least picosecond modulation on an input is needed. One possible fast input modulation candidate is an E-O deflector that can perform fast input voltage to output angle deflection[4]. In particular, a $LiNbO_3$ E-O waveguide deflector, a standard E-O prism deflector, has been miniaturized to a waveguide structure. Using this device, a multi-leveled (9 resolvable positions) deflection was probed in less than 10 nanoseconds. For a binary deflection between two points, picosecond operation of this device is possible. Thus, this scheme is generally suitable and needs to be further developed for the logic processor initial input modulation. To increase the speed further, all-optical deflection should also be investigated. Among various ultrafast switching schemes, nonlinear dynamic grating that can have pico and sub-picosecond response may be a helpful scheme for an ultrafast input modulation[5]. In fact, such a light controlled ultrafast deflection using a dynamic grating has been experimentally reported. At the present stage, the efficiency is still too low.

After each stage logic signal processing, to convert an output to the next stage binary input, a number of approaches should be investigated. Using either space-variant hologram[6] or cross-bar interconnect, the previous stage output signal can be scripted to the form required for the next stage processing. For non-binary and multiple-bit binary arithmetic and logic processing, the logic and number encoding should be performed by a 2D beam modulator. Therefore, research on all-optical ultrafast bistable etalons for the fabrication of 2D array modulators needs to perform.

10.2.3 Signal amplification for multistage logic operation

An important practical problem affecting the multi-stage operation is the signal fan-out. With most known ultrafast nonlinear materials, the strength of the nonlinearity is limited. In most cases, the SHG or OPC output is always much weaker (a few percent or less) than an input signal. To increase the output power with existing nonlinear materials, two amplification approaches for the device multistage operation need to be investigated. In a first (suitable for the OPC signal amplification), a direct, amplification scheme, the use of large nonlinearity material with the increased beam interaction length may be helpful. With CS_2 nonlinear material, a gain of three has been experimentally demonstrated[7]. When some higher nonlinearity materials, such as organic polymers and semiconductor multiple-quantum-wells, are used, higher amplifier gain with shorter interaction length can be expected.

In a second (suitable for both OPC and SHG signal amplification), a nonlinear parametric, amplification scheme, the use of an external strong laser pulse to deliver power to both the weak signal and the idler beams[8] may be helpful. When a signal (ω_1) and a strong pump beam (ω_3) are mixed in a second-order nonlinear material with an appropriate phase-matching geometry, due to nonlinear wave coupling, at the output, an amplified ω_1 and an idler ω_2 where $\omega_2 = \omega_3 - \omega_1$ signal will be obtained. Depending on material nonlinearity, input power density as well as interaction length, different gains on both ω_1 and ω_2 signals can be obtained. This parametric amplification scheme has widely been used in

ultrafast phenomena investigations where laser power is required at a particular wavelength. Since a large gain can be obtained using some crystals (e.g. a gain of $G = 10^4$ has been observed with NPP crystal[9]), the scheme can also be used for amplifying both our SHG and OPC logic outputs. For the SHG ($\omega_1 = 2\omega$), both wavelength and power needs to be converted. Thus, the pump beam may be chosen as a fundamental beam's third-harmonic (TH), i.e. $\omega_3 = 3\omega$. The use of a strong TH beam to mix with the weak SH can generate a strong idler beam at fundamental frequency. With a KDP crystal, this concept has been experimentally demonstrated[10]. In another approach, instead of TH, the use of a strong fundamental frequency $\omega_3 = \omega$ beam needs also be investigated. As a result, a new fundamental frequency idler $\omega_2 = \omega$ signal is obtained.

Along the same line, the methods to amplify OPC signal should also be investigated. Since there is no frequency conversion involved, the amplification scheme will be simpler. In particular, the weak OPC signal can be amplified by a strong pump beam with a SH frequency (a degenerate amplification can give a maximum amplification efficiency). In either case, for an efficient amplification, the new second order nonlinear materials, such as KTP, KNO^3 and NPP, can be used.

10.2.4 Device miniaturization

To compete with electronic chips, a practical optical circuit needs also to be integrated. Thus, another research direction will be to miniaturize these SHG- and OPC-based computing devices to integrated circuit scales. Instead of the large scale picosecond YAG and dye lasers a mode-locked semiconductor diode laser should be employed. Using various crystals and organic polymers, lattice-shaped 1-D, 2-D or 3-D SHG or OPC waveguides must be implemented to replace the currently used bulk materials. Other practical problems to be considered for a fast, efficient optical circuit miniaturization are the laser diode fan-out, size and speed, source-channel and channel-detector coupling efficiency, as well as detector size, response.

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XI. LIST OF THE THESIS RELATED PUBLICATIONS

A. Journal Articles:

(1) "Pulsed Mode Sagnac Interferometry with Applications in Nonlinear Optics and Optical Switching," Y. Li, G. Eichmann and R. R. Alfano, Appl. Opt. 25, Jan.15, (1986) p 209-214.

(2) "Optical Computing and Logic Using Sagnac Interferometric Switches," G. Eichmann, Y. Li, M. Conner and R. R. Alfano, Proc. SPIE, 625 (1986) p.79-86.

(3) "Digital Optical Logic Using Sagnac Interferometer Switches," G. Eichmann, Y. Li and R. R. Alfano, Opt. Eng. 25, Jan. (1986) p. 91-97.

(4) "Moire Deflectometry of Phase Objects Using a Single Grating," Y. Li and G. Eichmann, Appl. Opt. 25, Feb. 15, (1986) p. 477-479.

(5) "Optical computing using hybrid encoded shadow casting," Y. Li and G. Eichmann, Appl. Opt. 25, Aug.15, (1986) p. 2636-2638.

(6) "Optical Binary coded ternary arithmetic and logic," G. Eichmann, Y. Li, and R. R. Alfano, Appl. Opt. 25, Sept.15, (1986) p.3113-3121.

(7) "Ultrafast nonlinear optical processes in 4BCMU-Polydiacetylene," P. P. Ho, R. Dorsinville, N. L. Yang, G. Odian, G. Eichmann, T. Jimbo, Q. Z. Wang, G. C. Tang, N. D. Chen, W. K. Zou, Y. Li, and R. R. Alfano. Proc. SPIE, 682, (1985) p.36-43.

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(9) "Optical binary coded multivalued arithmetic and logic using two-port Sagnac interferometric switches," G. Eichmann, Y. Li, and R. R. Alfano, Proc. SPIE, 700. (1986) p.251-258.

(10) "Parallel optical logic generation using optical phase conjugation," G. Eichmann, Y. Li, and R. R. Alfano, Appl. Opt. 26, (1987) p.194-196.

(11) "Compact optical generalized perfect shuffle," G. Eichmann and Y. Li, Appl. Opt. 26, (1987) p.1167-1169.

(12) "Conditional symbolic modified signed-digit arithmetic using optical content-addressable memory logic elements," Y. Li, and G. Eichmann, Appl. Opt. 26, (1987), p.2328-2333.

(13) "Digital optical isochronous array processing," G. Eichmann, Y. Li, and R. R. Alfano, Appl. Opt. 26, (1987), p.2726-2732.

(14) "Fast parallel optical digital multiplication," Y. Li, G. Eichmann, and R. R. Alfano, Opt. Comm. 63 (1987), in press.

(15) "A phase-conjugation-based optical symbolic recognizer," Y. Li, G. Eichmann, R. Dorsinville, and R. R. Alfano, Opt. Comm. 63 (1987), in press.

(16) "Ultrafast optical computing networks using nonlinear optical second harmonic generation," Y. Li, G. Eichmann, X. Luo, P. P. Ho, and R. R. Alfano, submitted to Opt. Comm. for publication.

(17) "Ultrafast parallel optical digital and symbolic computation via optical phase conjugation," Y. Li, G. Eichmann, R. Dorsinville, and R. R. Alfano, submitted to Appl. Opt. for publication.

B. Conference Presentations:

[1] Y. Li, G. Eichmann, and R. R. Alfano, "Optical Switching Using a Sagnac Interferometer," 1985 OSA Annual Meeting, Washington, D.C. Oct. 1985.

[2] G. Eichmann, Y. Li, M. Conner, and R. R. Alfano, "Optical Computing and Logic Using Two-port Sagnac Interferometric PIE Conference on Digital Optical Computing, Los Angelas, CA. Jan. 1986.

[3] G. Eichmann, Y. Li, and R. R. Alfano, "Optical Binary Encoded Multivalued Arithmetic and Logic Using Two-port Sagnac Interferometric Switches," International Conference on Digital Optical Computation, Israel, July, 1986.

[4] Y. Li, G. Eichmann, P. P. Ho, and R. R. Alfano, "Optical Digital Computing Using Noncollinear Second Harmonic Generation," APS Annual Meeting, New York, NY, March, 1987.

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[6] Y. Li, and G. Eichmann, "Optical Modified Sign-Digit Arithmetic Using Conditional Symbolic Substitutions," to be presented at the OSA Annual Meeting, Rochester, NY, Oct. 1987.

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