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DIGITAL PROCESSING IN COMMUNICATION SYSTEMS

By

Joseph Garodnick

A dissertation submitted to the Graduate Faculty in Engineering in partial fulfillment of the requirements for the degree of Doctor of Philosophy, The City University of New York.

1972

This manuscript has been read and accepted for the Graduate Faculty in Engineering in satisfaction of the dissertation requirements for the degree of Doctor of Philosophy.

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date — Chairman of Examining Committee

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ABSTRACT

DIGITAL PROCESSING IN COMMUNICATION SYSTEMS

by

Joseph Garodnick

Adviser: Professor Donald L. Schilling

The creation of real-time special purpose digital computers is resulting in an enhancement of existing communication systems and the invention of new, sophisticated, versatile approaches to information transmission. Up to this time, computers were used mainly for system simulation and for systems where the time constants are many orders of magnitude greater than existing processing time. The application of computers to real-time processing of communication systems is relatively new, and an entirely new class of problems have emerged. These problems are of the form of logic speed limitations, quantization errors, roundoff and overflow errors. Three communication systems using digital processing techniques are presented in this thesis and analyzed both theoretically and experimentally.

The first system is an All Digital Adaptive Delta Modulator. Delta modulation, DM, is a one bit differential

source encoder that saves bandwidth at the expense of dynamic range. In 1969, C. L. Song derived the system equations for an optimum least mean square error DM. This optimum system provided the same output SNR as other systems but (theoretically) had an "infinite" dynamic range. In this thesis, Song's highly nonlinear system equations are approximated by piecewise linear equations and the system realized. While linear delta modulation is limited in dynamic range because of a fixed step size predictor, the described scheme varies its step size to one of 1024 possible values, adapting itself to input signal power. Experimental results are obtained for pseudo-random data inputs, squarewave inputs, sinewave inputs as well as for human voice. These results have been compared to systems designed by other investigators and have been found to be subjectively and objectively superior.

The second system is an All Digital FM Discriminator. This device frequency demodulates the input signal by digitally measuring the time between the zero-crossings. Both theoretical and experimental results for the output signal-to-noise ratios versus input carrier-to-noise ratios are obtained. The results include the effects of thermal noise, impulse noise, and quantization noise. Theoretical and experimental results differ by less than 1dB which is within our measurement accuracy. System design equations are presented that allow the digital discriminator to be applied to many frequency demodulation systems. An algorithm

is invented so that with a fixed internal clock frequency, the device can extend its operation to higher carrier frequencies.

Finally, an All Digital Phase Locked Loop, DPLL, used for FM demodulation, is analyzed, designed and constructed. The restrictions imposed by the digital circuitry necessitate the invention of new algorithms, including a digital VCO algorithm to allow the DPLL to operate in real-time. The algorithm eliminates the need for a continuous voltage controlled oscillator by computing the value of an oscillator at the sampling times. Time consuming digital multiplication is circumvented by employing a square-wave VCO that either inverts or noninverts the input signal at the phase detector. In addition, the sampling frequency is carefully chosen so that the FM signal is subsampled yielding a greater time for digital processing. The performance of the system in response to FM signals is determined theoretically and experimentally. Included are the effects of thermal, impulse and quantization noises. A comparison of theoretical and experimental results justify the algorithms employed and verify the theory.

The description of the three communication systems in this dissertation demonstrates the analytical and experimental techniques which are used to apply digital processing to real-time special purpose computers.

When only one combination
of two bodies can be obtained,
it must be presumed to be a Binary
unless some cause appear to the contrary.

—— JOHN DALTON 1808

ACKNOWLEDGEMENT

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Appreciation is also expressed to the staff of the Electrical Engineering Department of The City College of The City University of New York, without whose support and cooperation, this treatise could not have been completed.

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Chapter 1

INTRODUCTION

Digital systems have been emphasized considerably in the past decade because of their intrinsic trouble free operation, the multiplexed signal handling capabilities, and the complex processing techniques possible through special and general purpose digital computers. Also the digital evolution has allowed complexity in hardware to increase, while size, cost and power consumptions constantly decrease. Hence, functions previously deemed impossible to implement are now being constructed in production facilities. When digital techniques are used for source encoding, the information is transmitted and received with small probability of error compared to analog signals, especially when carriers and media take the form of laser beams and fiber optics.

A myriad of articles has been written concerning computer simulation of real time systems, but comparatively few papers pertain to the actual implementation of a digital system and the restrictions and considerations involved [1-1]. The majority of real-time processing available in the literature concerns itself with systems having extremely lengthy time constants compared to current logic speeds. Many chemical processes where time

constants are minutes or days are suitable for general purpose real-time computer application. However, where voice and video information must be processed, time constants become of the order of milliseconds and microseconds, and other techniques must be developed.

This thesis presents in part the realization that continuous systems based on theories and principles can be applied to digital hardware. However, a new class of problems emerges that takes the form of "noises" which do not appear in analog systems. Therefore, the analysis and the approximations used include some theories that are not found in the classical literature.

The basic problem when realizing a totally digital system is the limited processing time available between samples of the input signal. In an analog system, the addition of two voltages is the summation of electrons in a conductor which is performed near the speed of light. However, in digital hardware, the addition of two numbers is a numerical process which uses algorithms employing logic gates having finite propagation delays. Although there exists standard methods of performing digital numerical calculations, special purpose computers employ devices such as read-only-memories (ROM's) to decrease processing time by orders of magnitude. Any subsequent algorithms that decrease processing time are sought so that feasibility becomes apparent for a real-time process.

The first system considered in this thesis is a source encoding technique called delta modulation. The system is derived by successive approximations of an optimum scheme previously proposed [1-2]. Without these approximations, a realizable real-time computer is unfeasible regardless of the complexity to which one is willing to be subjected as shown in Chapter 3.

The disadvantage of delta modulation is, in general, the limited dynamic range of an input signal to produce a suitable output signal-to-noise ratio. Therefore, dynamic range for several types of input signals is considered as a figure of merit in the experimentation. Special care is taken in the selection of algorithms to ensure that the internal system arithmetic does not limit the dynamic range.

Frequency modulated (FM) carriers are widely used as a method of information transmission. Included in this dissertation are the theoretical and experimental treatment of two methods of digitally demodulating FM signals. The first system, the Digital Discriminator, utilizes the times between zero crossings of an FM signal to obtain the output signal. Since these time intervals must be carefully measured, all algorithms are designed to insure the required accuracy. Furthermore, the output is proportional to frequency, the inverse of a time interval. A ROM is utilized here to perform rapid, real-time inversion.

The second type of FM demodulator is the Phase Locked Loop, PLL. The PLL is a nonlinear feedback system containing a phase detector (multiplier), voltage controlled oscillator (VCO) and a filter. Algorithms are designed to permit bandpass sampling and real-time phase detection. A new algorithm is also presented for the VCO. These procedures ensure real-time processing without significantly increasing the quantization noise.

When designing each of the systems described, several questions with nonunique answers are posed. The first question is: What is the format of the information and how may it best be translated into a language that can be processed by a real-time digital machine? In the delta modulator and phase locked loop the input information is chosen to be translated into digital format by means of a sampler and an analog-to-digital converter, while the discriminator uses a hard limiter to produce the binary input. All three designs must accept signals in the analog format.

A very important factor when designing digital machines is the rate of the information from the source. With the logic speeds currently available in our laboratory the processing time is sufficient for only a limited class of input signals for all of the designs considered. The logic family used in the laboratory was DTL and permitted maximum baseband frequencies of 7 kHz for the delta modulator, 5.33 kHz for the discriminator and 333 Hz

for the phase locked loop. However, logic speeds, when using ECL are three hundred times that used in the experiments. Hence, for larger input signal bandwidths, the techniques remain the same.

The next question is: How much time will it take to process the information? Unfortunately, the systems considered are sufficiently complex to require more processing time than is available between samples of the input. Hence, approximations to the theory and algorithms are required for each system designed. Some of the approximations have deterimental effects on the performance while some algorithms produce nonlinearties making the theoretical analysis difficult.

In the delta modulator an important criterion is the output rate of the processed information. The basic advantage of the scheme is the conservation of bandwidth that the system offers. Hence the output rate (bit rate) is an important parameter in the delta modulator. In the discriminator and phase locked loop, the output is filtered and an output rate greater than the Nyquist rate (twice the maximum baseband frequency) is sufficient.

Finally, one must determine the effect on the output information of internal machine errors. In any digital machine, there can only be finite word lengths. Hence, quantization noise forms during an arithmetic process within the machine. In the delta modulator, finite word length limits dynamic range while in the discriminator

and phase locked loop maximum output signal-to-noise ratio is affected. The one consolation is that these noises can be predicted in theory, and with close correlation, measured in practice.

The building blocks used in the implemented systems are described in the following chapter.

Chapter 2

THE IMPLEMENTED SYSTEMS

2.1 Basic Configuration

The systems described in the ensuing chapters of this thesis are constructed with use of general purpose DTL and TTL plug-in modules. Eight and ten bit words are combined and manipulated via "one's complement" arithmetic to perform each of the functions needed. Aside from the special purpose algorithms used in the implementation, basic building blocks consisting of adders, scalers, and integrators are constructed to synthesize the theoretical development. Since the fundamental drawbacks of real-time digital systems are the speed of processing and cost, the systems are constructed so that parallel computations are performed, and major sections are time shared. When words are processed using parallel arithmetic, combinatorial logic is used. Thus the system is operating asynchronously, the fastest possible mode of operation. Time sharing permits the use of a common section of the processing unit to be used more than once, such as adders and integrators. Time sharing is accomplished with the use of digital switches and temporary storage registers commonly termed "scratch pad memories". Figure 2-1 shows an example of a timed shared adder to facilitate a single parallel adder to be used as a three point summer i.e., to add v_a, v_b and

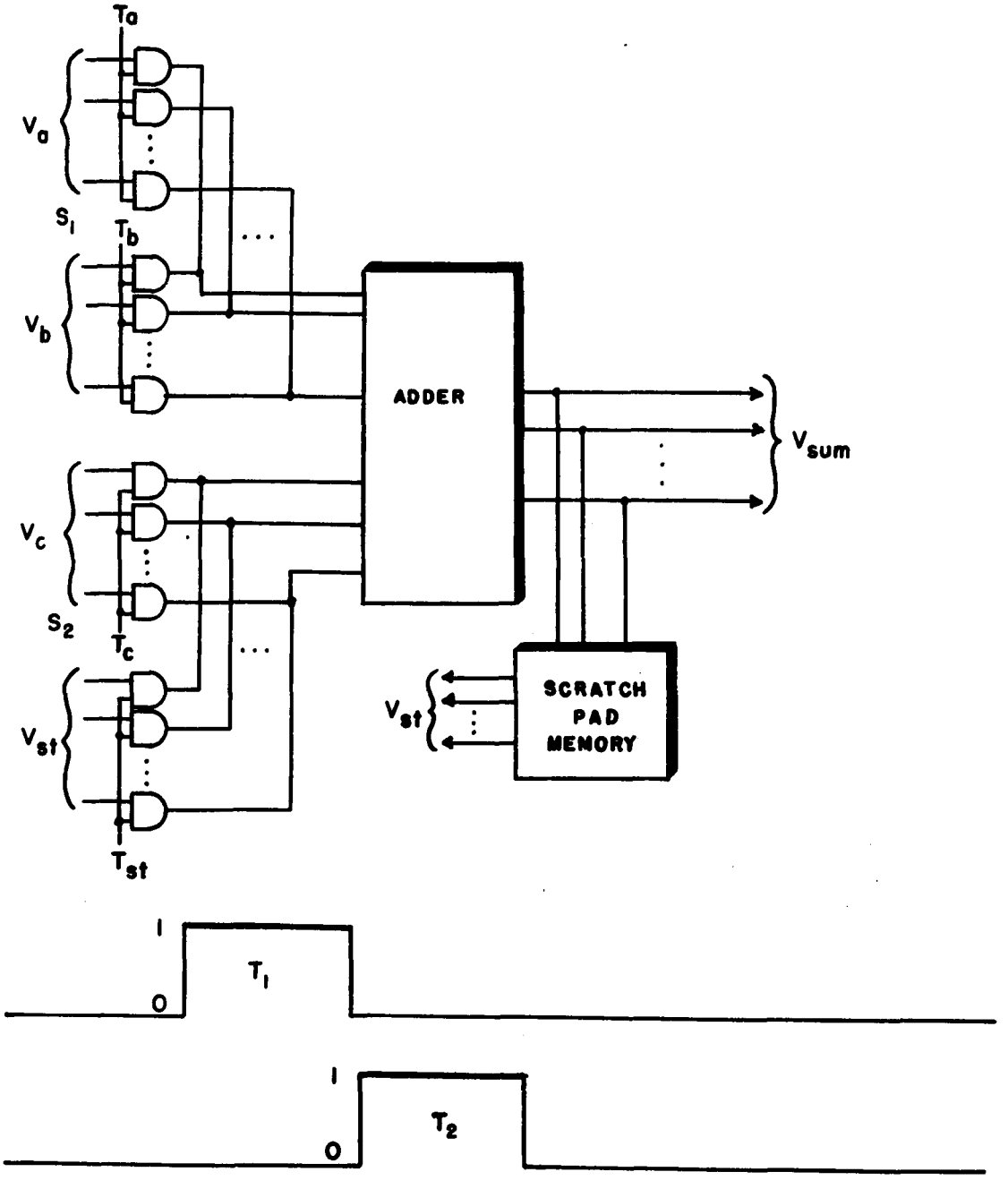


FIG. 2-1 CONFIGURATION OF A TIME SHARED ADDER

v_c simultaneously. During time period T_1, a logical 1 is sent to T_a and T_c on digital switches S_1 and S_2 allowing v_a and v_c to be added in parallel. The output of the adder is then temporarily stored in the scratch pad memory. During T_2, T_a and T_c are both at logical 0 and a logical 1 is sent to T_b and T_{st} so that the output of the adder is now $V_b + V_{st} = V_a + V_b + V_c$. The timing pulses shown in Fig. 2-1 are for a three point adder. However, it is easily seen how this process can be extended to an n point adder. Also, if the output is sent through a similar digital switch as at the input, the adder can be used to produce different sums in a different section of a system. These techniques are used in the implementation of the three described systems in this paper, so that only one adder is constructed per system; and then time shared as required.

2.2 The Adder Circuit

The adder circuit used in the implementation of the digital systems described in Chapters 3 and 5 in this thesis perform several functions other than one's-complement addition. If the number is negative and the adder becomes a subtractor, the circuit is constructed so that the sign of the result is known without special logic tests. A particular function peculiar to the

digital format is "saturation logic" and its capability in the one's-complement algorithm.

One's-complement coding is explained using the diagram shown in Fig. 2-2. Here it is seen that as the numbers continue to increase beyond the maximum, the number line folds back on itself in both the positive and negative direction. The fact that the number line traces a continuous curve is one of the advantages of digital circuitry. This can be explained by the following: Suppose over four time periods numbers are to be added into a digital integrator as shown in Fig. 2-3. If the maximum number that can be encoded is n + 2 as shown in Fig. 2-2, certainly n + 4 and n + 5 have no meaning. In an analog system where the maximum voltage in the system is (n + 2) volts, adding 3 volts still yields (n + 2) volts since the system saturates. Subsequently, when -1v and -3v are added, the result at time k + 3 is (n - 2) volts instead of the correct value of (n + 1) volts. However, in the digital system, n + 5 is encoded as +3; n + 4 as +2; and when -3 is added, the result is the correct number n + 1. The only circuitry that is needed is a storage element that flags the system when the integrator is in saturation. The flow diagram for the complete integrator with saturation logic is shown in Fig. 2-4. Referring to the diagram, the following chain of events occur: the input to the

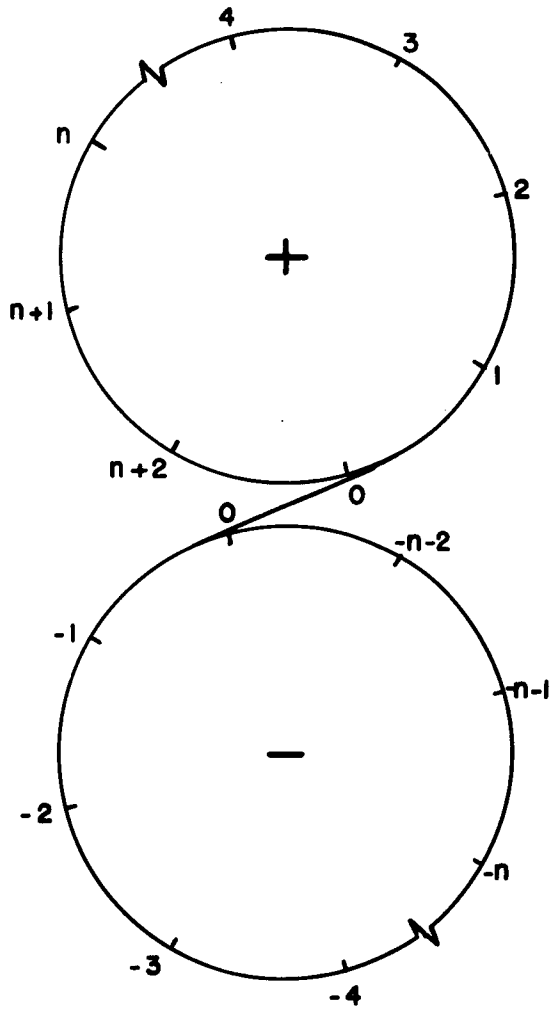
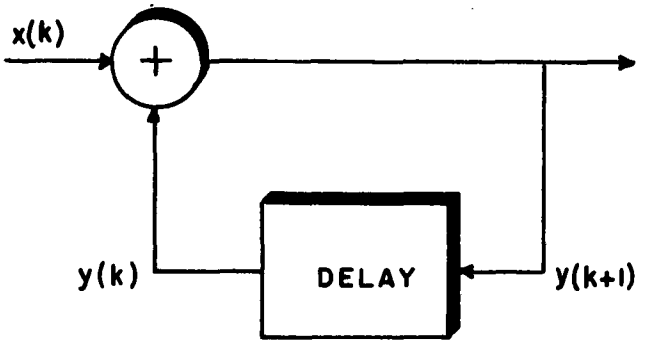


FIG. 2-2 ONE'S COMPLEMENT BINARY ARITHMETIC CODING



TIME PERIOD	INPUT x(k)	STORED NUMBER y(k)	NEW STORED NUMBER y(k+1)
k	2	n	n+2
k+1	3	n+2	n+5
k+2	-1	n+5	n+4
k+3	-3	n+4	n+1

FIG. 2-3 THE DIGITAL INTEGRATOR

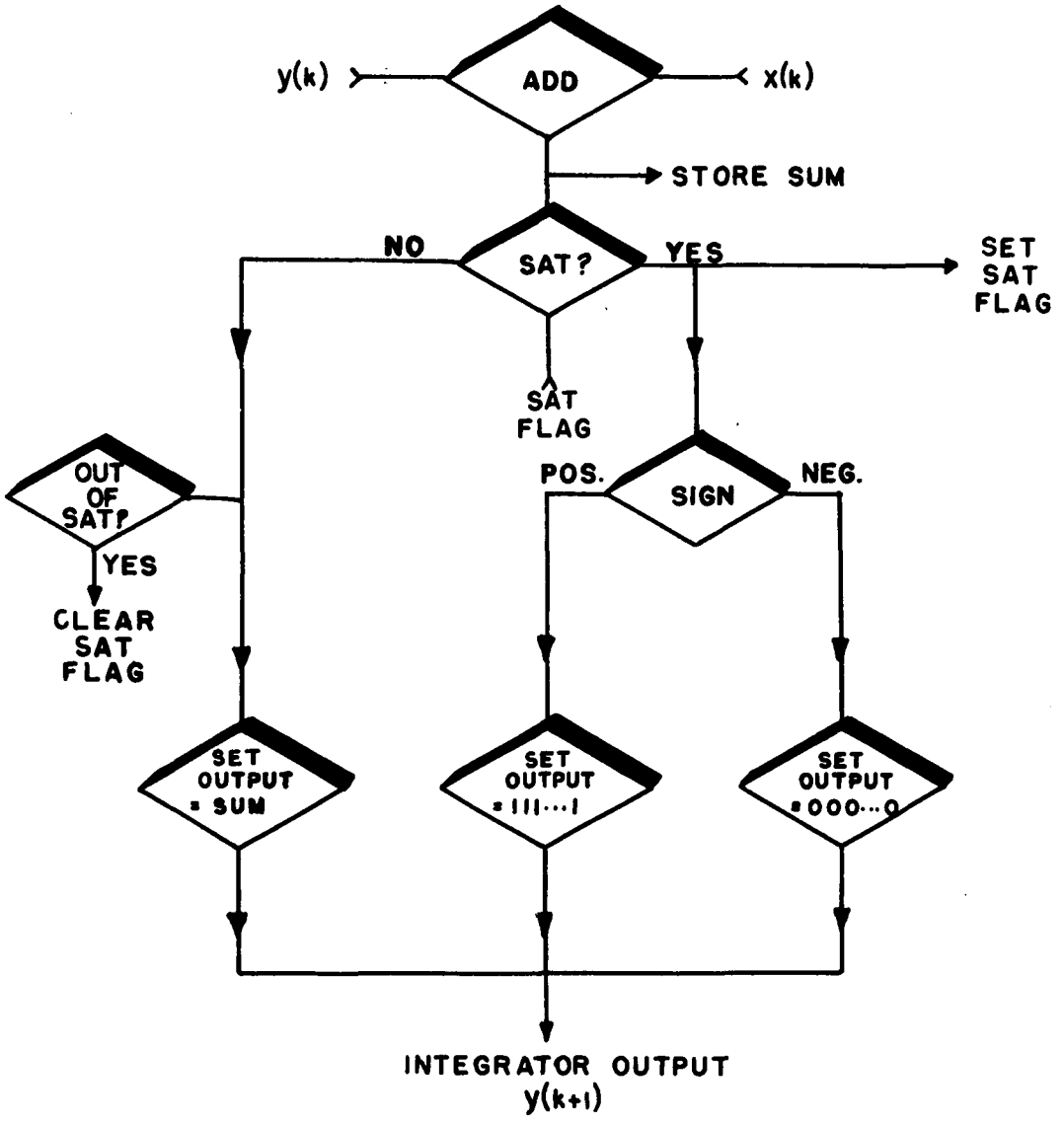


FIG. 2-4 FLOW DIAGRAM OF THE NONSATURATING INTEGRATOR

integrator, x_k, is added to the accumulated sum, y(k), and the new sum is stored. At the same time, if the input takes accumulated sum out of saturation, the saturation flag is cleared. Also, if the new sum enters saturation, the saturation flag is set and the output becomes the maximum positive or the maximum negative number depending upon the sign of the saturation number.

2.3 Analog-to-Digital, Digital-to-Analog Conversion

The input signals to the three systems described in this thesis are continuous analog waveforms. In the phase locked loop and delta modulator, the inputs are immediately converted to digital format with use of a analog-to-digital converter (A/D). The conversion time for the circuits is approximately 8 microseconds which is a moderate speed for the converters available for our laboratory [2-1] . Along with speed of conversion, A/D converters are specified by the length of the word appearing at the output at the end of the conversion. Word lengths up to 15 bits are currently available; however, fifteen bit accuracy means a converter accurate to $\pm 1/2^{15}$ or $\pm$ 0.003%. Higher resolution than $\pm$ 0.003% can not be expected even from analog circuitry. A ten bit A/D converter provides accuracy of 0.1% which proves sufficient for the work performed in the implementation of the described designs.

To best approximate impulse sampling, the A/D converter is preceded by a sample-and-hold amplifier which on command supplies the A/D with a constant amplitude signal during the conversion cycle. The sampling signal, although not an impulse, has an ambiguity window of less than 5 nanoseconds [2-2] which is sufficient for the work performed.

All three systems designed in this paper use digital-to-analog converters (D/A) to transform the digital words into an analog format. The D/A output contains a signal that has a periodic spectrum introduced by the sampling process. This output is invariably passed through a low-pass filter where the message signal is derived. The critical specification involving the D/A converter is the rate of change of the output for an applied sample-to-sample input. This parameter is commonly called the "slew rate", and for the systems involved, the D/A converters have slew rates greater than 5 volts/μsec. Since the sampling rates of the designed communication systems are less than 50 kHz (1/20 μsec), and the voltage never exceeds ± 5 volts, a slew rate of 5 volts/ μsec. adequately fills the specification.

2.4 Timing

The Digital Phase Locked Loop and Digital Delta Modulator contain internal clock pulse sources that synchronize each arithmetic task that is performed during

a sampling interval. The signals that are delivered to the digital switches, memories, and interconnected combinatorial networks, are derived from clocked sequential networks fed by the common clock source.

Consider the generation of the signal that starts the conversion process in the A/D converter. According to the specification of the A/D converter, the signal that initiates the conversion (START A/D) is to be a positive pulse with a 1 μsec. duration. Suppose the master clock in the system has a frequency of 1 MHz and a sampling rate of 50 kHz is desired. (This example is applied to the design of the phase locked loop.) The timing pulse, START A/D is derived by delivering the master clock (1 MHz) to five flip-flops interconnected to divide any input frequency by 20. Figure 2-5 shows the interconnection and the waveforms appearing at the flip-flops output. Combining outputs, Q_1 , Q_4, and Q_5 with a NAND gate and then inverting, as in Fig. 2-6, the signal START A/D is formed. Using similar techniques, all timing pulses required to produce the sequential operations are developed.

The Digital Discriminator derives the timing pulses from the incoming carrier frequency which makes the Discriminator different from the Phase Locked Loop and Delta Modulator in that the Discriminator is not an autonomous sequential system. However, the techniques of

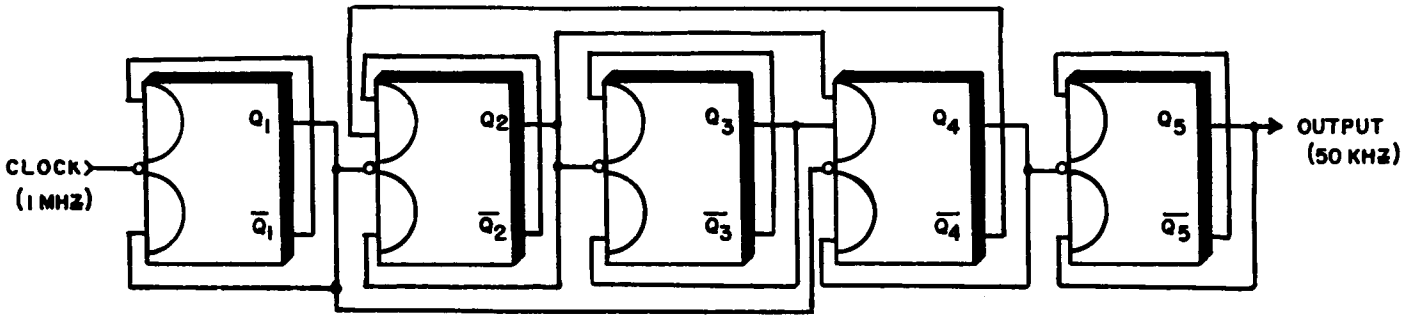


FIG 2-5 INTERCONNECTION OF MASTER-SLAVE FLIP-FLOPS TO PRODUCE A 20:1 FREQUENCY DIVISION

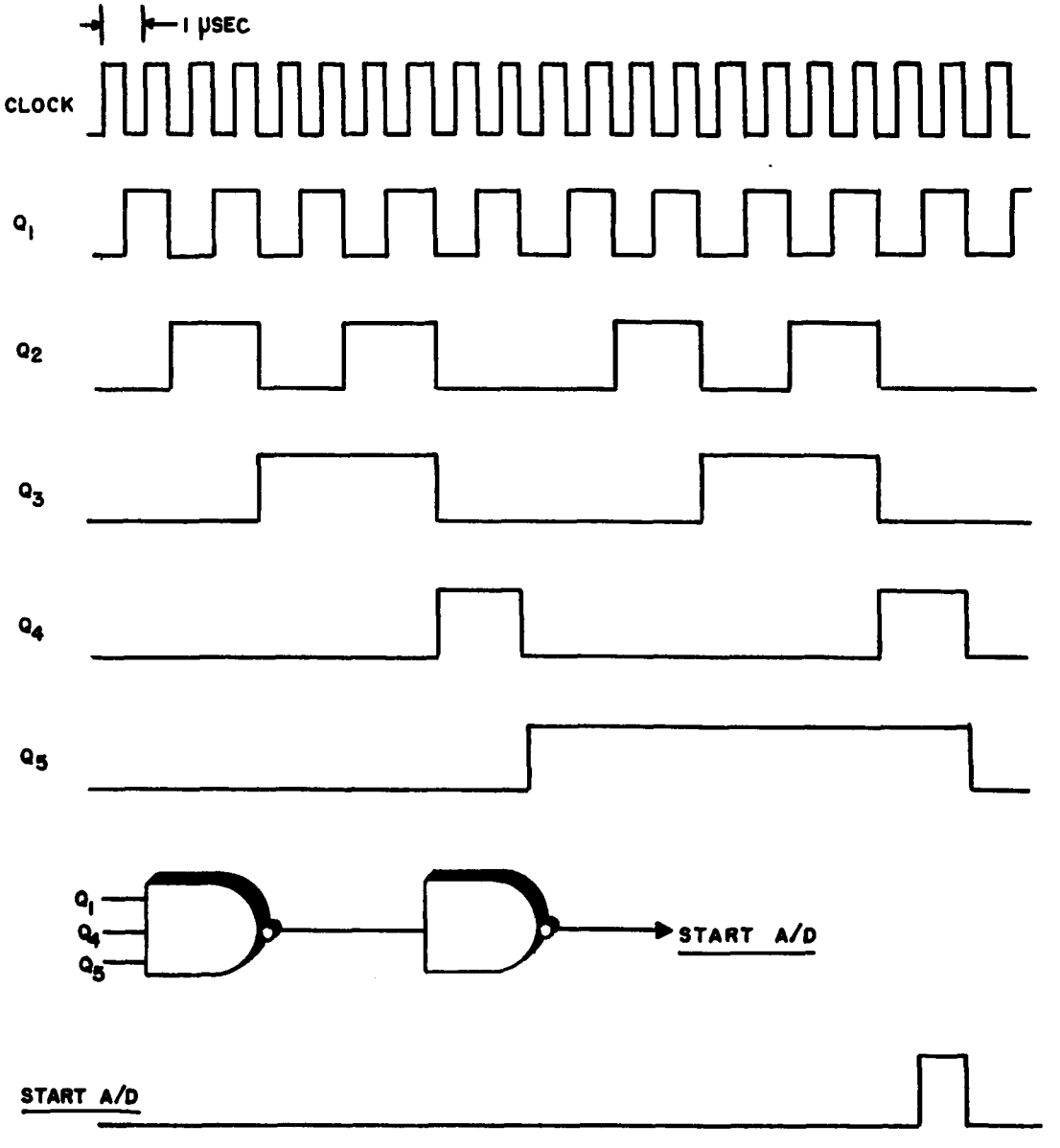


FIG. 2-6 GENERATION OF THE START A/D PULSE

frequency division and timing derivation are the same and are shown in Chapter 4.

Chapter 3

DIGITAL ADAPTIVE DELTA MODULATION

3.1 Linear Delta Modulation

Delta modulation is a source encoding technique by which information in analog format is converted into a one bit digital code. A block diagram of the linear delta modulator is shown in Fig. 3-1. The input signal $x(t)$, is compared to the estimate, $\hat{x}(t)$. If $x(t)$ is larger than $\hat{x}(t)$, a positive bit is transmitted and sent to the feedback integrator as a pulse with an appropriate scale factor. Conversely, if $x(t)$ is less than $\hat{x}(t)$ a negative bit is transmitted and fed to the integrator. The decoding scheme is the same as the feedback network, in this case an integrator. Values for $x(t)$, $x(kT)$, and $\hat{x}(t)$ are plotted versus time in Fig. 3-2 showing how $\hat{x}(t)$ approximates the input signal. Also shown are the transmitted data, e_k.

The digital system that performs the delta modulation encoding algorthm is shown in block diagram form in Fig. 3-3. It is seen that the input is first converted to digital form via a sample-and-hold amplifier followed by an analog-to-digital converter. Once in digital form the input, $x(k)$ is subtracted from the estimate, $\hat{x}(k-1)$, using a one's-complement subtractor. The

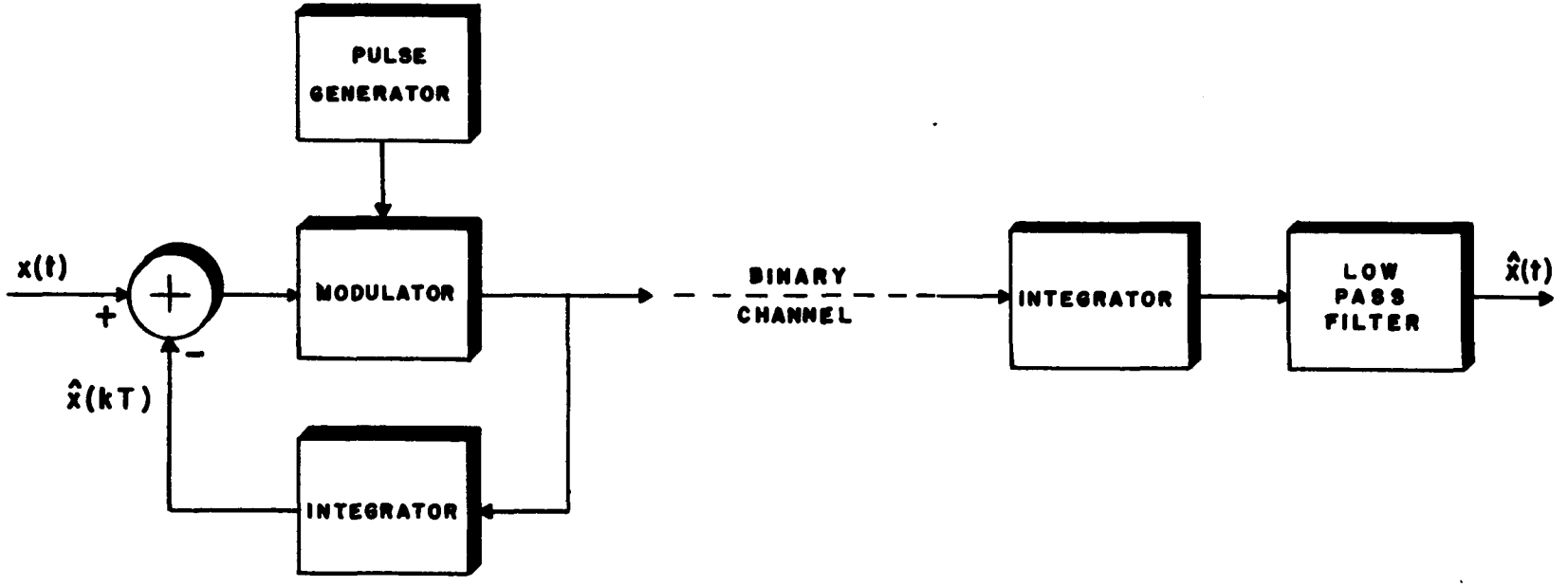


FIG. 3-1 BLOCK DIAGRAM OF THE LINEAR DELTA MODULATOR

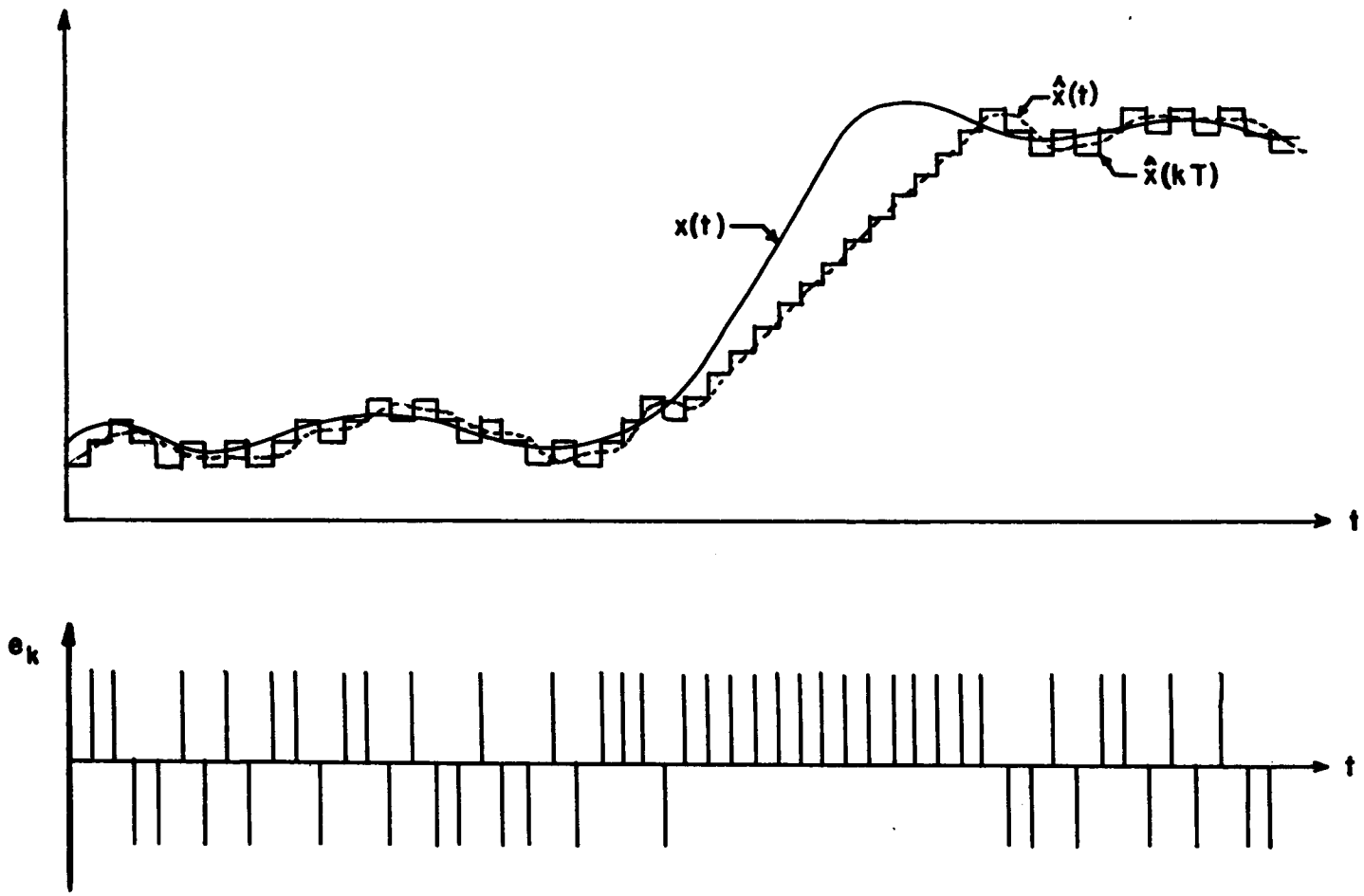


FIG. 3-2 WAVEFORMS IN THE LINEAR DELTA MODULATOR

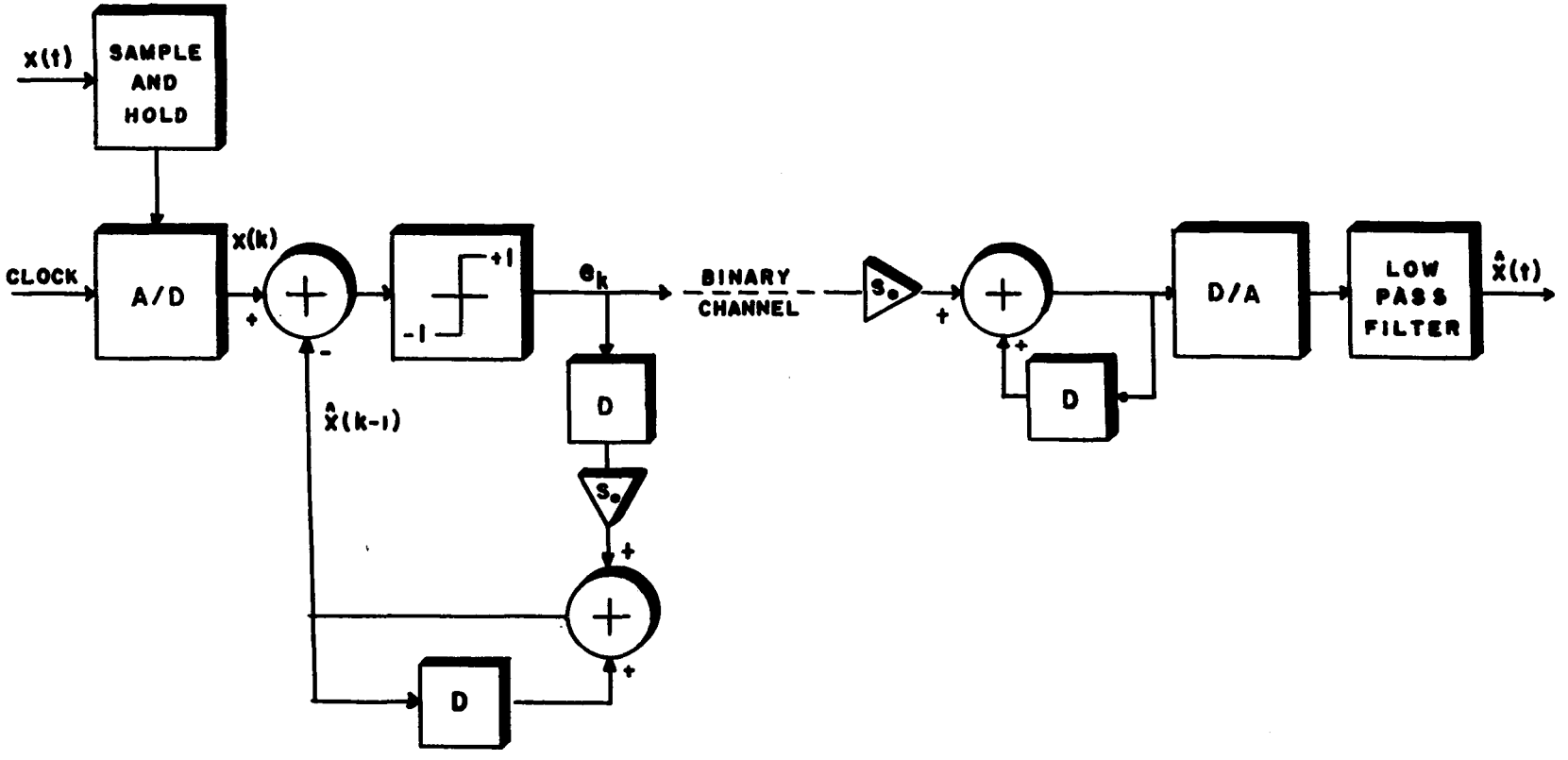


FIG. 3-3 BLOCK DIAGRAM OF THE DIGITAL LINEAR DELTA MODULATOR

hard limiting is performed by using the sign bit at the output of the subtractor as the encoded digital signal which is fed to a one bit shift register. The integrator is replaced by a digital accumulator. The weight of the bit stored in the shift register determines the step size of the linear delta modulator. The decoder is merely a digital accumulator driving a digital-to-analog converter which in turn provides an input to a low-pass filter where the final output is derived.

The implementation is further explained with the use of the timing diagram shown in Fig. 3-4. Here we see tha A/D conversion process beginning on the signal START A/D. During the conversion time, the integrator is updated using the previous output bit e_{k-1}. If e_{k-1} is a positive pulse, the integrator output increases by the step size s_o. If e_{k-1} is negative, the integrator output decreases by the step size s_o. The output of the integrator after the update is $\hat{x}(k-1)$. When the A/D conversion is completed, the A/D output, $x(k)$ is compared with the newly formed $\hat{x}(k-1)$ and the output data, e_k, are stored and transmitted. The process is repeated every T seconds (T = 20 μsec. in Fig. 3-4).

The experimental results obtained using this linear delta modulator are discussed at the end of this chapter.

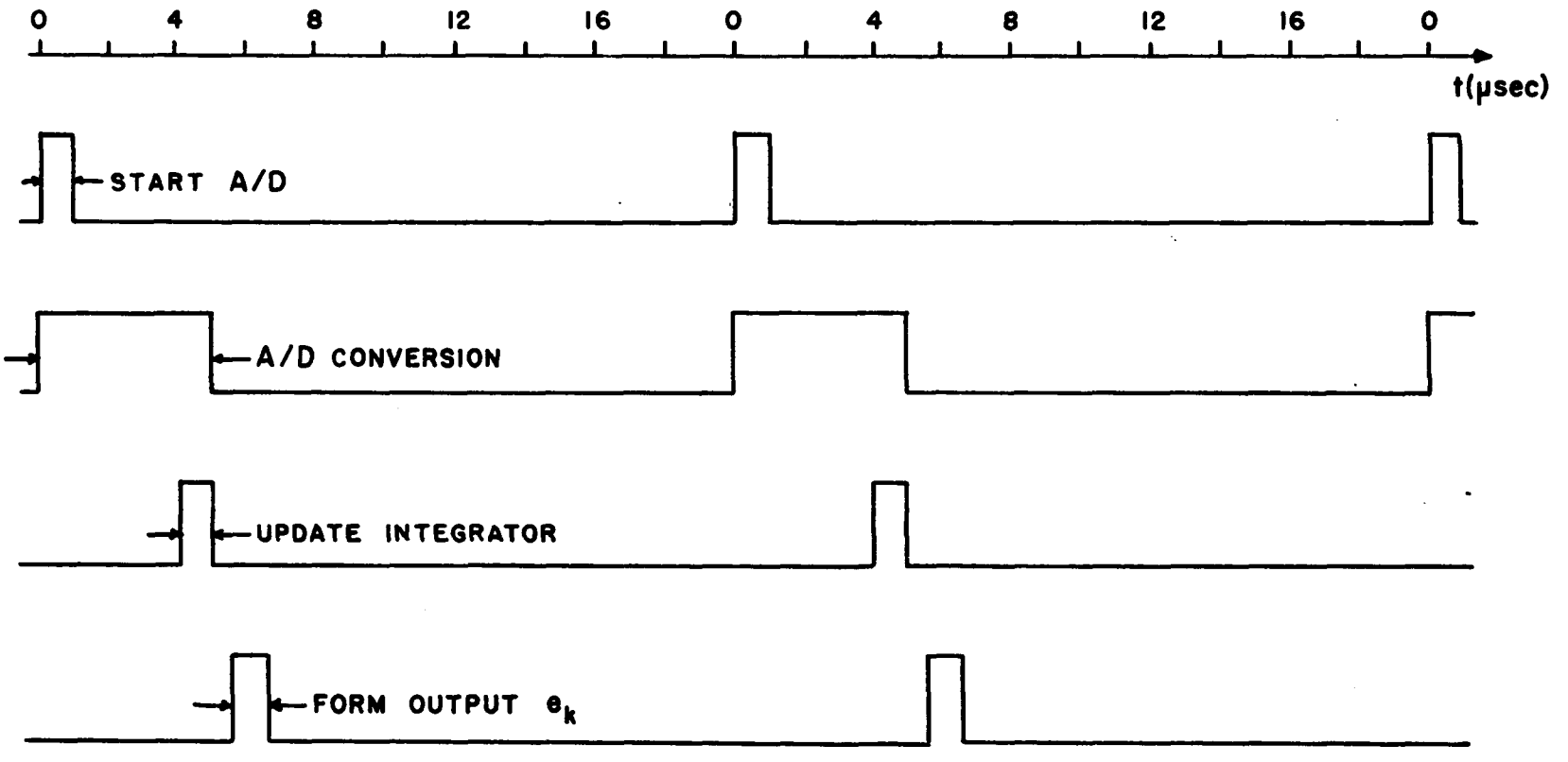


FIG. 3-4 TIMING DIAGRAM FOR THE DIGITAL LINEAR DELTA MODULATOR

3.2 Limitations Due to Fixed Step Size

Two types of signal deterioration are immediately apparent when observing the signal estimate in Fig. 3-2. Consider the case where the input signal, $x(t)$ is small compared to the step size that feeds the feedback integrator. The signal $\hat{x}(t)$ is then a poor estimate of the input signal, being either too high or too low in amplitude. The noise associated with this type of behavior is commonly termed quantization or granular noise. Ideally it is desired to have the step size as small as possible to reduce the effects of the distortion due to quantization. This results in an increase in another type of noise termed slope overload. This noise occurs when the input signal changes rapidly compared to the integration of the constant step size fed to the integrator; i.e.,

$$T\left|\dot{x}(t)\right| > \left|\hat{x}(t) - \hat{x}(t-T)\right| = s_o \text{ (step size)} \qquad (3.1)$$

Therefore, it is seen that an optimum point with respect to input signal power exists. A curve of output signal-to-noise ratio (SNR) versus relative input signal power is shown in Fig. 3-5 [3-1]. Note that the curve slopes downward for low input signal power due to quantization noise and also slopes downward for high signal power due to slope overload noise. In practice, where the desired system is to operate over a wide dynamic range, slope overload and granular noises severely

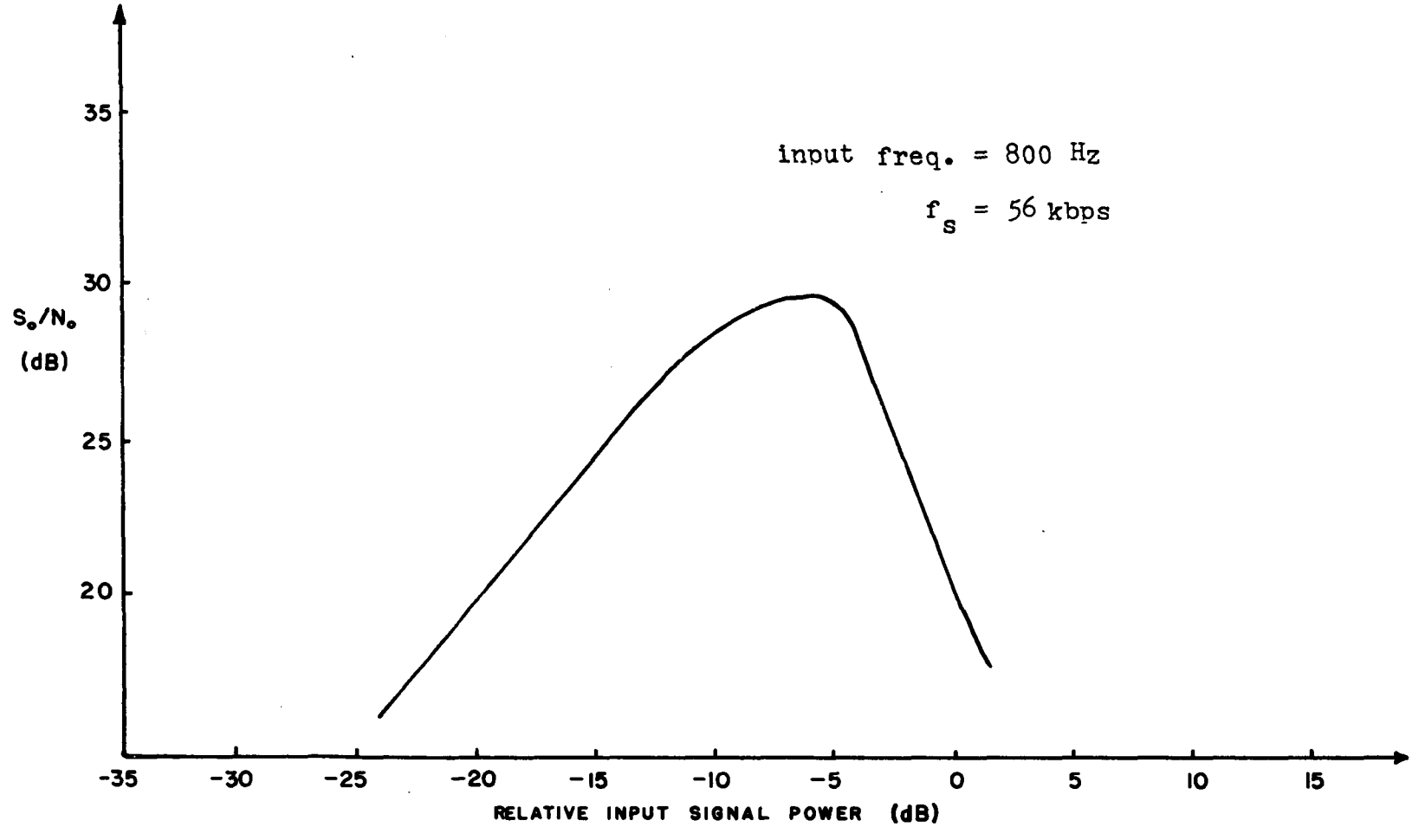


FIG. 3-5 OUTPUT SIGNAL-TO-NOISE RATIO VERSUS INPUT SIGNAL POWER FOR LINEAR DELTA MODULATION

limit the usefulness of the linear delta modulation scheme.

3.3 Digital Adaptive Delta Modulation

Several adaptive delta modulation schemes have been developed in the recent past. They were designed to increase the dynamic range by subduing the detrimental characteristics discussed in the previous sections. Almost invariably, these adaptive schemes were developed through experimentation and the design procedure was at most empirical [3-2], [3-3], [3-4], [3-5], and [3-6]. An optimum adaptive scheme, in the least mean square error sense, has been developed by Song [3-7]. In this system the output signal-to-noise ratio is constant over any given range of input signal power. The optimization procedure assumes a stationary Markov, gaussian amplitude distributed source which is a good model for many types of input signals. The equation for the assumed stationary Markov input is

$$s_k = \rho\, s_{k-1} + \lambda_{k-1} \qquad (3.2)$$

where ρ is a constant and each λ_{k-1} is uncorrelated, normal, zero mean, with standard deviation σ_λ. A block diagram of the Song system is shown in Fig. 3-6 where s_k is the signal input, e_k is the transmitted coded output, x_k is the predicted signal and r_k is the estimated signal.

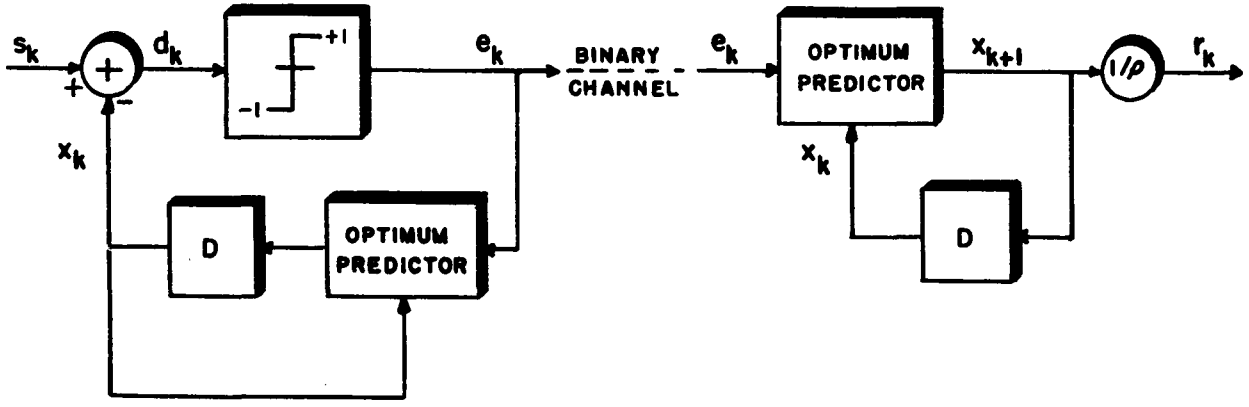


FIG. 3-6 THE SONG ADAPTIVE DELTA MODULATOR

Song developed equations for a system that depended upon the two past encoded outputs, e_k and e_{k-1}. The results for the output are given below:

$$r_k = \begin{cases} \dfrac{\int_{-\infty}^{x_{k-1}} \left[\rho\, q'(z_{k-1})\, s_{k-1} + \dfrac{\sigma_{\lambda_{k-1}}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} z^2_{k-1}\right) \right] P(s_{k-1})\, ds_{k-1}}{\int_{-\infty}^{x_{k-1}} q'(z_{k-1})\, P(s_{k-1})\, ds_{k-1}} & \text{for } e_{k-1} = -1,\ e_k = +1 \quad (3.3a) \\ \dfrac{\int_{x_{k-1}}^{\infty} \left[\rho\, q'(z_{k-1})\, s_{k-1} + \dfrac{\sigma_{\lambda_{k-1}}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} z^2_{k-1}\right) \right] P(s_{k-1})\, ds_{k-1}}{\int_{x_{k-1}}^{\infty} q'(z_{k-1})\, P(s_{k-1})\, ds_{k-1}} & \text{for } e_{k-1} = +1,\ e_k = +1 \quad (3.3b) \\ \dfrac{\int_{x_{k-1}}^{\infty} \left[\rho\, s_{k-1}\, q(z_{k-1}) - \dfrac{\sigma_{\lambda_{k-1}}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} z^2_{k-1}\right) \right] P(s_{k-1})\, ds_{k-1}}{\int_{x_{k-1}}^{\infty} q(z_{k-1})\, P(s_{k-1})\, ds_{k-1}} & \text{for } e_{k-1} = +1,\ e_k = -1 \quad (3.3c) \\ \dfrac{\int_{-\infty}^{x_{k-1}} \left[\rho\, s_{k-1}\, q(z_{k-1}) - \dfrac{\sigma_{\lambda_{k-1}}}{\sqrt{2\pi}} \exp\left(-\frac{1}{2} z^2_{k-1}\right) \right] P(s_{k-1})\, ds_{k-1}}{\int_{-\infty}^{x_{k-1}} q(z_{k-1})\, P(s_{k-1})\, ds_{k-1}} & \text{for } e_{k-1} = -1,\ e_k = -1 \quad (3.3d) \end{cases}$$

where

$$z_{k-1} = \frac{x_k - \rho s_{k-1}}{\sigma_\lambda}$$

and

$$q'(z) = \frac{1}{\sqrt{2\pi}} \int_z^\infty \exp(-u^2/2)du$$

$$q(z) = 1 - q'(z)$$

Equation (3.3) involves integrals with x_{k-1}, a random variable, in the limits. The functional relationship between the estimator r_k, and the estimates, x_k and x_{k-1}, are not apparent by simply considering these integral relationships. Hence, (3.3) was simplified by assuming

$$q'(y) = \begin{cases} \frac{1}{2} e^{-ay^2}; & y > 0 \qquad (3.4a) \\ 1 - \frac{1}{2} e^{-ay^2}; & y < 0 \qquad (3.4b) \end{cases}$$

and

$$q(y) = 1 - q'(y)$$

The value of a which minimized the mean square error between $q'(y)$ and the approximate relation given by (3.4) is $a = 1.23$. However, the greatest simplification of (3.3) resulted when setting $a = 0.5$. Figure 3-7 shows the comparison of the approximated $q'(y)$ for $a = 0.5$ and $a = 1.23$. It is seen that (3.4) with $a = 0.5$ is a good approximation to the exact $q'(y)$. If in addition to the approximation in (3.4) the input samples are

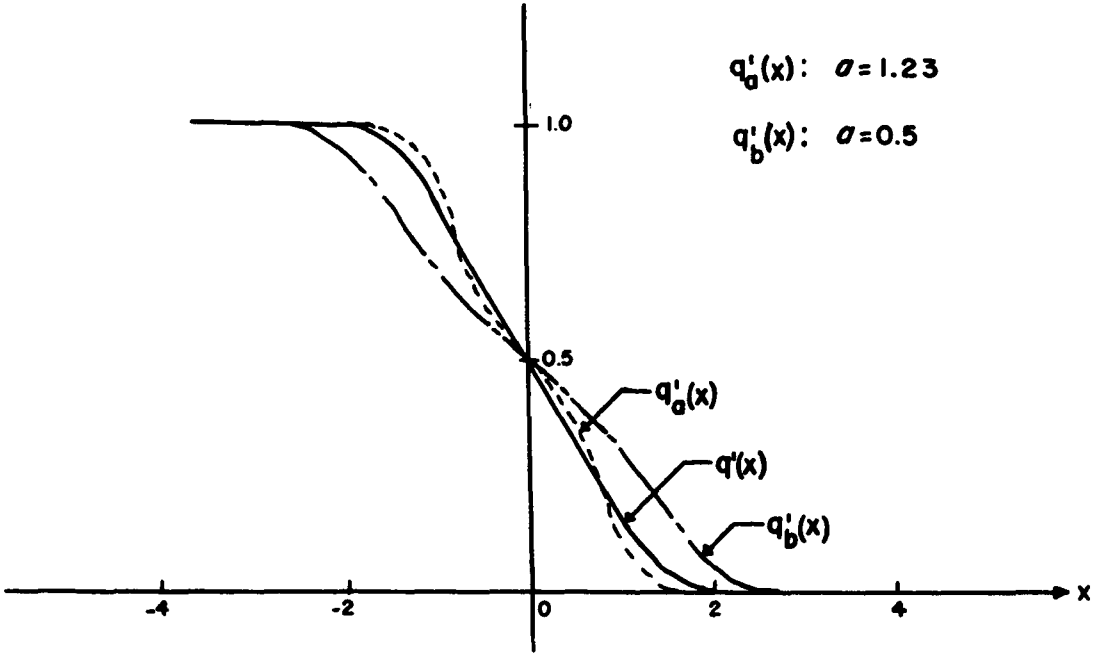


FIG. 3-7 APPROXIMATIONS TO THE q'(x) FUNCTION

highly correlated ($0.9 \leq \rho \leq 1$), (3.3) is reduced to the following set of equations:

$$r_k = \begin{cases} \frac{2}{\sqrt{2\pi}}\sigma_\lambda + x_k - \frac{\sigma_\lambda \exp(y_k^2/2)}{\sqrt{2\pi}\, q(y_k)}\ ; \\ \qquad e_{k-1} = -1,\ e_k = +1 \qquad (3.5a) \\ \frac{2}{\sqrt{2\pi}}\sigma_\lambda + x_k + \frac{\sigma_\lambda \exp(y_k^2/2)}{\sqrt{2\pi}\, q'(y_k)}\ ; \\ \qquad e_{k-1} = +1,\ e_k = +1 \qquad (3.5b) \\ -\frac{2}{\sqrt{2\pi}}\sigma_\lambda + x_k + \frac{\sigma_\lambda \exp(y_k^2/2)}{\sqrt{2\pi}\, q'(y_k)}\ ; \\ \qquad e_{k-1} = +1,\ e_k = -1 \qquad (3.5c) \\ -\frac{2}{\sqrt{2\pi}}\sigma_\lambda + x_k - \frac{\sigma_\lambda \exp(y_k^2/2)}{\sqrt{2\pi}\, q(y_k)}\ ; \\ \qquad e_{k-1} = -1,\ e_k = -1 \qquad (3.5d) \end{cases}$$

where

$$y_k = \frac{\rho\, x_{k-1} - x_k}{\sigma_\lambda} \qquad (3.6)$$

The above equations represent the first approximation to the optimum delta modulation system.

By computer simulation Song found that a system governed by (3.5) would yield a constant output signal-to-noise ratio over an 80 dB range of input signal power. Also, the output signal-to-noise ratio was 3.1 dB less than the rate distortion bound for $\rho = 0.95$ and only 3.2 dB less than the rate distortion bound for $\rho = 0.9$.

To implement a real-time computer that would obey (3.5) would be an extremely difficult task since the equations include exponentials and "q" functions. Hence, Song's work was extended by undertaking several approximations to (3.5) to realize an adaptive scheme.

Since the simulated system assumed a highly correlated input ($0.9 \leq \rho \leq 1$), let $\rho = 1$. Since ρ is unknown, but close to unity, this assumption eliminates the need for estimation and scaling. With $\rho = 1$, (3.6) becomes

$$y_k = \frac{x_{k-1} - x_k}{\sigma_\lambda} \tag{3.7a}$$

where from (3.2)

$$\sigma_\lambda^2 = E\left[(s_k - \rho\, s_{k-1})^2\right] = E\left[(s_k - s_{k-1})^2\right] \tag{3.7b}$$

If the system is working properly, x_k is a close estimate of s_k for all k. Hence

$$\sigma_\lambda^2 = E\left[(x_k - x_{k-1})^2\right] \tag{3.8a}$$

Even the expected value of the squared difference, $(x_k - x_{k-1})^2$, is difficult to transform into hardware.

A first order estimate is obtained by letting

$$\sigma_\lambda^2 = (x_k - x_{k-1})^2 \qquad (3.8b)$$

Now, (3.7) simplified to

$$y_k = \text{sgn}\ (x_{k-1} - x_k) \qquad (3.8c)$$

Using the definition of q(y) and (3.8b, 3.8c), the set of complex equations (3.5 a,b,c, and d) simplify dramatically to a set of linear equations. The results are the following:

for $x_k - x_{k-1} > 0$

$$r_k = x_{k+1} = \begin{cases} x_k + 0.51\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = -1,\ e_k = +1 \qquad (3.9a) \\ x_k + 1.15\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = +1,\ e_k = +1 \qquad (3.9b) \\ x_k - 0.51\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = +1,\ e_k = -1 \qquad (3.9c) \\ x_k - 1.15\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = -1,\ e_k = -1 \qquad (3.9d) \end{cases}$$

and for $x_k - x_{k-1} < 0$

$$r_k = x_{k+1} = \begin{cases} x_k - 0.51\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = -1,\ e_k = +1 & (3.10a) \\ x_k - 1.51\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = +1,\ e_k = +1 & (3.10b) \\ x_k + .51\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = +1,\ e_k = -1 & (3.10c) \\ x_k + 1.15\,(x_k - x_{k-1})\ ; \\ \qquad e_{k-1} = -1,\ e_k = -1 & (3.10d) \end{cases}$$

To construct r_k knowing x_k, $x_k - x_{k-1}$, e_k, and e_{k-1}, it is convenient to rewrite (3.9) and (3.10) in the following form:

$$r_k = x_{k+1} = \begin{cases} x_k + 0.815|x_k - x_{k-1}| - 0.3|x_k - x_{k-1}|; \\ \qquad e_{k-1} = -1,\ e_k = +1 \qquad (3.11a) \\ x_k + 0.815|x_k - x_{k-1}| + 0.3|x_k - x_{k-1}|; \\ \qquad e_{k-1} = +1,\ e_k = +1 \qquad (3.11b) \\ x_k - 0.815|x_k - x_{k-1}| + 0.3|x_k - x_{k-1}|; \\ \qquad e_k = +1,\ e_k = -1 \qquad (3.11c) \\ x_k - 0.815|x_k - x_{k-1}| - 0.3|x_k - x_{k-1}|; \\ \qquad e_{k-1} = -1,\ e_k = -1 \qquad (3.11d) \end{cases}$$

In short form, the above can be written as

$$r_k = x_{k+1} = x_k + g_1 + g_2 \qquad (3.12)$$

where

$$g_1 = g_2\ (e_k,\ x_k - x_{k-1})$$
$$g_2 = g_2\ (e_{k-1},\ x_k - x_{k-1}) \qquad (3.13)$$

In words, the new estimate $r_k = x_{k+1}$, is equal to the old estimate, x_k, plus the outputs of the function generators, g_1 and g_2. Figure 3-8 shows the graph of the functions g_1 and g_2 described by (3.13).

Note that g_1 and g_2 approach the origin directly in proportion to $(x_k - x_{k-1})$. In a digital system, the words that are used for computations have a finite bit length. Therefore special attention is given to the functions g_1 and g_2 in the neighborhood of the origin to ensure correct operation of the delta modulator. The resulting forms for g_1 and g_2 are shown in Fig. 3-9. Here it is seen that if the step size is zero $(x_k - x_{k-1} = 0)$, then g_1 is set to $\pm$ 0.08, and g_2 is set to 0.0. At the next sampling instant, $(x_k - x_{k-1})$ is now equal to $\pm$ 0.08 and the functions g_1 and g_2 take on new values yielding a new step size that is different than the previous one. Hence, the step size changes continuously and a dead zone near the origin does not exist.

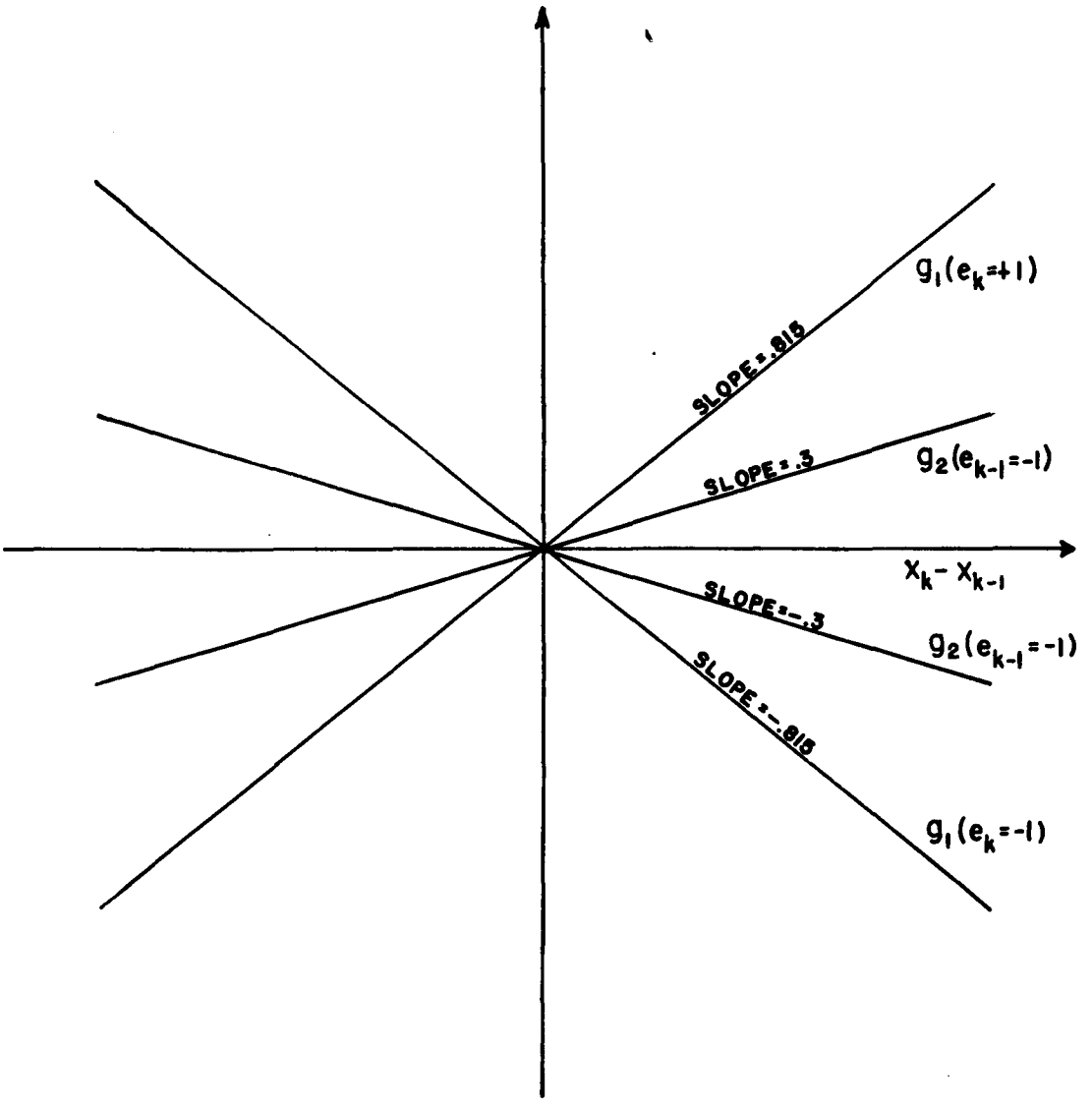


FIG. 3-8 FUNCTION GENERATORS OF THE APPROXIMATED OPTIMUM ADAPTIVE DELTA MODULATOR

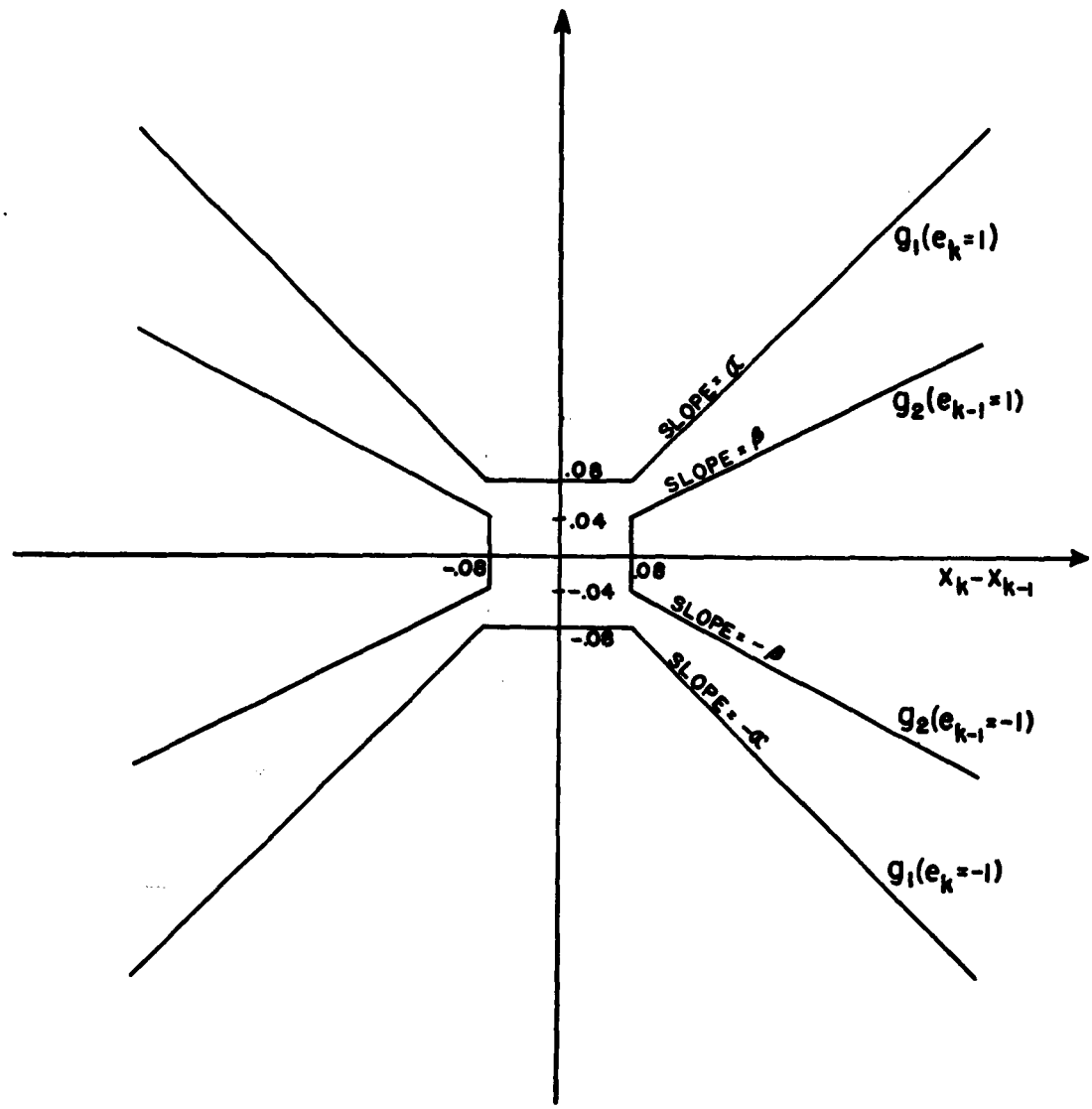


FIG. 3-9 FUNCTION GENERATORS OF THE APPROXIMATED OPTIMUM SCHEME MODIFIED TO ACCOUNT FOR FINITE WORD LENGTH

Since equations developed for the functions g_1 and g_2 were based on numerous approximations to an optimum encoder-decoder, the slopes of g_1 and g_2 are labeled α and β respectively to add a degree of freedom to the system during experimentation. The resulting equations for g_1 and g_2 reflected by Fig. 3-9 are:

for $x_k - x_{k-1} > 0$

$$g_1(e_k = +1) = .08 + \alpha(x_k - x_{k-1} - .08)\ U\ (x_k - x_{k-1} - .08) \tag{3.14a}$$

$$g_1(e_k = -1) = -.08 - \alpha(x_k - x_{k-1} - .08)\ U\ (x_k - x_{k-1} - .08) \tag{3.14b}$$

$$g_2(e_{k-1} = +1) = \left[.04 + \beta(x_k - x_{k-1} - .08)\right]\ U\ (x_k - x_{k-1} - .08) \tag{3.14c}$$

$$g_1(e_{k-1} = -1) = -\left[.04 + \beta\ (x_k - x_{k-1} - .08)\right]\ U\ (x_k - x_{k-1} - .08) \tag{3.14d}$$

and for $x_k - x_{k-1} < 0$

$$g_1(e_k = +1) = .08 - \alpha(x_k - x_{k-1} + .08)\ U\ (-\left[x_k - x_{k-1}\right] - .08) \tag{3.15a}$$

$$g_1(e_k = -1) = -.08 + \alpha\ (x_k - x_{k-1} + .08)\ U\ (-\left[x_k - x_{k-1}\right] - .08) \tag{3.15b}$$

$$g_2(e_{k-1} = +1) = \left[.04 - \beta\ (x_k - x_{k-1} + .08)\right]\ U\ (-\left[x_k - x_{k-1}\right] - .08) \tag{3.15c}$$

$$g_2(e_{k-1} = -1) = -\left[.04 - \beta\ (x_k - x_{k-1} + .08)\right] U\ (-\left[x_k - x_{k-1}\right] - .08) \tag{3.15d}$$

where

$$U(z) = \begin{cases} 1 & z \geq 0 \\ 0 & z < 0 \end{cases} \tag{3.16}$$

The numbers 0.04 and 0.08 are derived assuming that the system utilizes an eight bit A/D converter

and eight bit internal arithmetic where the maximum value for a digital word corresponds to $\pm$ 5 volts. Therefore, the smallest quantization level and hence the minimum step size becomes the ratio of the total voltage excursion (10 volts) over the total number of quantization levels (2^8); viz.,

$$\frac{10 \text{ volts}}{2^8 \text{ levels}} = 0.04 \text{ volts/quantization level}$$

The final form of the delta modulator is shown in block diagram form in Fig. 3-10. Here it is seen that the functions of g_1 and g_2 define the step size that is fed to the digital integrator. One two input adder is time shared (as described in Chapter 2) to produce all the addition computations needed.

The system was tested for various types of input signals and varying input signal power. The results are described in the next section.

3.4 Experimental Results

The slopes of the functions of g_1 and g_2 can take on any value with the use of a read-only memory (ROM). However, the unavailability of a ROM in the laboratory restricted the slopes α and β to be powers of 2; i.e., 1/8, 1/4, 1/2, 1,2, etc. Results are obtained for $\alpha = 1, \beta = \frac{1}{2}$, and for $\alpha = 1$, $\beta = 0$ since these slopes are the closest to the values obtained in (3.11)(.815 and .3) and also yield the best performance experimentally. The limited slopes available are demonstrated to be sufficient.

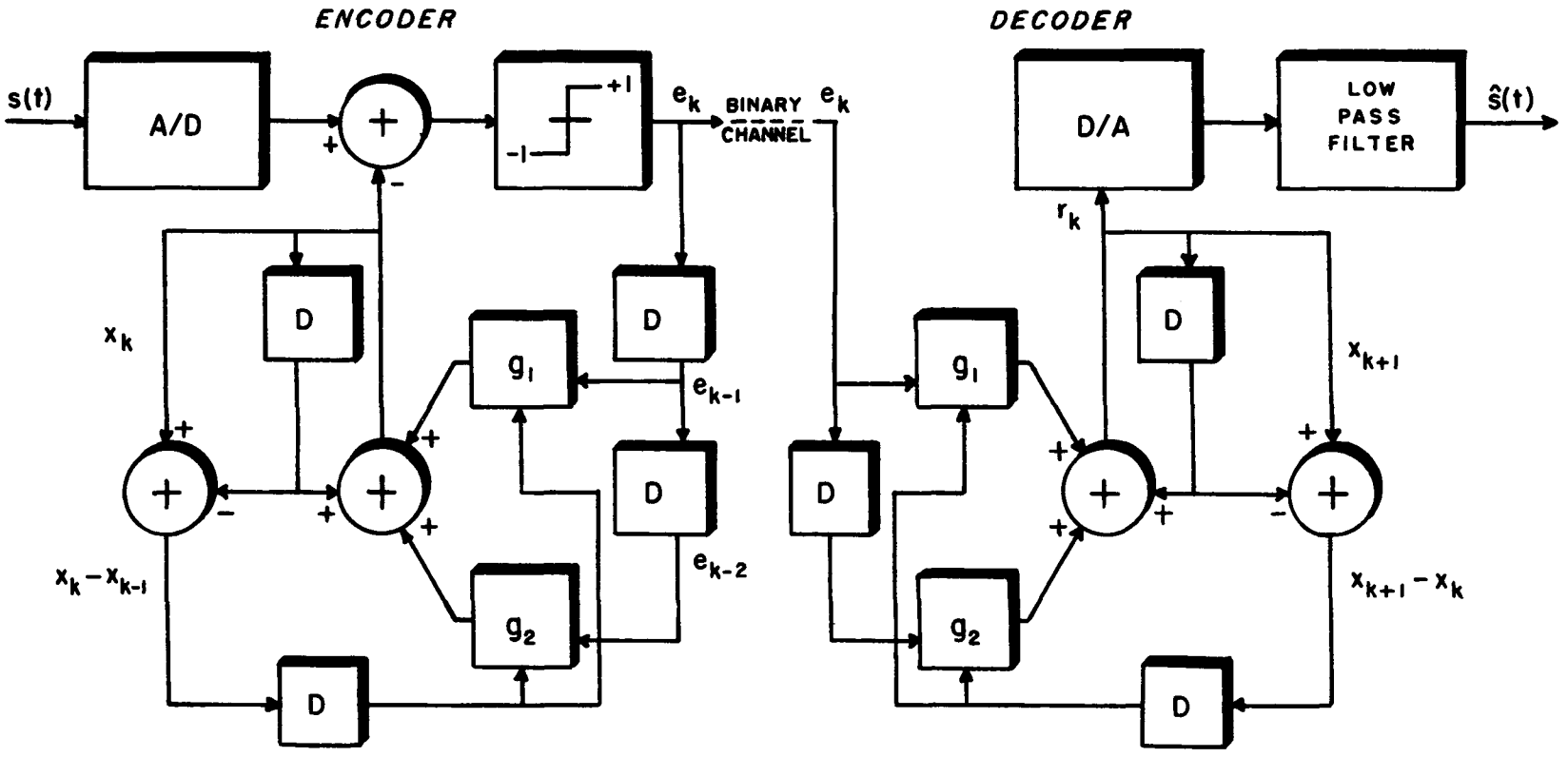


FIG. 3-10 BLOCK DIAGRAM OF THE IMPLEMENTED ADAPTIVE DELTA MODULATOR

The system described by Fig. 3-10 was simulated on a computer for a Markov source with $\rho = 0.9$ and $\rho = 0.95$, $\alpha = 1$, and $\beta = 0$. The results, shown in Fig. 3-11, display the increased dynamic range and flat response of the delta modulation system. A minimum value of 0.08v was used in the simulation hence the output signal-to-noise ratio drops for low input signal power. The performance of the actual real-time system is demonstrated in the following sections.

3.4.1 Description of the Test Facility

Experimental results are obtained using the test facility shown in Fig. 3-12. Referring to the figure, the input message signal is passed directly to the delta modulator while being monitored for input signal power. The output of the modulator is the signal estimate $\hat{x}(kT)$. This output is filtered and measured for purity using a distortion analyzer when the message is a sinewave. For other types of input signals such as voice and video, subjective tests were employed.

3.4.2 Response to a Square Wave Input

The response of the adaptive delta modulation system to a 500 Hz square wave is shown in Fig. 3-13 for $\alpha = 1$, $\beta = 0.5$ and $\alpha = 1$, $\beta = 0$. Note the difference in the rise time of the two displays. It is clear from

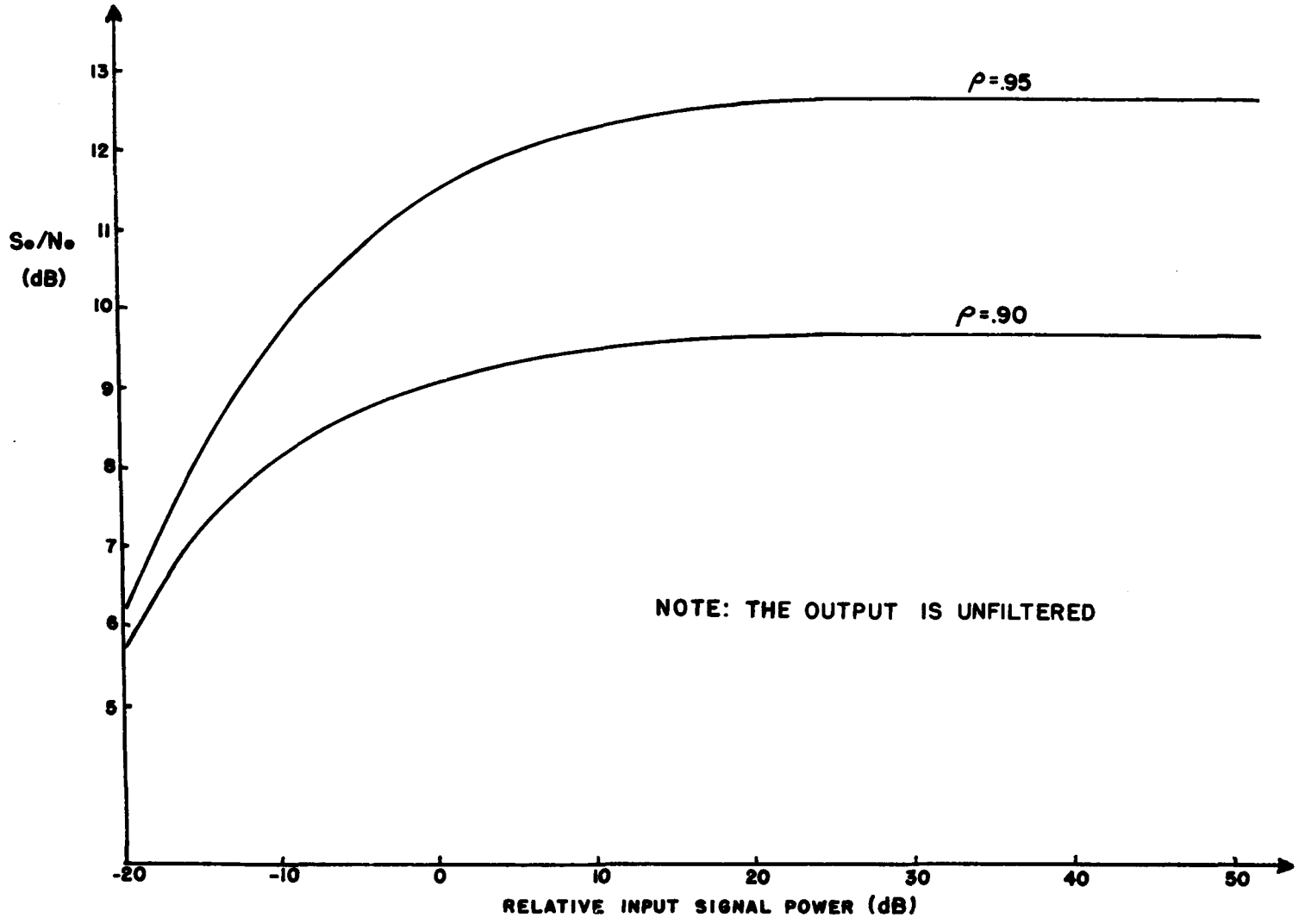


FIG. 3-11 SIMULATED PERFORMANCE OF THE 8 BIT ADAPTIVE DELTA MODULATOR

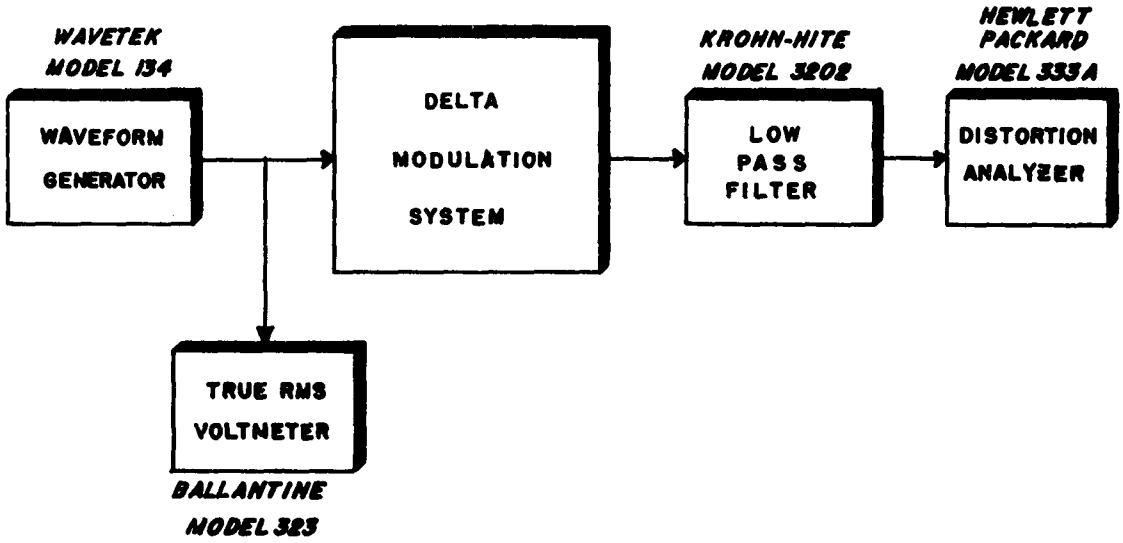
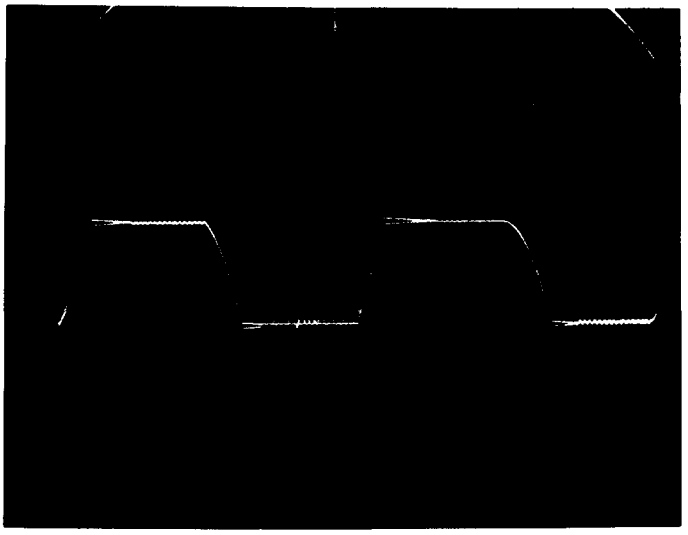


FIG. 3-12 TEST FACILITY FOR EVALUATING THE DELTA MODULATION SYSTEM

(a)

$\alpha=1, \beta=0$



(b)

$\alpha=1, \beta=0.5$

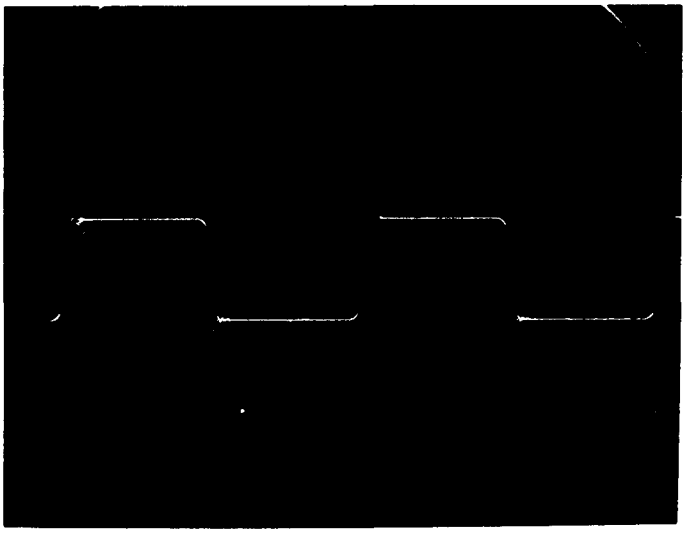


FIG. 3-13 RESPONSE OF THE DIGITAL ADAPTIVE DELTA MODULATOR TO A 500HZ SQUAREWAVE; (a) $\alpha=1, \beta=0$ (b) $\alpha=1, \beta=0.5$

the figure that for input signals with discontinuities (such as video signals), the system with $\alpha = 1, \beta = 0.5$ yields by far the best performance.

3.4.3 Response to Sinusoidal Inputs

Purity of voice signals cannot be measured directly without the use of subjective testing. However, it is generally accepted that the response of a system to an 800 Hz test tone provides a good indication of the system response to voice inputs. The linear delta modulation discussed in Section 3-1 yields a performance curve for an 800 Hz sinewave input as shown in Fig. 3-14. Note the similarity to the performance curve of the analog delta modulator shown in Fig. 3-5.

Figures 3-15 and 3-16 display the output signal-to-noise ratio vs. input signal power for the adaptive scheme with $\alpha = 1$, $\beta = 0.5$ and for $\alpha = 1$, $\beta = 0$, respectively. The $\alpha = 1$, $\beta = 0$ curve has a higher output signal-to-noise ratio but the $\alpha = 1$, $\beta = 0.5$ curve has a flatter response region. The curves with the smallest dynamic range reflect the function generators described by (3-14) and (3-15) where the minimum step size is 0.08 volts. This finite step size causes the output signal-to-noise ratio to decrease at low input signal power. The downward slope at the upper limit of the input signal power is caused by the $\pm$ 5v limitation of the A/D and D/A converters.

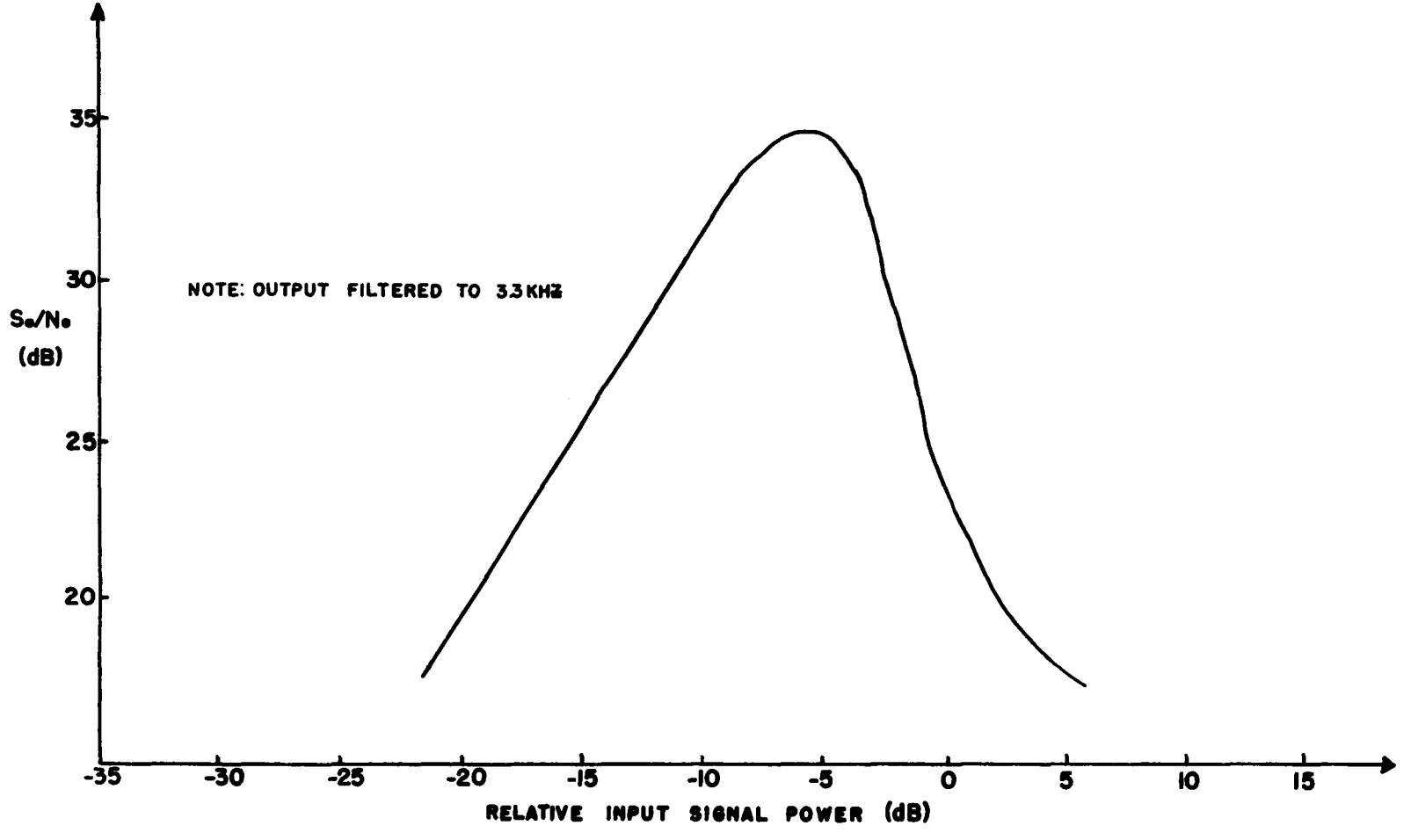


FIG. 3-14 RESPONSE OF THE LINEAR DELTA MODULATOR TO AN 800HZ SINEWAVE INPUT SHOWING THE LIMITATION OF DYNAMIC RANGE

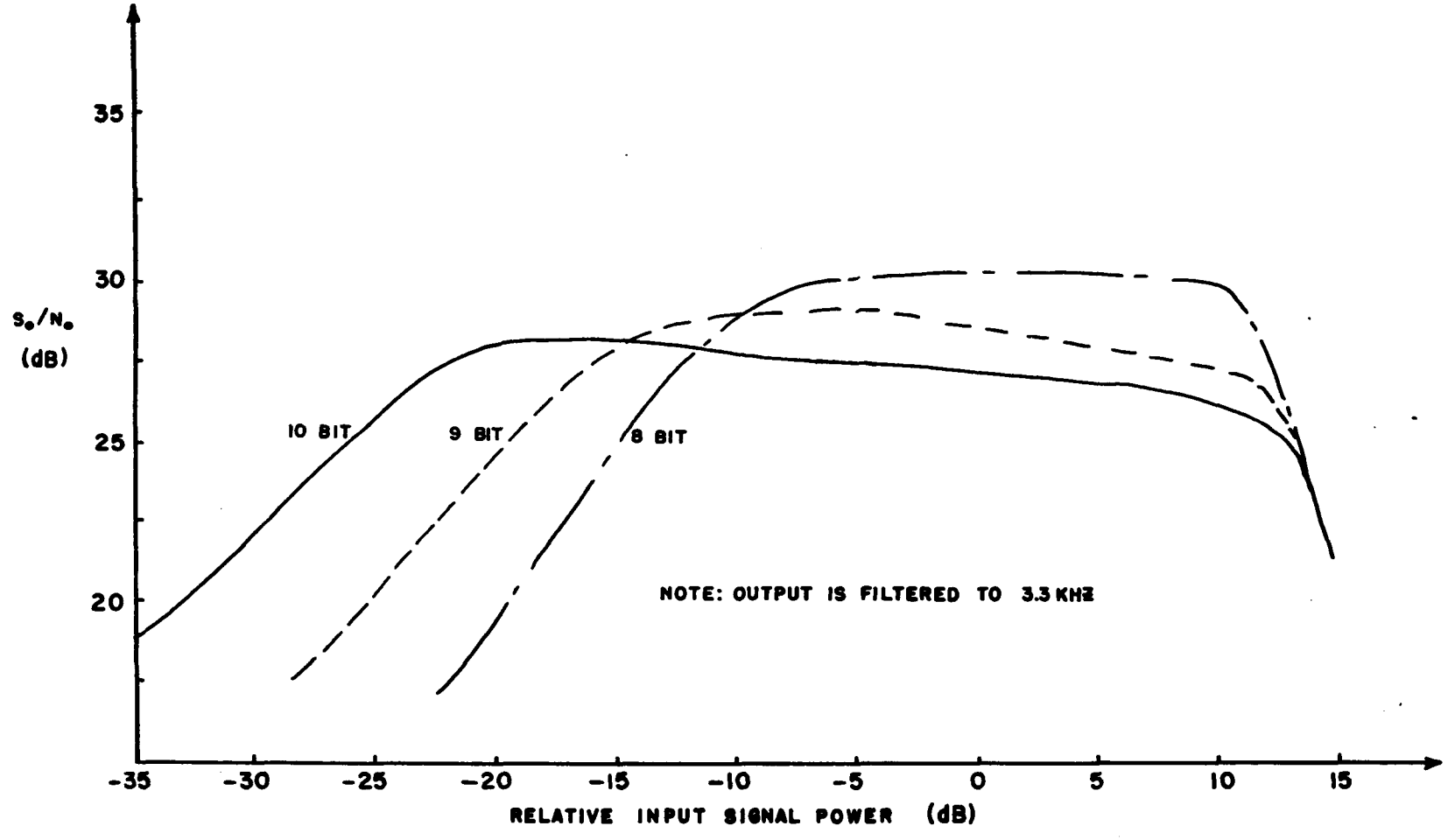


FIG. 3-15 RESPONSE OF THE DIGITAL DELTA MODULATOR TO AN 800HZ SINEWAVE ($\alpha = 1$, $\beta = 0.5$)

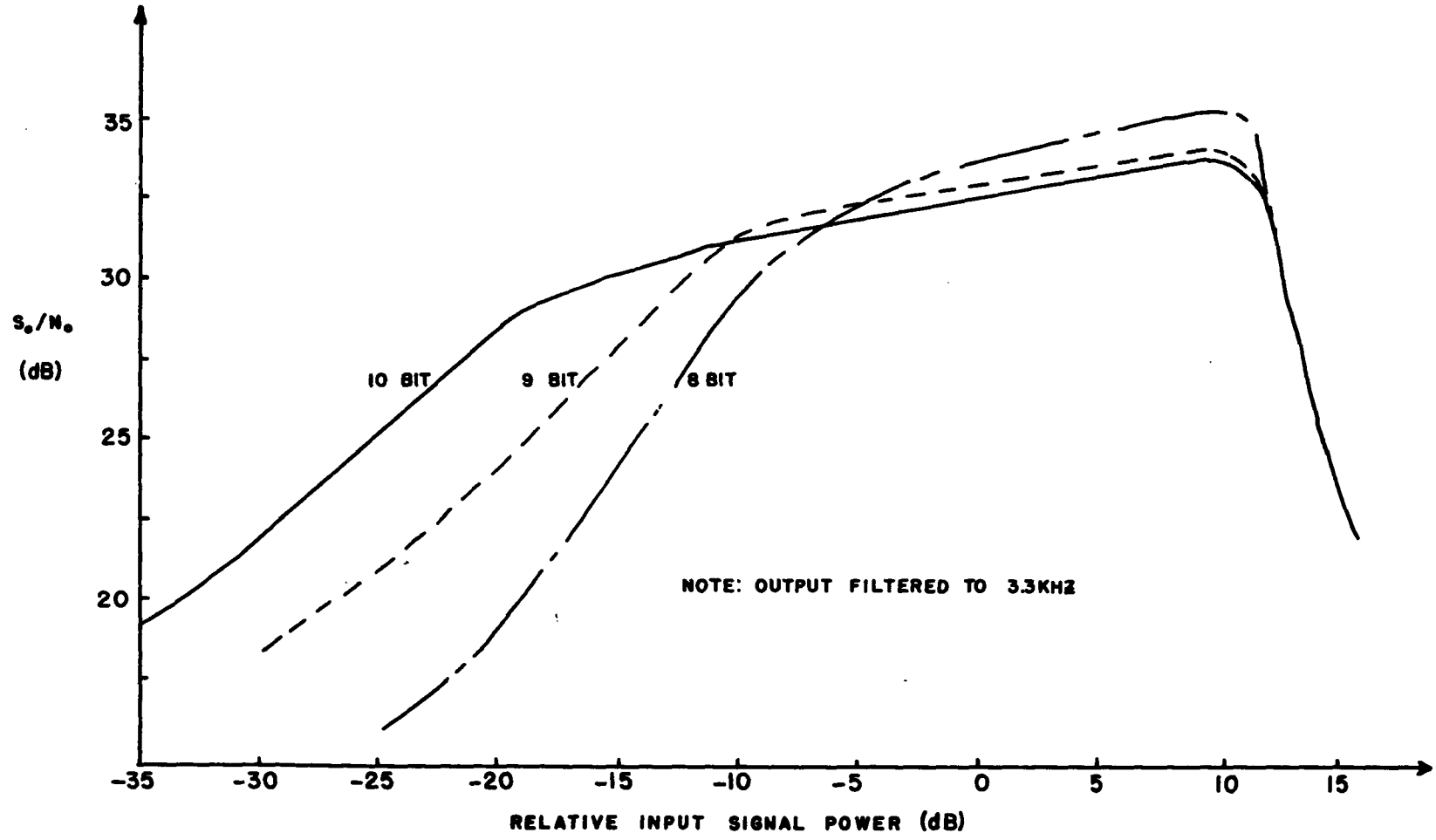


FIG. 3-16 RESPONSE OF THE DIGITAL DELTA MODULATOR TO AN 800HZ SINEWAVE ($\alpha=1, \beta=0$)

When comparing Figs. 3-15 and 3-16 with the performance curve of the linear delta modulator (Fig. 3-14), increased dynamic range becomes apparent.

To demonstrate that the dynamic range is a direct function of the number of bits used in the internal arithmetic, the word length was increased to 9 and 10 bits. This resulted in minimum step sizes of 0.04v and 0.02v respectively. The resulting performance curves in Figs. 3-15 and 3-16 reflect the increase in dynamic range made available by the increased word length (6dB per bit).

All of the above tests were performed at a bit rate of 56 kilobits/seconds and a low-pass filter cutoff of 3.3 kHz. This rate is common to the telephone binary channels used in present day equipment.

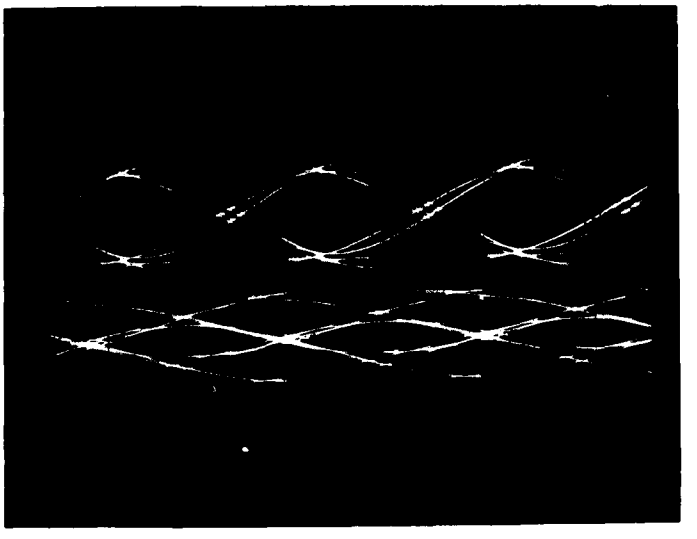
3.4.4 Response to Random Data Sequences

The oscillograms shown in Fig. 3-17 display the eye patterns of the system response to pseudo-random data sequences. The input is obtained by passing the output of a pseudo-random sequence generator through a low-pass filter. Figure 3-17a shows the eye pattern response of a linear delta modulator while Fig. 3-17b shows the eye pattern response of the adaptive delta modulator with $\alpha = 1$, $\beta = 0.5$. The results in the figure clearly show that the adaptive system has a superior ability in reconstructing data.

(a) LINEAR SCHEME

INPUT

OUTPUT



(b) ADAPTIVE SCHEME

INPUT

OUTPUT

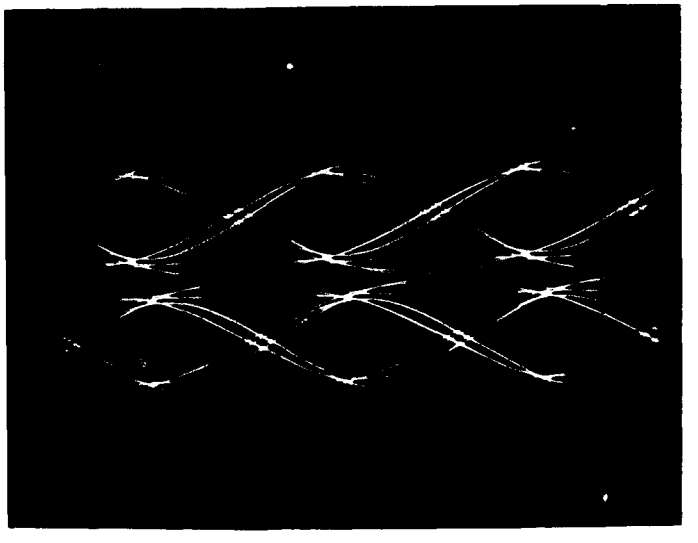


FIG. 3-17 RESPONSE TO PSEUDO-RANDOM DATA OF (a) THE LINEAR DELTA MODULATOR (b) ADAPTIVE DELTA MODULATOR ($\alpha = 1$, $\beta = 0.5$)

3.5 High Speed Digital Adaptive Delta Modulation

The adaptive delta modulation scheme described in this chapter is designed to operate at bit rates up to 56 kilobits/second to encode signals bandlimited up to 7 kHz. However, for video applications, the maximum baseband frequency is typically 1 MHz [3-8]. This baseband frequency would then require a bit rate of 8 Megabits/second which reduces processing time to about 125 nanoseconds.

Utilizing state of the art integrated circuitry, the adaptive delta modulation scheme can be used for video encoding if modifications are made in the implementation. Of course, to reduce the processing time, time shared adders can no longer be used.

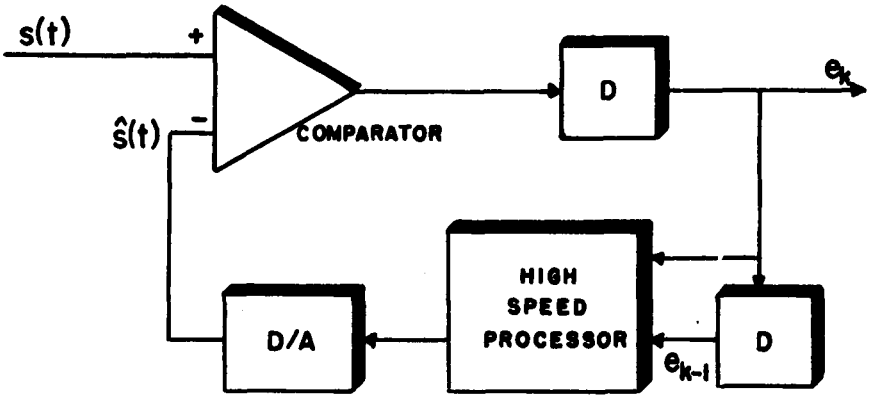
Using 270 MHz nonsaturating type logic, ECL, addition of 10 bit numbers can be performed in 5 ns. Referring to Fig. 3-10 we see that three adders are required, hence 15 ns of time. The function generators g_1 and g_2 are merely digital switches with propagations delay times of 4 ns. Since g_1 and g_2 are switched simultaneously, the resultant time remains 4 ns. The delay registers are also inserted simultaneously and add 4 ns.

The time consuming A/D converter must be replaced by an analog voltage comparator. These comparators are commercially available at suitably high switching rates.

The remaining items is a D/A converter to feed the comparator. Present day converters can change voltages in response to digital inputs in the nanosecond time region.

Consequently, the total time used for processing when utilizing high speed devices is 15 ns (for addition) + 4 ns (switching g_1 and g_2) + 4 ns (delay register propagation time) + 5 ns (D/A conversion and analog comparison) = 28 ns. With a total time available of 125 ns, the 80% remaining time can be used as guard time between operations.

A block diagram of the high speed system is shown in Fig. 3-18. Although no attempt was made to implement a high speed delta modulator in the laboratory, the feasibility is evident.



NOTE: THE COMPARATOR IS AN ANALOG DEVICE

FIG. 3-18 BLOCK DIAGRAM OF A HIGH SPEED DIGITAL ADAPTIVE DELTA MODULATOR

Chapter 4

A DIGITAL FM DISCRIMINATOR

4.1 Introduction

The theory of operation and the design of an All Digital FM Discriminator is presented in this chapter. It is shown that the digital discriminator is equivalent to the Foster-Seely demodulator; i.e., a discriminator which converts the FM signal into an AM signal and then recovers the AM by using envelope detection. The output signal-to-noise ratio is found analytically above and below threshold and the results are verified experimentally. The theoretical analysis includes the effect of quantization noise, frequency jitter in the internal oscillator, and thermal noise.

The system can be integrated and with the use of readily available emitter-coupled logic (ECL) can operate at intermediate frequencies suitable for many space, industrial and commercial applications.

4.2 The Differentiating, Envelope-Dectector Discriminator

The Differentiating, Envelope-Dectector Discriminator is shown in Fig. 4-1. The input FM signal embedded in noise is filtered and then hard limited. The limiter is followed by a filter so that the limiter output is a

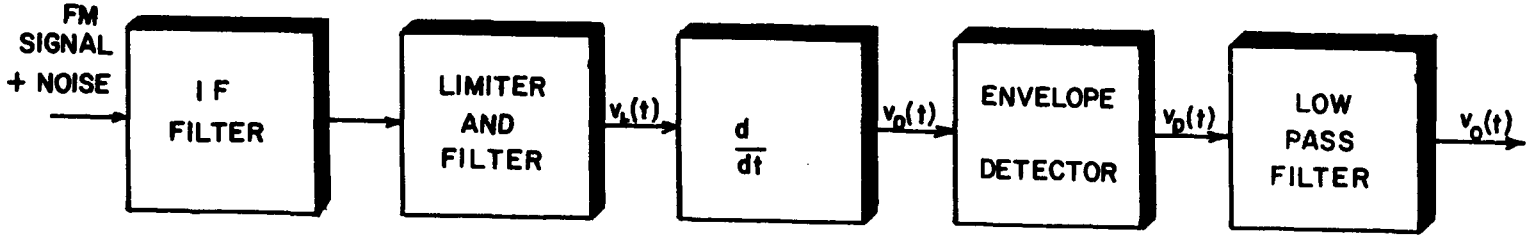


FIG. 4-1 THE DIFFERENTIATING ENVELOPE-DETECTOR DISCRIMINATOR

sinusoidal signal

$$v_L(t) = \sin [\omega_o t+\phi(t)] \tag{4.1}$$

where $\phi(t)$ is the sum of the modulation and phase noise.

The differentiator is usually a combination of tuned circuits adjusted so that the envelope of the voltage is proportional to $\dot{\phi}(t)$. Thus (referring to Fig. 4-1), $v_D(t)$ is

$$v_D(t) = [\omega_o+\dot{\phi}(t)]\cos[\omega_o t+\phi(t)] \tag{4.2}$$

The result is sketched in Fig. 4-2. Note that the envelope of $v_D(t)$ increases as the frequency increases.

The envelope detector follows the envelope of $v_D(t)$ thereby separating (discriminating) the envelope (AM) from the FM signal. The output voltage is obtained by smoothing $v_p(t)$.

It is interesting to note that the envelope detector follows the <u>peak</u> of each cycle of the FM signal. Thus, the true frequency is detected only at the <u>peaks</u> of the FM waveform. Also, these peaks are not uniformly spaced; the spacing varies with the modulation and noise. In addition, the peak voltage must decay sufficiently to follow the maximum possible change in $\dot{\phi}(t)$ during each cycle. In the digital system it will be shown that a

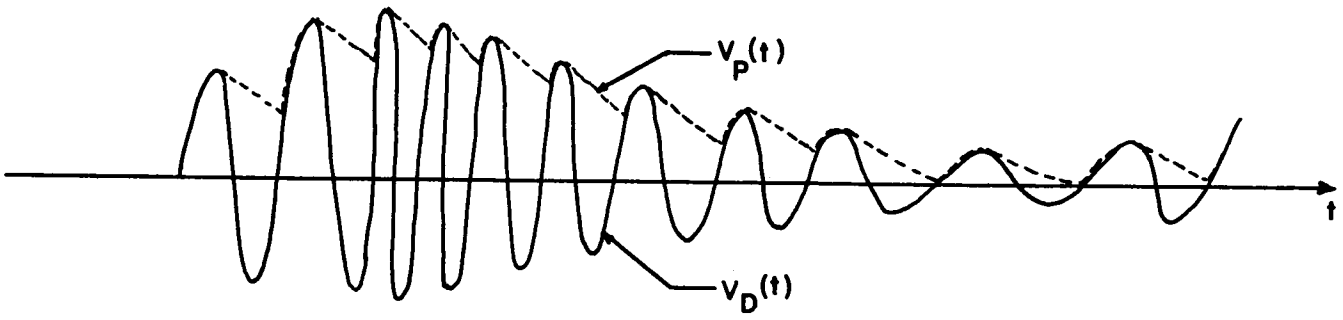


FIG. 4-2 WAVEFORMS IN THE DIFFERENTIATING ENVELOPE-DETECTOR DISCRIMINATOR

system that follows 1 of N peaks, still recovers the modulation.

4.3 The Zero-Crossing Discriminator

The Zero-Crossing Discriminator is shown in Fig. 4-3. In this circuit a Schmitt trigger follows a hard limiter to produce uniform amplitude pulses at each positive zero-crossing of the FM wave. This pulse-position modulated signal gates a sweep circuit as shown in Fig.4-4. The peak of the resulting sweep voltage varies as $\omega_o+\dot{\phi}(t)$. Since the peak value of the voltage is proportional to the time difference, it represents an estimate of the average frequency in the interval. If the interval is sufficiently small, the amplitude is approximately equal to the frequency at the center of the interval. Thus, the peak voltage at time t_k is approximately

$$v_o(t_k) \doteq \omega_o + \dot{\phi}\left[\frac{t_k+t_{k-1}}{2}\right]$$

if t_k-t_{k-1} is sufficiently small. The envelope detector again is used to separate the amplitude modulation from the frequency modulation of the sweep voltage.

In summary, both the differentiating, envelope-detector discriminator and the zero-crossing discriminator are similar, converting an FM signal into an AM-FM signal and removing the AM from the FM by envelope detecting.

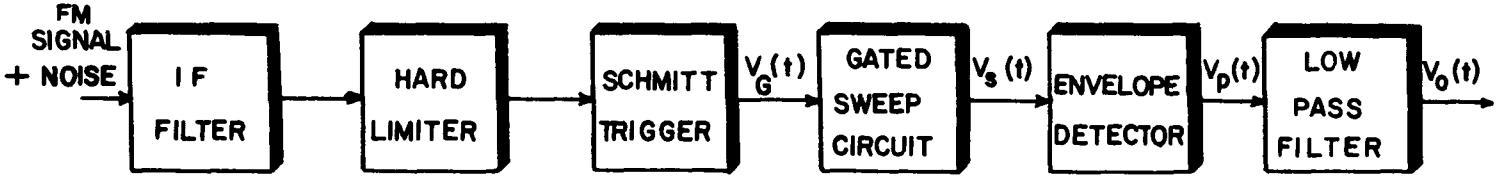


FIG. 4-3 AN ANALOG ZERO-CROSSING DISCRIMINATOR

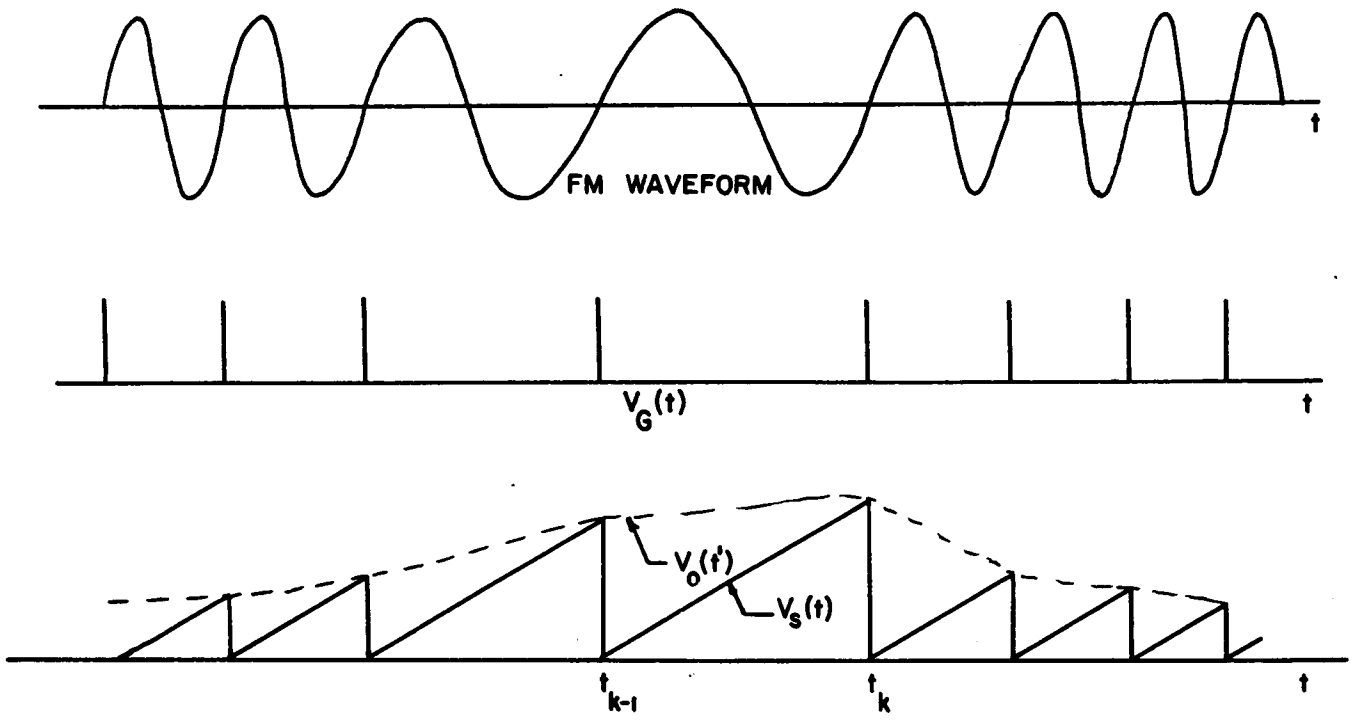


FIG. 4-4 WAVEFORMS IN THE ZERO-CROSSING DISCRIMINATOR

It is interesting to note that the PPM waveform $v_G(t)$, shown in Fig. 4-4, if low-pass filtered, will approximately demodulate the FM signal. This type of PPM detection has its counterpart in the system shown in Fig. 4-1, where by full-wave (or half-wave) rectifying the limiter output, $v_L(t)$, and then low-pass filtering the result, produces a demodulated output.

4.4 The All Digital FM Discriminator

The All Digital FM Discriminator is shown in Fig. 4-5. As before, the FM signal and noise is filtered and then hard limited. The limiter output has only two possible values; hence, a binary format. The output of the limiter enters a digital frequency divider which passes every Nth positive word. As seen in Fig. 4-6, these words close and open a gate to pass high frequency clock pulses. The clock pulses cause a counter to produce an output word proportional to the number of pulses counted during the N positive zero-crossings.

The digital processor is a read-only-memory (ROM) programmed to invert v_c and then subtract from the result a number equal to the carrier frequency f_c. Thus, the output of the ROM, $v_p(t)$ is a digital word which can have a positive or a negative polarity. Note that $v_p(t)$ is the digital equivalent to the envelope detector used in

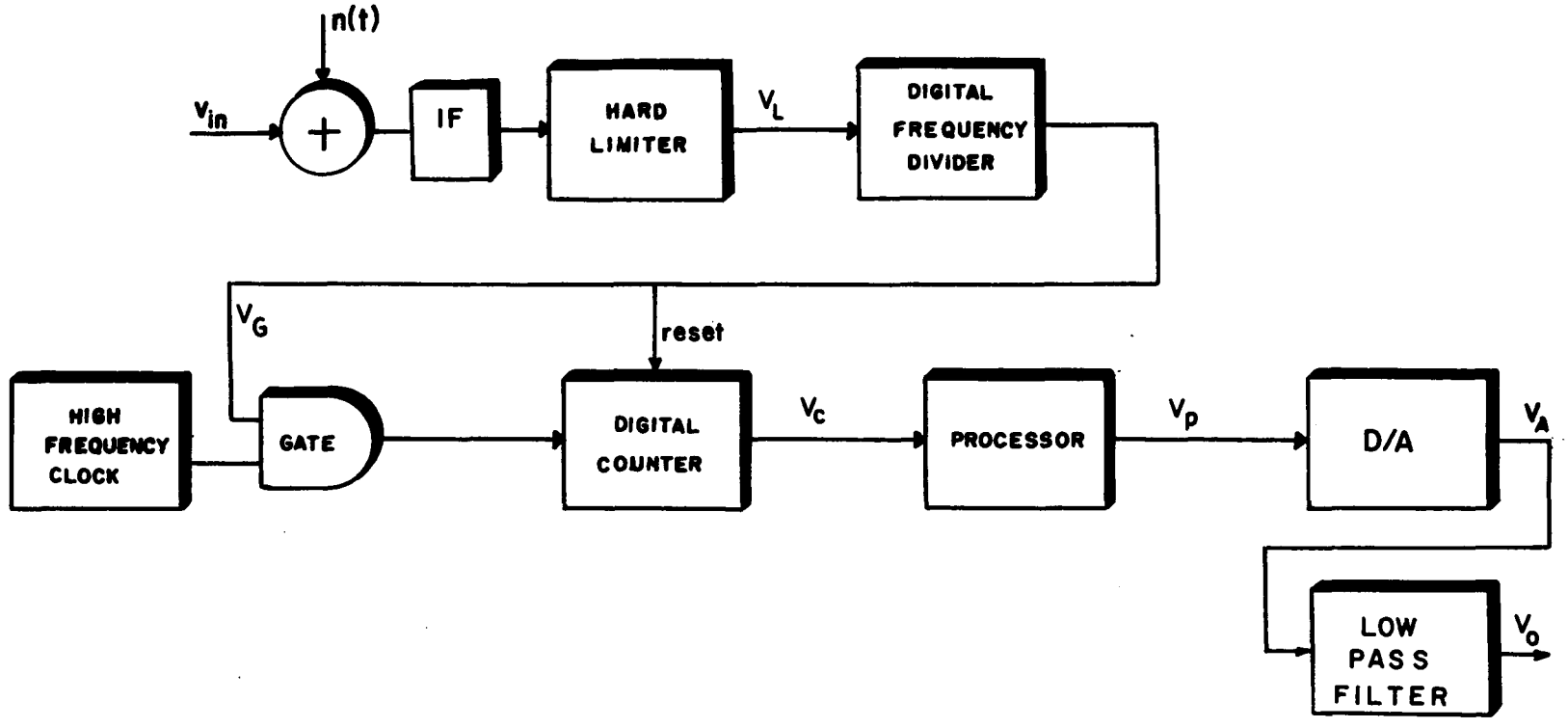


FIG. 4-5 BLOCK DIAGRAM OF THE DIGITAL FM DISCRIMINATOR MODIFIED TO PRODUCE AN INCREASE IN QUANTIZATION LEVELS.

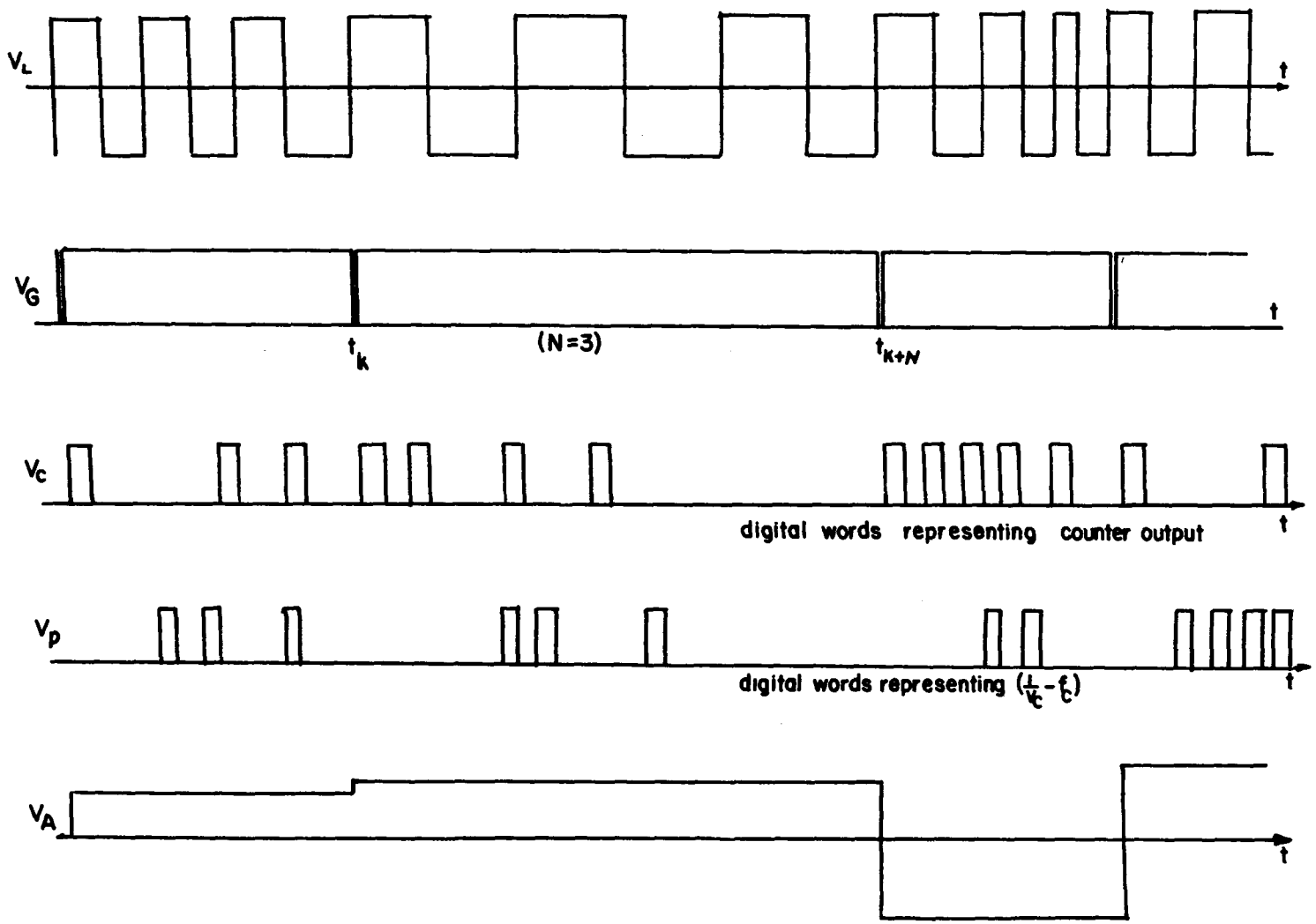


FIG. 4-6 WAVEFORMS IN THE DIGITAL DISCRIMINATOR

Figs. 4-1 and 4-3. Thus, $v_o(t)$ is the demodulated output of the All Digital Discriminator.

The output voltage is similar to the output of an analog discriminator. However, there are several distinctions between the systems. The first distinction is that every Nth positive zero-crossing is considered rather than every positive zero-crossing. The counter counts pulses in this interval; the difference in the number of pulses that are able to be counted at the maximum and minimum deviations represent the system accuracy. Thus, the signal at the counter output is quantized. Dividing by N increases the count allowing a larger number of quantization levels while employing a commercially available clock. Note that as in the zero-crossing discriminator, the counter output at time t_{k+N} is approximately equal to the frequency at time $(t_{k+N} + t_k)/2$ if $t_{k+N} - t_k$ is sufficiently small. The constraint limits the value of N and is discussed below.

Another, and an even more interesting distinction is the use of the D/A converter which holds the peak amplitude until the next word appears, at which time that amplitude is held. This is in constrast to the envelope detector whose amplitude decays exponentially between peaks. This difference is not noticeable at the output because of the smoothing of the output low-pass filter. As shown in Fig. 4-7, the output is produced by

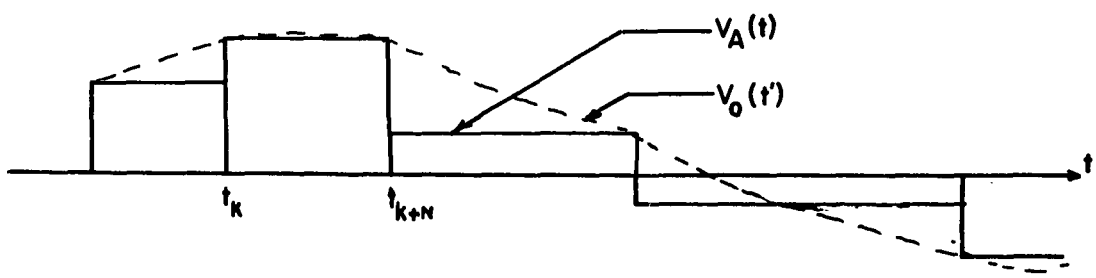


FIG. 4-7 OUTPUT WAVEFORM OF THE DIGITAL DISCRIMINATOR

steps (or impulses) of varying height and width just as the analog discriminators.

4.4.1 Design of the Digital Discriminator

Consider the case where the input frequency is deviated to the maximum value, $f_c + \Delta f$, where f_c is the nominal carrier frequency, and Δf is the peak frequency deviation. The time between successive positive zero-crossings, τ, is then a minimum and given by

$$\tau_{min} = \frac{1}{f_c + \Delta f}$$

The number of pulses appearing in the counter, n, is then also a minimum and is given by

$$n_{min} = f_{cL}\tau_{min}$$

where f_{cL} is the frequency of the high speed clock. Now, let the input frequency deviate to the minimum value $f_c - \Delta f$. The time between successive positive zero-crossings becomes

$$\tau_{max} = \frac{1}{f_c - \Delta f} \tag{4.3}$$

and

$$n_{max} = f_{cL}\tau_{max} \tag{4.4}$$

If one-to-one coding is used, each word that appears

in the counter corresponds to a particular output level. The difference in the pulse count, $n_{max} - n_{min}$, is the total number of quantization levels that appears at the output. Letting M be the number of quantization levels yields,

$$M = n_{max} - n_{min} = f_{cL}(\tau_{max} - \tau_{min})$$

$$M = f_{cL}\left[\frac{1}{f_c - \Delta f} - \frac{1}{f_c + \Delta f}\right] \qquad (4.5)$$

Since the output is proportional to the inverse of τ, the tendency is for the quantization levels to cluster when τ is a minimum. Therefore, so that each different count that appears in the binary counter corresponds to a different quantization level, a restriction is imposed on the frequency deviation so that

$$\Delta f \ll f_c$$

This is a narrowband condition and it will suffice to use the restriction

$$\Delta f \leq 0.1 f_c \qquad (4.6)$$

It is seen from (4.5) that the number of quantization levels M is increased by increasing the clock frequency, f_{cL}, and also by decreasing the nominal frequency f_c. This results in a decrease in the quantization noise.

Additional quantization levels can be obtained by inserting a digital frequency divider after the hard limiter as shown in Fig. 4-5. The digital frequency divider is composed of flip-flops and gates to produce frequency division by integer N.

With the divider in the circuit, pulses now accumulate in the counter for a period of $N\tau$. From (4.5) the new number of quantization levels becomes

$$M' = NM = Nf_{cL}\left[\frac{1}{f_c - \Delta f} - \frac{1}{f_c + \Delta f}\right] \qquad (4.7)$$

Determination of N -- Signal to Distortion Ratio

Consider the input signal

$$\sin[\omega_c t + \phi(t)]$$

Assume that at time t_k a positive zero-crossing occurs. Then

$$\omega_c t_K + \phi(t_k) = 2\pi k \qquad (4.8)$$

Similarly, at time t_n the Nth consecutive positive zero-crossing occurs so that

$$\omega_c t_n + \phi(t_n) = 2\pi(K+N) \qquad (4.9)$$

Subtracting (4.8) from (4.9) yields an expression for a time interval between the N positive zero-crossings; viz.,

$$t_n - t_k = \frac{N}{f_c} - \frac{\phi(t_n) - \phi(t_K)}{\omega_c}$$

Thus,

$$\tau = \frac{N}{f_c} - \frac{1}{\omega_c}\left[\frac{\phi\left(T + \frac{\tau}{2}\right) - \phi\left(T - \frac{\tau}{2}\right)}{\tau}\right]\tau \qquad (4.10)$$

where $T \equiv \frac{t_n+t_K}{2}$ and $\tau \equiv t_n - t_K$. Solving (4.10) for $1/\tau$ (assuming small deviations) yields

$$\frac{1}{\tau} = \frac{f_c}{N} + \frac{1}{2\pi N}\left[\frac{\phi(T + \tau/2) - \phi(T - \tau/2)}{\tau}\right] \qquad (4.11)$$

Equation (4.11) shows explicitly the limitation of the digital discriminator (and the zero-crossing discriminator), since N/τ is approximately equal to $f_c + \frac{1}{2\pi}\dot{\phi}(T)$ only if τ is small. Note again that the voltage produced at t_n is proportional to the frequency at $T=(t_n + t_k)/2$. To determine how closely (4.11) approximates the actual frequency, the term $\phi(T + \tau/2) - \phi(T - \tau/2)$ is expanded. Then

$$\psi(t_n) \equiv \frac{N}{\tau} - f_c = \frac{1}{2\pi}\left[\frac{\phi(T+\tau/2) - \phi(T-\tau/2)}{\tau}\right]$$

$$= \frac{1}{2\pi}\left[\dot{\phi}(T) + \frac{\tau^2}{24}\dddot{\phi}(T) + \frac{\tau^4}{192}\phi^{(5)}(T) + \ldots\right] \qquad (4.12)$$

where $\phi^{(5)}(T) = \frac{d^5}{dt^5}\phi(t)\Big|_{t=T}$

To determine τ (and hence N), the thermal noise is neglected and $\dot{\phi}(t)$ is set to m(t), the modulating signal. Then, if m(t) is assumed gaussian, with zero mean and

power spectral η_m = constant for $-f_M \leq f \leq f_M$ and zero elsewhere, the signal-to-distortion ratio is found to be

$$\frac{S_o}{N_D} = \frac{2\eta f_M}{(2\eta f_M)(2\pi\tau f_M)^4/2880} = \left[\frac{7.4}{2\pi\tau f_M}\right]^4 \qquad (4.13)$$

To maintain the signal-to-distortion ratio less than 40dB, for example, yields

$$10 = \frac{7.4}{2\pi\tau f_M}$$

or

$$\frac{f_c}{N} = \frac{1}{\tau} = 8.5\ f_M \qquad (4.14)$$

[Note that $1/\tau$ was approximated by fc the carrier term. This is valid since this merely represents a bound on fc/N, and also, in practical systems, $\omega_c >> |m(t)|$.]

Equation (4.13) is used to determine N. Its use in the system design is explained in Sec. 4.6.

4.4.2 Quantization Noise

Assuming the error caused by quantization is uniformly distributed within a quantization level the noise power that appears at the output is given by [4-1], (the quantization noise is, in general, assumed to be white),

$$N_q = \frac{S^2}{12}\, 2f_M\bar{\tau} \qquad (4.15)$$

where,

S = step size (rad)

$\bar{\tau}$ = average time between computations = $\frac{N}{f_c}$

f_M = output low-pass filter frequency cutoff

4.4.3 Effect of Clock Jitter

Associated with the high frequency clock is the short term frequency stability specification commonly called "jitter." Crystal controlled oscillators maintain a nominal frequency within $\pm$1part/10^8 for short-time intervals. However, the unavailability of a crystal clock at the time this research was conducted forced the use of an astable multivibrator capable of an rms jitter of $\pm$2 parts/10^3 ($\pm$0.2%). The result of this frequency jitter is an added noise source that affects the output and is taken into consideration.

To calculate the average output noise power caused by the clock jitter, note that the number of quantization levels given in (4.7) is directly proportional to the clock frequency, f_{cL}. Hence, the number of quantization levels affected by the jitter is given by,

$$M_j' = \pm\Delta M' \qquad (4.16)$$

If one-to-one coding is assumed, the error caused by

jitter is,

$$e_j = \pm \Delta M' S$$

where S is the step size.

If the jitter is assumed to be gaussian distributed in amplitude with an rms jitter of $\Delta M'$, the power spectral density of the jitter is,

$$G_j(f) = (\Delta M' S)^2 \bar{\tau}$$

where $\bar{\tau}$ is the average length of the computation interval. Hence the output noise power (after the low-pass filter) is given by

$$N_j = (\Delta M' S)^2 \bar{\tau}\ 2f_M \qquad (4.17)$$

4.4.4 The Effect of Thermal Noise on the Output Noise Power

Since the digital discriminator is identical in form to the analog discriminator with the exception of the quantization noise, the thermal noise is the same as in the ordinary discriminator both above and at threshold. Thus the gaussian component of the output noise is [4-2]

$$N_q = \frac{4\pi^2 f_M^2}{3\ Si/\eta f_M} \qquad (4.18)$$

and the spike component is [4-3]

$$N_s = 8\pi^2 f_M |\overline{\delta f}| \exp\left[-\frac{1}{\beta+1}\frac{S_i}{\eta f_M}\right] \qquad (4.19)$$

where,

f_M = output low-pass filter frequency cutoff

$|\overline{\delta f}|$ = phase deviation

S_i = input signal power

η = one-sided noise power spectral density

$\beta = |\overline{\delta f}|/f_M$

4.4.5 Output Signal-to-Noise Ratio

To find the theoretical output signal-to-noise ratio, an expression for signal power is needed. If sinusoidal modulation is assumed, the output signal power after filtering becomes

$$S_o = \frac{(\Delta\omega)^2}{2} \qquad (4.20)$$

where $\Delta\omega$ is the peak frequency deviation.

Combining the total noises given in (4.14), (4.17), (4.18), and (4.19) the average output signal-to-noise ratio is obtained; viz.,

$$\frac{S_o}{N_o} = \frac{(\Delta\omega)^2/2}{N_q+N_j+N_{th}+N_s} \qquad (4.21)$$

Note that the step size, $S = 2\Delta\omega/M'$, and the value of N was adjusted so that the harmonic distortion is negligible compared to N_q.

4.5 Experimental Results

The digital FM discriminator was constructed and tested using sinewave modulation for several values of M' and β. The system parameters were adjusted to ensure low distortion. The rms clock jitter was not negligible and was measured to be 0.2%. The results are shown in Figs. 4-8 and 9. Referring to Fig. 4-8, β=3, it is seen that there exists three distinct regions: Below 15 dB is threshold. Above 15 dB the system is first thermal noise limited (high input SNR region) and then quantization noise limited. Note that when $M' = 2^{10}$, S/N_q should be 60 dB; and when $M' = 2^8$, S/N_q should be 48 dB. Instead, the system is limited by the clock jitter. This noise could be reduced significantly by using a crystal clock.

Figure 4-9 shows the results for β=10. Here, since threshold occurs at a higher input SNR, the thermal noise region is greatly reduced. Again, the 8 and 10 bit systems are limited by the clock jitter.

Note the reasonably good experimental veriafication obtained. A block diagram of the test facility is shown in Fig. 4-10.

4.6 A Digital Discriminator Design Example

To illustrate the design of the digital discriminator, consider the following example: An input signal-to-noise ratio, $S_i/\eta f_M$ = 25 dB is available from the channel and

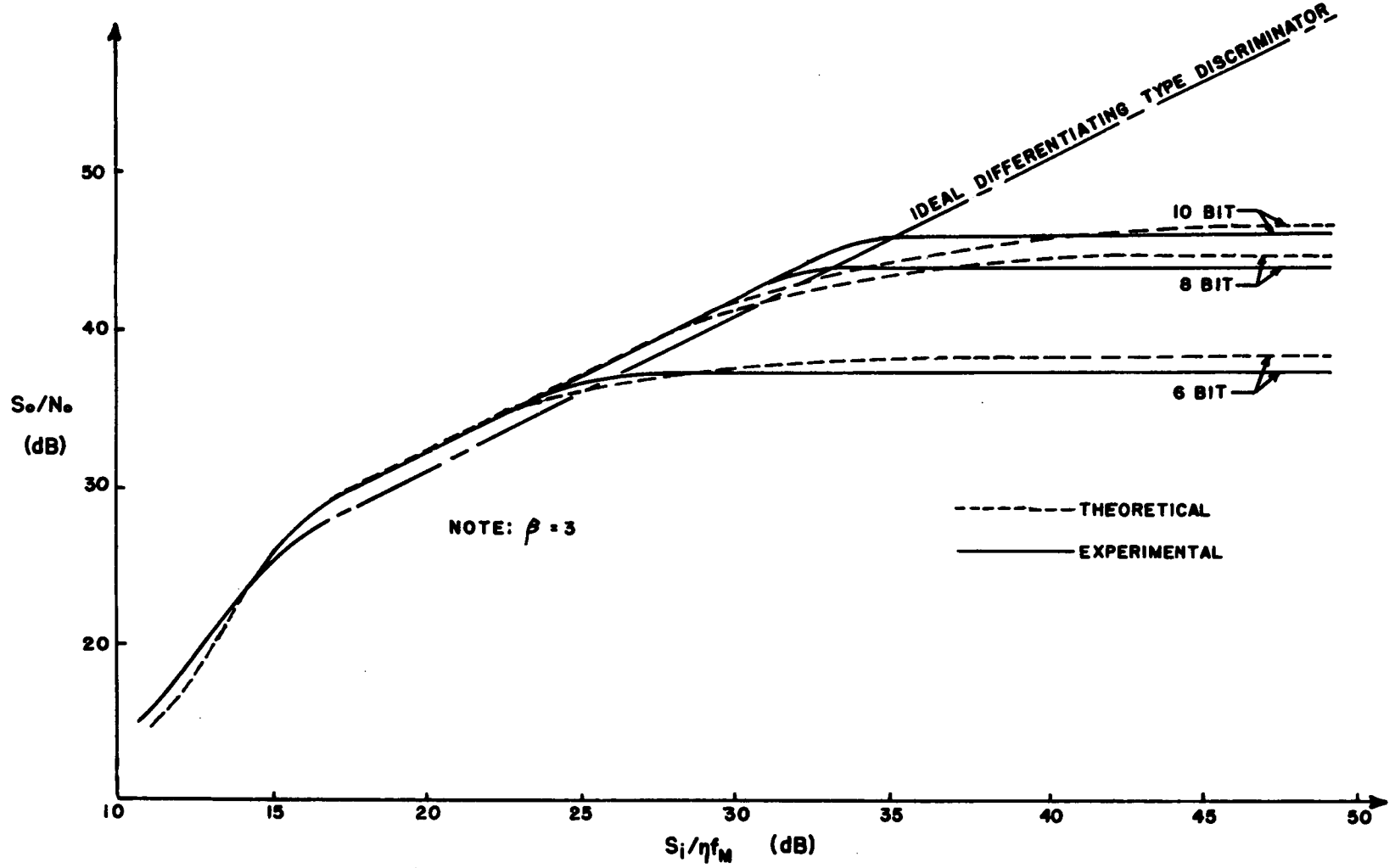


FIG. 4-8 OUTPUT SIGNAL-TO-NOISE RATIOS OF THREE DIGITAL DISCRIMINATOR DESIGN EXAMPLES (β = 3)

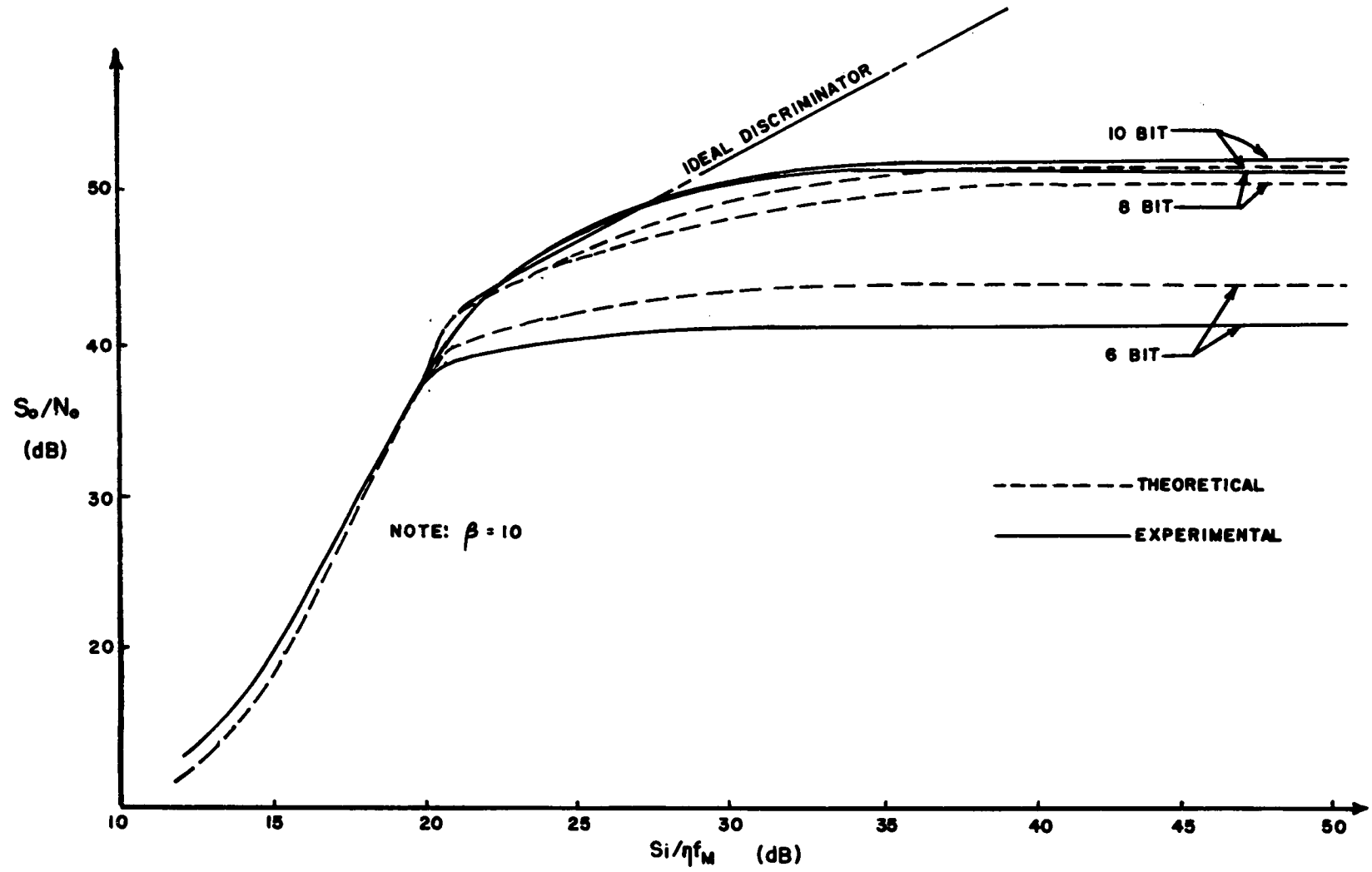


FIG. 4-9 OUTPUT SIGNAL TO NOISE RATIOS OF THREE DIGITAL DISCRIMINATOR DESIGN EXAMPLES (β = 10)

an output signal-to-noise ratio of 35 dB is required. The modulating signal is bandlimited to 5 kHz and the carrier rms frequency deviation is limited to 15 kHz. A carrier frequency of 1 MHz is employed. The distortion is to be kept 40 dB below the signal. The design problem is to specify the clock frequency, f_{cL}, and N.

The solution is as follows: Operating above threshold, the maximum output signal-to-noise ratio is [4-4]

$$\frac{S_o}{N_o} = 3\left[\frac{\Delta f_{rms}}{f_M}\right]^2 \frac{S_i}{\eta f_M} = 39 \text{ dB}$$

To ensure that the distortion noise is 40 dB below the output signal power [see (4.14)]

$$\frac{f_c}{N} = 8.5\, f_M$$

Hence N=23. Coupled with the thermal noise this yields a net output SNR of 37 dB. To prevent degradation by quantization, the quantization noise is set to 42 dB below the output signal power yielding M', the number of quantizing levels, equal to 128. Using (4.7), i.e.,

$$M' = N\, f_{cL}\left[\frac{1}{f_c-\Delta f} - \frac{1}{f_c+\Delta f}\right]$$

and assuming the peak deviation $\Delta f = 3\Delta f_{rms} = 45$ kHz, yields

$$f_{cL} = 62 \text{ MHz}$$

The total output signal-to-noise ratio is then 35.5 dB. Note that the clock jitter can be ignored if [see (4.16)]

$$\frac{\Delta f}{f_{cL}} = \frac{\Delta M'}{M'} < \frac{1}{128} = .78\%$$

This is an extremely easy specification to meet. Also a clock frequency of 62 MHz is easily implemented using readily available digital logic [4-5].

4.7 Conclusions

The theoretical equations governing the operation of a digital discriminator have been obtained. It is shown that the digital device operates in a manner similar to the zero-crossing discriminator and the differentiating-type discriminator.

Design equations and an illustrative example have also been presented.

A comparison of theoretical and experimental results verify the theory.

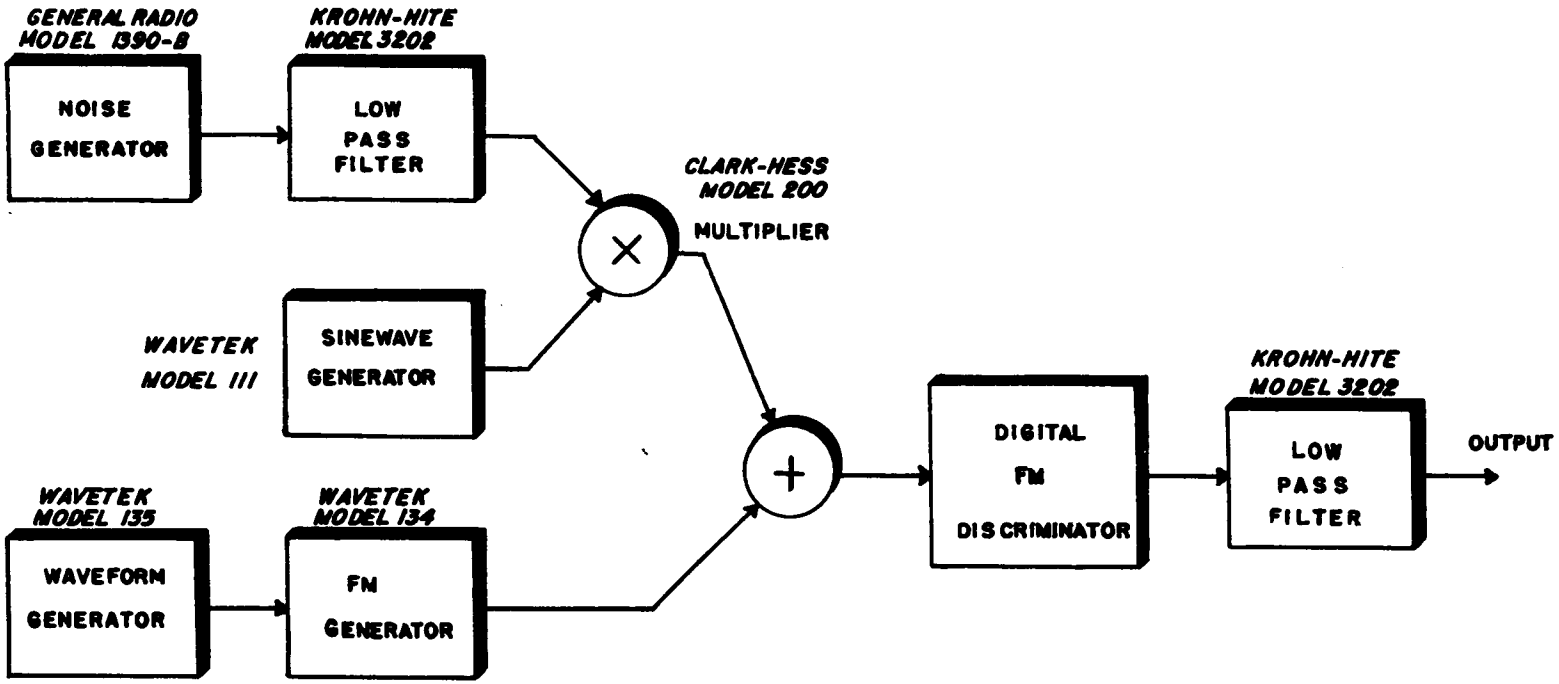


FIG. 4-10 TEST FACILITY FOR EVALUATING THE DIGITAL FM DISCRIMINATOR

Chapter 5

AN ALL DIGITAL PHASE LOCKED LOOP FOR FM DEMODULATION

5.1 Introduction

At the present time, digital phase locked loops are being employed only for carrier phase tracking of received signals, thus generating a signal suitable for synchronous demodulation [5-1]. When used for FM demodulation, phase locked loops employ analog circuitry in the construction. However, analog implementation has the following disadvantages:

1. Since the voltage controlled oscillator (VCO) present in all phase locked loops must change frequency in response to a phase input, the circuit becomes an integrator. Analog integrators are always "leaky," i.e., do not respond to a DC input in a linear fashion.

2. The phase detector and amplifiers insert inaccuracies and spurious poles in the closed loop system. The inaccuracies are due to the multiplication that is needed in phase detection. Also, analog multipliers are extremely sensitive to DC drift or any offset erroneously appearing on the multiplier inputs.

3. The saturation of components in the phase locked loop is extremely common when the input carrier-to-noise ratio is low enough so that noise spikes appear. When this type of input is present, the loop must tolerate the condition where the signal "rides" on the noise rather

than the noise on the signal. If the VCO saturates due to a noise spike, all previous information stored during the integration procedure is lost. Therefore, when the spike is no longer present, the loop reverts to a transient state where signal acquisition begins as if there was an inception of system power.

4. When an attempt is made to augment an analog loop to a higher order system, stray capacitance inserts additional poles and the system has a tendency to become unstable when noise is present.

To avoid these problems, the phase locked loop described in this chapter is designed with all digital circuitry. Along with digital adders, multipliers, scalers and filters, a digital voltage controlled oscillator algorithm is also designed. The problems mentioned above are eliminated; however, new phenomena common to digital systems become apparent. These include roundoff and overflow errors taking the form of quantization noise.

5.2 Description of the System

The all Digital Phase Locked Loop is shown in block diagram form in Fig. 5-1. Referring to the figure, the input FM signal is passed through a sample-and-hold amplifer, converted to digital format using an A/D converter, and then sent to the digital multiplier. The

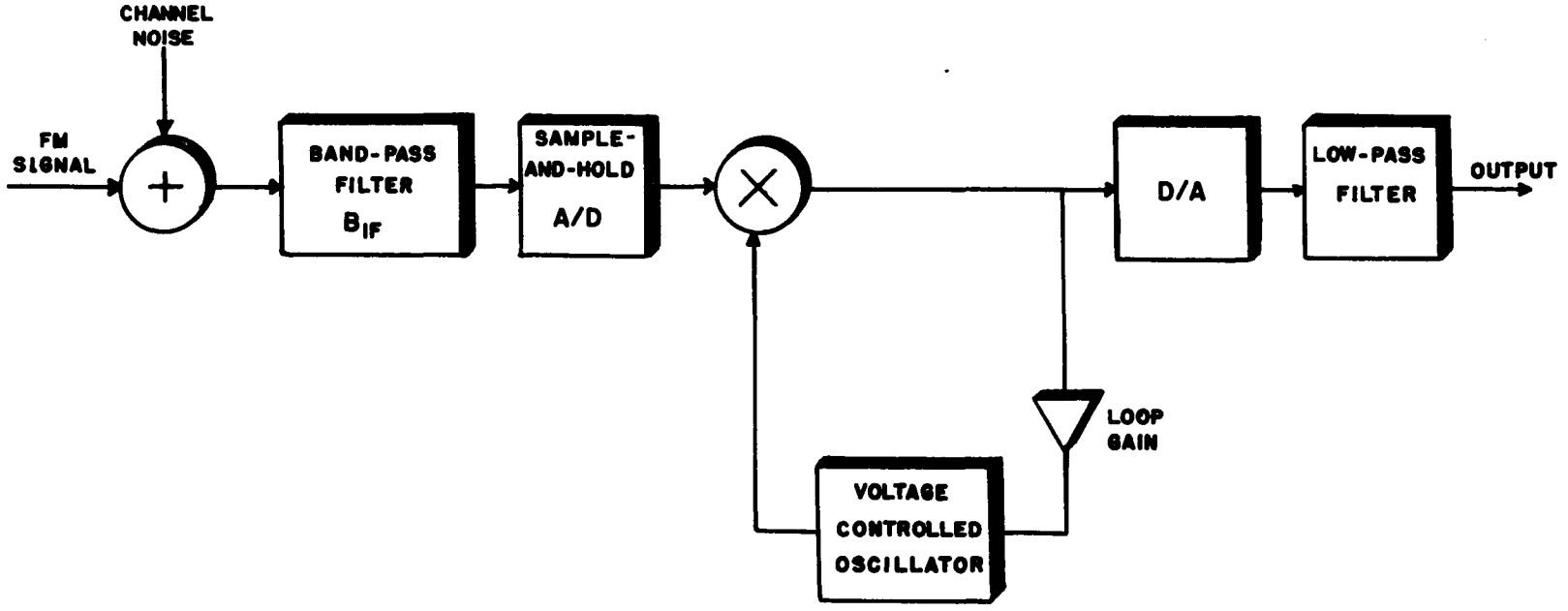


FIG. 5-1 BLOCK DIAGRAM OF THE DIGITAL PHASE LOCKED LOOP

output of the multiplier is the product of the input signal and the output of the digital voltage controlled oscillator (VCO). This product becomes the input to the forward loop digital filter. The resulting output of the forward loop filter becomes the input to the digital VCO and the output of the loop. Analog format is obtained when the loop output is passed through a D/A converter.

To realize this system in real time, special purpose algorithms are developed and are described in the ensuing sections.

5.2.1 Determination of the Sampling Frequency

If an input FM signal operating at a typical IF frequency is sampled at a frequency twice the highest frequency, the samples would have to be processed at a rate much beyond the rate possible with any type of high speed processor available today. Referring to Fig. 5-2, it becomes clear that the input signal can be sampled much below twice the highest frequency without having the spectrums overlap if the following conditions are met:

$$f_s \geq 2B \tag{5.1}$$

$$nf_s = f_o - \frac{B}{2} \tag{5.2}$$

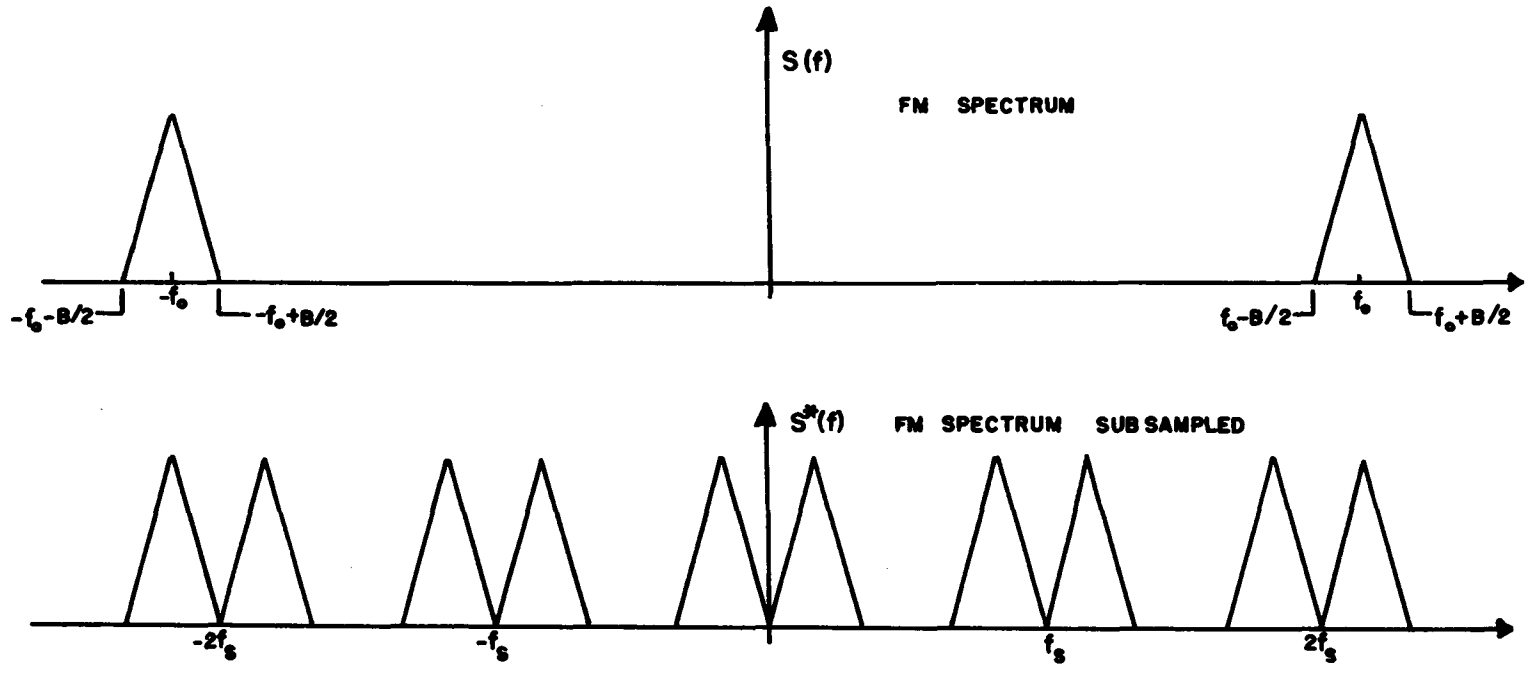


FIG. 5-2 FM SPECTRUM SUBSAMPLED WITH n=2

where

f_s = sampling frequency

B = IF Bandwidth

n = positive integer

The carrier frequency, f_o, can be made as large as desired, limited only by the ambiguity window of the sample and hold amplifier. The sampling frequency which is also the processing rate is limited by the logic speed. Hence, from (5.2) increasing f_o increases the integer n. For clarity, Fig. 5-2 is shown for n = 2.

Using an equality for (5.1) and substituting in (5.2), the following equation results:

$$nf_s = f_o - \frac{f_s}{4} \tag{5.3}$$

Solving (5.3) for the carrier frequency, f_o,

$$f_o = (n + \tfrac{1}{4})\, f_s \tag{5.4}$$

The result obtained in (5.4) becomes useful when the input FM waveform and digital VCO are characterized after sampling. The FM signal has the form,

$$x(t) = A \cos\left[\omega_o t + \varphi(t) \right] \tag{5.5}$$

where ω_o is the carrier frequency in radian / second, and $\varphi(t)$ is the integral of the modulating message. After sampling, (5.5) becomes,

$$x(kT) = A \cos\left[\omega_o kT + \varphi(kT)\right] \qquad (5.6)$$

where k is an integer and $T = 1/f_s$. However, from (5.4),

$$T = 1/f_s = (n + \tfrac{1}{4})/f_o \qquad (5.7)$$

Inserting (5.7) into (5.6), the FM wave has the following form:

$$x(kT) = A \cos\left[2\pi k\,(n + \tfrac{1}{4}) + \varphi(kT)\right] \qquad (5.8)$$

Finally, since k and n are both integers,

$$x(kT) = A \cos\left[\pi\, k/2 + \varphi(kT)\right] \qquad (5.9)$$

Equation (5.9) is the mathematical representation of the FM input to the digital multiplier. The other multiplier input is discussed next.

5.2.2 Digital VCO Algorithm

If the VCO in the phase locked loop is an analog type oscillator, its output can be described as

$$v(t) = B \cos\left[\omega_o t + G_v \int_o^t v_{in}(\tau)\, d\tau\right] \qquad (5.10)$$

where

$v_{in}(\tau)$ = VCO input

G_v = VCO gain

ω_o = carrier frequency

After sampling and substituting (5.7), (5.10) becomes,

$$v(kT) = B \sin\left[\pi k/2 + G_v \sum_{n=0}^{k-1} v_{in}(nT) \right] \quad (5.11)$$

Since the output of the VCO is of interest only at the sampling instant as in (5.11), the output can be generated by computing the phase of the waveform at the sampling instant. Therefore, the continuous waveform is not generated in this system. To see how the output is generated, first (5.11) is rewritten to read

$$v(kT) = B \sin\left\{ \sum_{n=0}^{k-1} \left[(G_v v_{in}(nT) + \pi/2) \right] \right\} \quad (5.12)$$

That is, at each sampling instant, the input to the VCO, v_{in}, integrated (digitally), the constant $\pi/2$ is added, and the VCO output computed. This output is now fed to the multiplier.

5.2.3 Digital Multiplier

In a general purpose computer, the multiplication of two digital words is accomplished by successive addition of the multiplicand [5-2]. This operation is the most time consuming process in a digital computer. A much faster method would involve the use of a read-only-memory (ROM). The multiplication of two ten bit words is explained via Fig. 5-3. The multiplicand addresses half the memory while the multiplier addresses the second

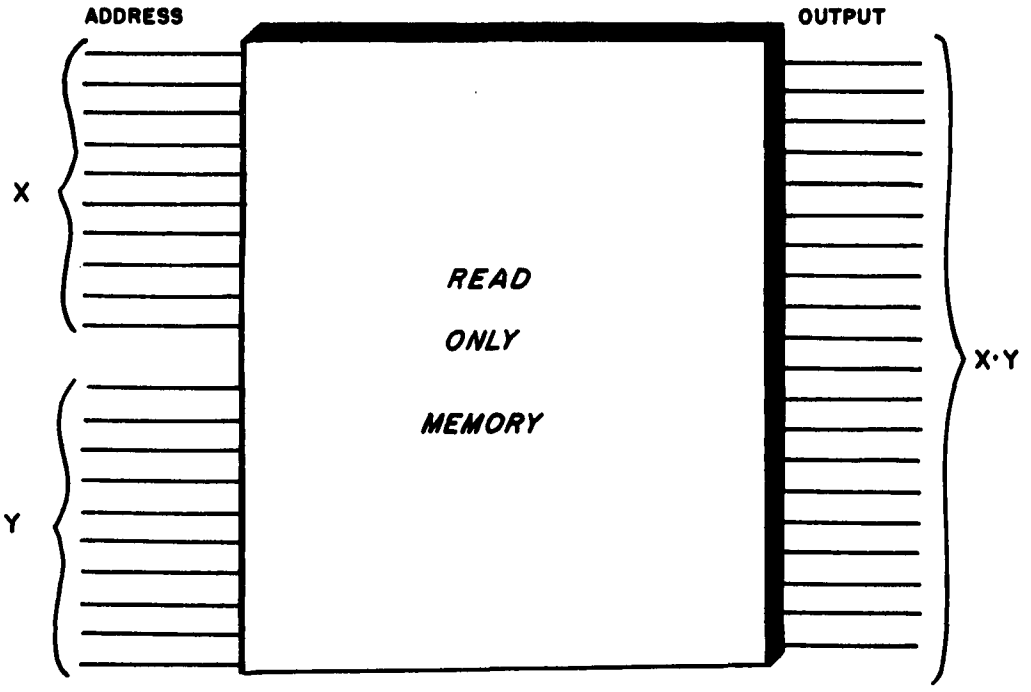


FIG. 5-3 A READ-ONLY MEMORY USED AS A DIGITAL MULTIPLIER

half. Since there exists a unique memory location for any two input words, the ROM can be preprogrammed to perform multiplication, division, addition, or any function the user desires. Typical access time for present day ROM's are less than 500 ns [5-3]. Note the output of the multiplier is a word that contains up to twenty significant digits depending upon the accuracy needed. For twenty bit output words, a 20 x 20 ROM is required, while for ten bit accuracy, a 10 x 10 ROM is needed.

The inacessibility of ROM's is circumvented by modifying the VCO described by (5.12) to be a squarewave rather than a sinewave. The coefficient of (5.12) is set to 1, and the equation of the new digital VCO becomes,

$$v(kT) = S_q\left\{\sum_{n=0}^{k-1}\left[G_v v_{in}(nT) + \pi/2\right]\right\} \qquad (5.13)$$

where

$$S_q(x) = \begin{cases} +1, & 0 \le x < \pi \\ -1, & \pi \le x < 2\pi \end{cases}$$

and,

$$S_q(x) = S_q(x + 2\pi)$$

Now, the multiplier either passes the input signal unchanged, or inverts the input word. This process is easily accomplished using a bank of "exclusive - or" logic gates as shown in Fig. 5-4. From the figure, one

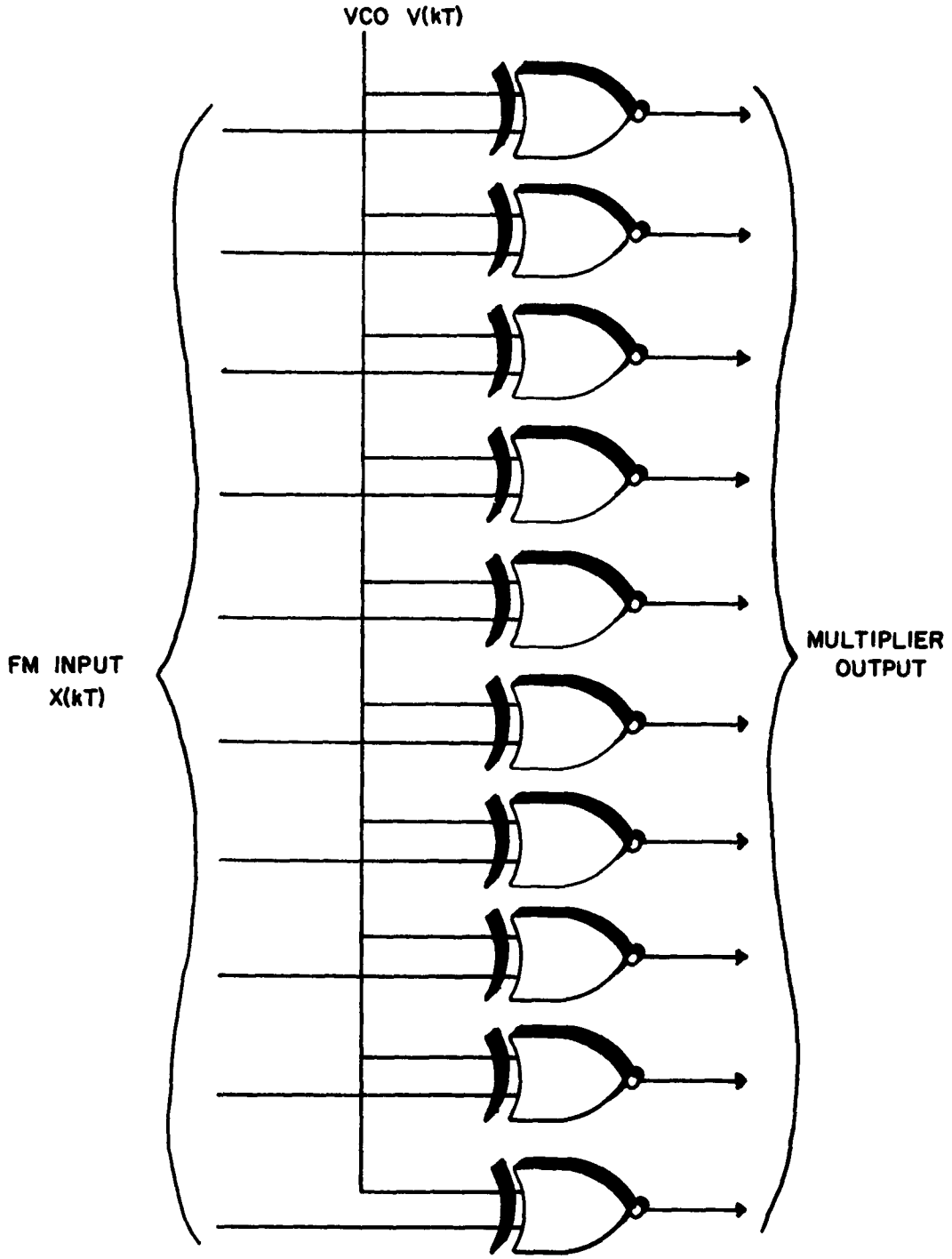


FIG. 5-4 EXCLUSIVE-OR GATES USED AS A DIGITAL MULTIPLIER

sees that each bit of the input word is an input to one gate. The VCO output (one wire) is a common input to all the gates.

The computation of $S_q(x)$ is accomplished by dividing the binary scale into intervals of length π. Then by examining one bit of the VCO output word the particular π interval in which the argument of $S_q(x)$ falls is easily determined by the value of that bit (1 or 0). Note that the periodicity of the $S_q(x)$ corresponds to the periodicity of binary numbers. Hence, the VCO integrator never saturates and the saturation logic described in Section 2.2 is inhibited.

The gain of the VCO is determined by which bit is selected to determine the π intervals. For example, if +5 volts is encoded as the maximum positive binary number in the ten bit word (1111111111), the selection of the second most significant bit to represent a π interval results in a VCO gain of $\pi/2.5$ rad/volts; the selection of the third most significant bit to represent a π interval results in a VCO gain of $\pi/1.25$ rad/volt; etc.

5.2.4 Harmonic Distortion

The use of the squarewave VCO algorithm results in an increase of harmonic distortion that is propagated to the output of the Digital Phase Locked Loop. To see this, the output of the VCO is expanded into a Fourier

series; i.e.,

$$v(kT) = \frac{4}{\pi} \sin\left[\frac{\pi k}{2} + \hat{\varphi}\ (kT) \right] - \frac{4}{3\pi} \sin\left[\frac{3\pi k}{2} + 3\,\hat{\varphi}\ (kT) \right]$$

$$+ \frac{4}{5\pi} \sin\left[\frac{5\pi k}{2} + 5\,\hat{\varphi}(kT) \right] + \cdots \qquad (5.14)$$

where $\hat{\varphi}\ (kT)$ is the VCO phase at the sampling instant.

When the input given in (5.9) is multiplied by (5.14) the following appears at the multiplier output:

$$v_o\ (kT) = \frac{2A}{\pi} \sin\left[\hat{\varphi}\,(kT) - \varphi\ (kT) \right] + \frac{2A}{3\pi} \sin\left[3\hat{\varphi}(kT) + \varphi\ (kT) \right]$$

$$+ \frac{2A}{5\pi} \sin\left[5\hat{\varphi}(kT) - \varphi\,(kT) \right] + \cdots + \text{terms at}$$

$$\text{half the sampling frequency } (\pi k) \qquad (5.15)$$

It is seen from (5.15) that there exists unwanted distortion terms that appear in the baseband. To minimize the effect of these terms, the sampling frequency is chosen so that

$$f_s = NB \qquad (5.16)$$

where N is any integer equal to or greater than 2. (Note in the previous analysis where a sinewave VCO was used, it was sufficient to choose N = 2.) Inserting (5.16) into (5.2) yields,

$$f_o = \left(n + \frac{1}{2N}\right) f_s \qquad (5.17)$$

When (5.17) is inserted into the equations for the input, (5.9) and the squarewave VCO (5.14) the following appears at the output of the multiplier,

$$v_o(kT) = \frac{2A}{\pi}\sin\left[\hat{\varphi}(kT) - \varphi(kT)\right] + \frac{2A}{\pi}\sin\left[\frac{2\pi k}{N} + \hat{\varphi}(kT) + \varphi(kT)\right]$$
$$- \frac{2A}{3\pi}\sin\left[\frac{2\pi k}{N} + 3\hat{\varphi}(kT) - \varphi(kT)\right]$$
$$+ \frac{2A}{3\pi}\sin\left[\frac{2\pi k}{N} + 3\hat{\varphi}(kT) + \varphi(kT)\right] + \cdots$$
$$+ \frac{2A}{(2N-1)\pi}\sin\left[(2N-1)\hat{\varphi}(kT) + \varphi(kT)\right] \qquad (5.18)$$

Now it is seen that depending upon the choice of N, only the squarewave harmonics of higher order need be shifted (or folded) to the baseband (DC). In fact, the 2N-1 harmonic is the first harmonic to be folded down to DC. Thus, the advantage of using a large value for N is that the coefficient of the unwanted term is reduced by the factor $1/(2N-1)$. Therefore, it would seem the larger N can be made, the better performance would result.

However, there is a limit to the size of N. Referring to (5.18), the largest distortion term is centered at a frequency of $2\pi f_s/N$ rps or f_s/N Hz, where f_s is the sampling frequency. If it is assumed the maximum frequency deviation at the input is Δf and the loop is tracking:

$$\hat{\varphi}(kT)\Big|_{\max} \approx \varphi(kT)\Big|_{\max} \triangleq 2\pi\Delta f$$

Hence the spectral line of the first distortion term of (5.18) occurs (during maximum negative frequency deviation)

at

$$f_D = 2\pi f_s/N - 2\Delta f = f_s/N - 2\Delta f \qquad (5.19)$$

For this spectral line not to have an effect on the control properties of the loop, one wants the frequency, f_D, to lie outside the loop bandwidth. Thus, a design criteria is imposed that will determine how large N can be made. Letting B_L be the loop bandwidth yields, from (5.19),

$$f_s/N - 2\Delta f \geq B_L \qquad (5.20)$$

It has been shown that to minimize harmonic distortion in a phase locked loop, the error that appears at the output of the phase comparator should be much less than $\pi/2$. (In a paper by Osborne and Schilling [5-4], a value of $0.1\pi/2$ was used.) This result sets the bandwidth of the loop to be much larger than the input frequency deviation. However, a small signal at the phase comparator output results in a lower output signal-to-quantization noise ratio since the output in the first order phase locked loop is directly proportional to the phase error. Greco [5-5] showed that for sinusoidal modulation the best compromise exists when the loop bandwidth is set to 3.3 times the maximum frequency deviation. That is,

$$B_L = 3.3\Delta f \qquad (5.21)$$

Inserting (5.21) into (5.20) and solving for N, yields the criteria for the maximum value of N; viz,

$$N \leq f_s/5.3\,\Delta f \qquad (5.22)$$

An equality in (5.22) would result in the distortion term at the 3dB point of the loop bandwidth. Using a guard band of 2 between the distortion term and the loop bandwidth results in the following:

$$N \leq f_s/10.6\,\Delta f \qquad (5.23)$$

Knowing the maximum frequency deviation of the input signal, Δf, the bandwidth of the loop is found from (5.21). Logic speed limitations fix the maximum value of the sampling frequency, f_s. Hence, from (5.23) the maximum value of N is found.

In the experimental section of this chapter (section 5.4), oscillograms are shown of the spectral density at the output of the Digital Phase Locked Loop for several values of N. The results verify the previous discussion.

5.3 Noises and the Digital Phase Locked Loop

When the incoming FM signal to the Digital Phase Locked Loop is subjected to additive gaussian channel noise,

both thermal and impulse noises appear at the output as in the FM discriminator. The noises produced by A/D conversion and internal scaling also appear at the output and affect the output signal-to-noise ratio. To calculate the effect of these noises, it is convenient to linearize the loop so that the model appears as in Fig. 5-5. It has been shown by Greco [5-5] that this linearized model is a suitable approximation to the digitized loop.

5.3.1 Quantization Noise

There are two sources of quantization noise that affect the output of the Digital Phase Locked Loop. The first source is the quantization present in the A/D converter which because the loop is wide band with respect to the output low-pass filter, and the noise is white, appears inside the loop as shown in Fig. 5-5. The second noise source is the quantization that is formed by the scaling in the feedback path. This noise is represented by an additive white noise source also shown in Fig. 5-5.

Using this model, the quantization noise that appears at the output is found. Referring to Fig. 5-5, the input to the VCO, y(k) is

$$y(k) = \frac{1}{2^{n_1}} n_{q_1}(k) + \frac{1}{2^{n_1}} v_o(k) \qquad (5.24)$$

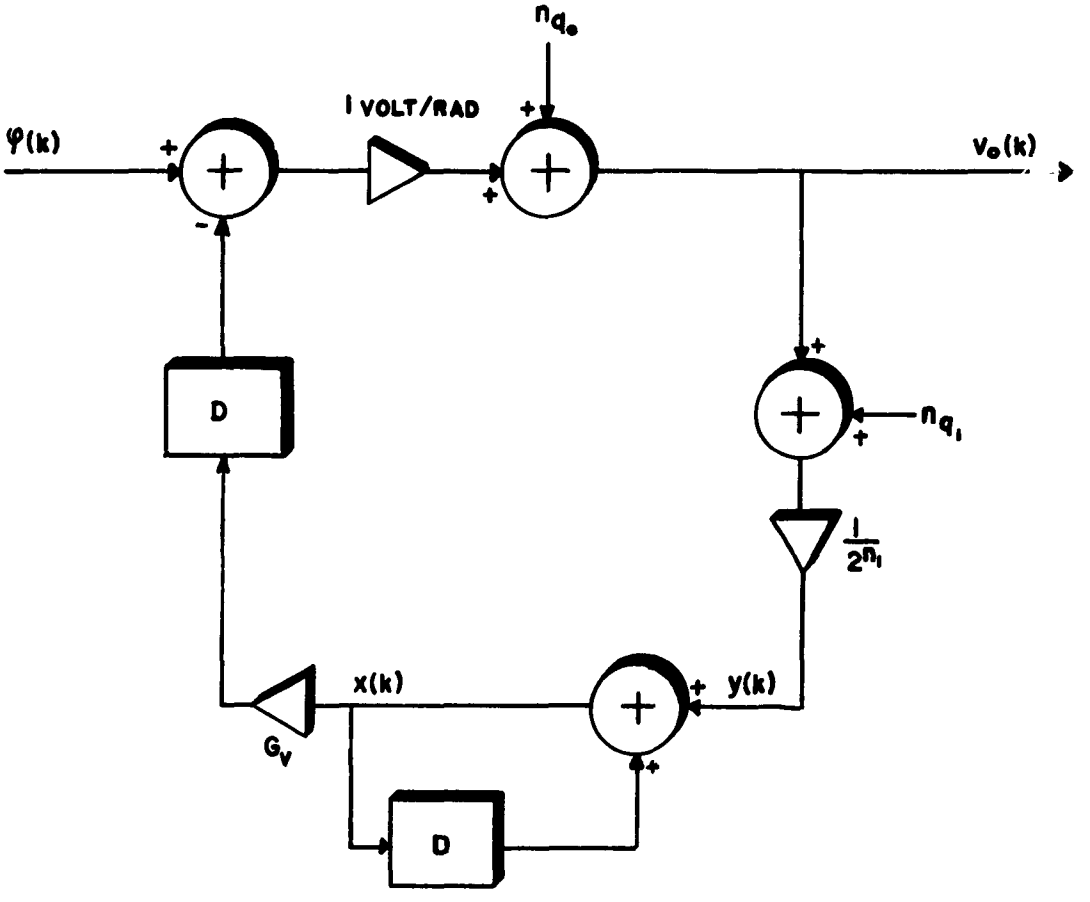


FIG. 5-5 LINEARIZED DIGITAL PHASE LOCKED LOOP SHOWING NOISES INTRODUCED BY QUANTIZATION

and the VCO output, x(k), is

$$x(k) = y(k) + x(k-1) \tag{5.25}$$

The output, $v_o(k)$ is given by (assuming no input)

$$v_o(k) = n_{q_o}(k) - G_v\, x(k-1) \tag{5.26}$$

where G_v is the VCO gain.

Combining (5.24), (5.25), and (5.26) and solving for the output, v_o, yields

$$v_o(k) - \left(1-\frac{G_v}{2^{n_1}}\right) v_o(k-1) = n_{q_o}(k) - n_{q_o}(k-1) - \frac{G_v}{2^{n_1}}\, n_{q_1}(k-1) \tag{5.27}$$

The output spectral density, assuming the noises are stationary and independent from sample to sample, is

$$G_{v_o}(f) = \frac{1}{\left| 1-\left(1-\frac{G_v}{2^{n_1}}\right) e^{-j\omega T} \right|^2} \left[2\, G_{n_{q_o}}(f) + \left(\frac{G_v}{2^{n_1}}\right)^2 G_{n_q}(f) \right] \tag{5.28}$$

The next task is to characterize $G_{n_q}(f)$. If the input signal can assume any value with equal probability, the quantization error is then any value between $\pm S/2$ with equal probability, where S is the step size of the A/D converter. After scaling, referring to Fig. 5-5, the noise becomes

$$n_q(k) = \frac{1}{2^{n_1}}\, n_{q_o}(k) + \frac{1}{2^{n_1}}\, n_q(k)$$

Since the step size remains fixed, this noise must also vary between $\pm S/2$ with equal probability. Therefore, the noise after scaling has the same power spectral density as that of the A/D converter. Hence,

$$G_{n_{q_o}}(f) = \frac{1}{2^{2n_1}} G_{n_{q_o}}(f) + \frac{1}{2^{2n_1}} G_{n_q}(f) \qquad (5.29)$$

Inserting (5.29) into (5.28) yields,

$$G_{v_o}(f) = \frac{1}{\left| 1-\left(1- \frac{G_v}{2^{n_1}}\right)e^{-j\omega T} \right|^2} \left[(2 + G_v^2 - \frac{G_v^2}{2^{2n_1}} \right] G_{n_{q_o}}(f)$$

When solving for the output in terms of power, note that for the frequency range of interest, $\omega << 1/T$. (For example, the system under consideration operates with $\omega_M = 6.3 \times 10^2$ rps while $1/T = 5 \times 10^4$.) Therefore,

$$G_{v_o}(f) = 2^{2n_1} G_{n_{q_o}}(f) \left[\frac{2}{G_v^2} + 1 - \frac{1}{2^{2n_1}} \right]$$

Now,

$$G_{n_{q_o}}(f) = \frac{\overline{|P(f)|^2}}{T} = \frac{S^2 T^2/12}{T} = \frac{S^2 T}{12}$$

Hence,

$$N_q = \frac{2^{2n} f_M T S^2}{6} \left[\frac{2}{G_v^2} + 1 - \frac{1}{2^{2n_1}} \right] \qquad (5.30)$$

where N_q is the output noise power caused by quantization.

5.3.2 Thermal Noise in the Digital Phase Locked Loop

When thermal noise is added to the linearized phase locked loop, the output is expressed as [similar to (5.17)] ,

$$v_o(k+1) - v_o(k) + \frac{G_v}{2^{n_1}} v_o(k) = \frac{y(k+1)}{A} - \frac{y(k)}{A} \qquad (5.31)$$

where

A = carrier amplitude

and $y(k)$ = noise amplitude at the sampling instant k [5-6] .

Using the approximation that $\omega << \frac{1}{T}$ in the region of interest, the output power spectral density becomes,

$$G_{v_o}(f) = \frac{2^{2n_1}}{G_v} \left[G_{n_{th}}(f) \right]$$

To find $G_{n_{th}}(f)$, first note that

$$R_y[kT, (k-n)T] = 2R_y(kT) - R_y[(k-n)T] - R_y[(k+n)T]$$

Therefore,

$$G_{n_{th}}(f) = \frac{G_y(f)}{A^2} \left[2 - e^{-j\omega T} - e^{j\omega T} \right]$$

$$= \frac{4G_y(f)}{A^2} \left[\sin \omega T/2 \right]^2$$

or,

$$G_{n_{th}}(f) = \frac{4G_y(f)}{A^2} \left[\frac{\sin \omega T/2}{\omega T/2} \right]^2 \left[\frac{\omega T}{2} \right]^2$$

Again, in the region of interest, ωT is small. Hence

$$G_{n_{th}} \doteq \frac{\omega^2 T^2 G_y(f)}{A^2}$$

Setting the noise power spectral density, $G_y(f) = \eta$ in the IF filter, the output noise power becomes

$$N_{th} = \frac{2^2 n_1}{G_v^2} \cdot \frac{4}{3} \cdot \frac{\pi^2 f_M^2 T^2}{S_{i/\eta} f_M} \qquad (5.32)$$

where $S_i = A^2/2$ and N_{th} is the output noise power produced by the additive gaussian noise at the input.

5.3.3 Impulse Noise in the Digital Phase Locked Loop

When a noise spike occurs on an FM carrier, the phase undergoes a 2π excursion [5-6]. Since the input is sampled, the phase can be represented by,

$$\varphi(k) - \varphi(k-1) = \alpha_k T \qquad (5.33)$$

where α_k in the most general case is a random variable, and T is the sampling period. A representation of the input phase versus time during a noise spike is shown in Fig. 5-6.

Let $p(k) = \varphi(k) - \varphi(k-1)$ so that the Fourier transform of p(k), P(f), is given by,

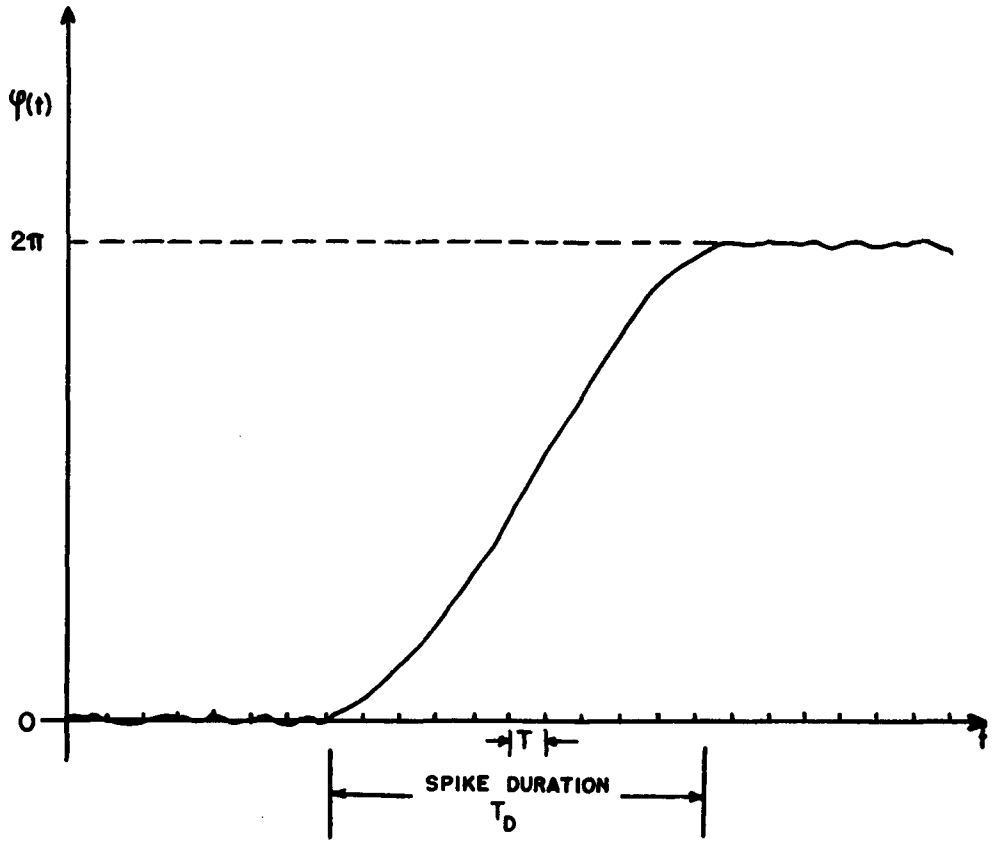


FIG. 5-6 THE PHASE OF AN FM WAVE DURING AN OCCURRENCE OF A NOISE SPIKE

$$P(f) = \begin{cases} \sum_{k=1}^{K} p(k)\, e^{-j\omega kT}\, T; & \text{during the spike } (1 \le k \le K) \\ 0 \qquad\qquad ; & \text{elsewhere} \end{cases}$$

The power spectral density of the spike, $\overline{|P(f)|^2}$, is then,

$$\overline{|P(f)|^2} = R_e \left\{ T^2 \sum_{k=1}^{K} \sum_{i=1}^{K} p(k)p(i)\, e^{-j\omega kT}\, e^{j\omega iT} \right\}$$

$$= T^2 \left\{ \sum_{k=1}^{K} \sum_{i=1}^{K} \overline{p(k)p(i)} \left[1 - 2 \sin^2 \frac{\omega T}{2} (k-i) \right] \right\} \qquad (5.34)$$

In the frequency range of interest, $2 \sin^2 [\omega T (k-i)/2]$ becomes a small quantity. To see this, note the maximum value will occur when ω is a maximum and $(k-i)$ is the maximum value, $(K-1)$. The maximum value of ω in the region of interest is $2\pi f_M$, where f_M is the frequency cutoff of the output low-pass filter. The duration of the impulse or spike, KT, is known to be (in the worst case),

$$KT = 1/B_{IF}$$

where B_{IF} is the IF band-pass filter bandwidth. Therefore,

$$2 \sin^2[\omega T(k-i)/2] \Big|_{\max} = 2 \sin^2 (2\pi f_M T(K-1)/2)$$

$$= 2 \sin^2 \left[\pi f_M \frac{1}{B_{IF}} - T \right] \qquad (5.35)$$

Using Carson's Rule for bandwidth, i.e., $B_{IF} = 2(\beta+1) f_M$, and noting that $K >> 1$, yields for (5.35),

$$2 \sin^2 [\omega T(k-i)/2] \Big|_{max} = 2 \sin^2\left[\frac{\pi}{2(\beta+1)}\right]$$

For $\beta \geq 3$, $2 \sin^2[\pi/2(\beta+1)] \leq 0.1$. Hence for $\beta \geq 3$ (from (5.34)),

$$\overline{|P(f)|^2} = T^2 \sum_{k=1}^{K} \sum_{i=1}^{K} \left\{\overline{p(k)p(i)}\right\} ; \; |f| \leq f_M \qquad (5.36)$$

Since the phase changes by 2π when a spike occurs,

$$\sum_{k=1}^{K} p(k) = \sum_{k=1}^{K} \alpha_k T = 2\pi \qquad (5.37)$$

Inserting the deterministic quantity of (5.37) into (5.36) gives the following result for the spectral density of a single spike:

$$\overline{|P(f)|^2} = 4\pi^2 T^2 ; \quad |f| \leq f_M \qquad (5.38)$$

For spikes occurring at an average rate $1/T_{ave}$, (5.38) is modified to read,

$$G_s(f) = \frac{1}{T_{ave}} \overline{|P(f)|^2} = \frac{4\pi^2 T^2}{T_{ave}} \qquad (5.39)$$

It has been found that the first order phase locked loop yields approximately the same frequency of spikes as that of a discriminator [5-4]. Using T_{ave} for a discriminator [5-6], and a frequency offset for an

input signal, the output noise power caused by noise spikes is

$$N_s = \left[\frac{2^{2n_1}}{G_v^2}\right] 8\pi^2 f_M T^2 \, |\Delta f| \cdot \exp(-S_1/\eta B_{IF}) \qquad (5.40)$$

where Δf is the input frequency offset.

5.3.4 Output Signal Power

The digital phase locked loop responds to an input frequency offset with a transient and steady state response. For an offset of $\Delta\omega_1$ rps.,

$$\varphi(k) - \varphi(k-1) = \Delta\omega_1 T$$

where T is the sampling period. Therefore, from previous arguments the output power spectral density is,

$$G_{v_o}(f) = \frac{2^{2n_1}}{G_v^2} (\Delta\omega_1 T)^2$$

Therefore the output signal power (since the spectral density is an impulse at zero frequency) is,

$$S_o = \frac{2^{2n_1}}{G_v^2} (\Delta\omega_1 T)^2 \qquad (5.41)$$

(Note for sinusoidal modulation, $\Delta\omega_1$ becomes $\Delta\omega_1/\sqrt{2}$)

5.3.5 Output Signal-to-Noise Ratio

The output signal-to-noise ratio is the basis used for the system performance. Combining (5.30), (5.32), (5.40) (5.41), results in the theoretical output signal-to-noise

ratio of the digital phase locked loop. The result for an input frequency offset is,

$$\frac{S_o}{N_o} = 24\pi^2 (\Delta f)^2 \Big/ \left[\frac{f_M S^2}{T} \left(2 + G_v^2 - \frac{G_v^2}{2^{n_1}} \right) + \frac{8\pi^2 f_M^2}{S_i/\eta f_M} + 48\pi^2 f_M |\Delta f| \cdot \exp\left(- \frac{S_i}{\eta B_{IF}} \right) \right] \quad (5.42)$$

where,

S = A/D step size

G_v = VCO gain

$1/2^{n_1}$ = feedback gain

Δf = input frequency offset

T = sampling period

B_{IF} = IF bandwidth

S_i = input signal power

η = one sided noise spectral density

f_M = low-pass filter frequency cutoff

Curves of (5.42) and experimental results are displayed in Section 5.4. Using the previously derived design criteria the harmonic distortion is much smaller than any other noise term and is omitted in (5.42).

5.4 Experimental Results

The Digital Phase Locked Loop described by the block diagram in Fig. 5-1 was constructed with the use of DTL logic elements. The sampling rate was fixed at 50 kHz thereby allowing sufficient time for processing. The implemented system was tested using the facility of Fig. 4-10 (facility for the FM Discriminator), for modulation indexes, β , of 3 and 10 for frequency offsets (DC outputs) and sinusoidal modulation.

5.4.1 Loop Bandwidth and Determination of N

From the discussion in Sec. 5.2.4 it is seen that the best results are obtained when the factor N is large. However, for a fixed sampling frequency (limited by the logic speed), setting N large forces the deviation, Δ f, to be small [refer to (5.23)] . For experimental purposes, the deviation, Δ f, was chosen to be 300 Hz. The bandwidth of the loop is then by (5.21) to be 1000 Hz.

Using (5.24), (5.25) and Fig. 5-5, the closed loop transfer function of the linearized Digital Phase Locked Loop is given by

$$H(j\omega) = \frac{G}{1 - (1-G)\, e^{-j\omega/f_s}} \qquad (5.43)$$

where f_s is the sampling frequency and G is the loop gain. Using the first coefficient of the Fourier expansion of

the squarewave VCO, the loop gain becomes,

$$G = \frac{4\ G_v}{\pi\ 2^{n_1}} \qquad (5.44)$$

where G_v is the VCO gain and $1/2^{n_1}$ is the feedback gain.

The magnitude of the transfer function given in (5.43) is plotted both analytically and experimentally in Fig.5-7 for $G_v = \pi/2.5$, and $1/2^{n_1} = 1/16$. By examination of the figure, it becomes apparent that the linearization of the loop model is indeed a valid assumption.

From (5.23) it is seen that for f_s = 50 kHz and Δf = 300 Hz,

$$N \leq 16$$

The oscillograms in Figs. 5-8a,b,c show the spectral density from 0 to 1000 Hz of the Digital Phase Locked Loop for N = 2,4,8,16 and 32 when a 100 Hz sinuosoid modulates the FM carrier. Note the in-band distortion decreases as N increases and that for N = 32 distortion terms appear inside the loop bandwidth. Clearly, the best results are obtained for N = 16 and it is this configuration that was used for the remaining experimental discussion.

5.4.2 Response to Frequency Offsets

In the steady state, the Digital Phase Locked Loop tracks any frequency input that will produce an error less than $\pi/2$ (greater values yield instability). Therefore, frequency offsets of up to 675 Hz (instead of 300 Hz as

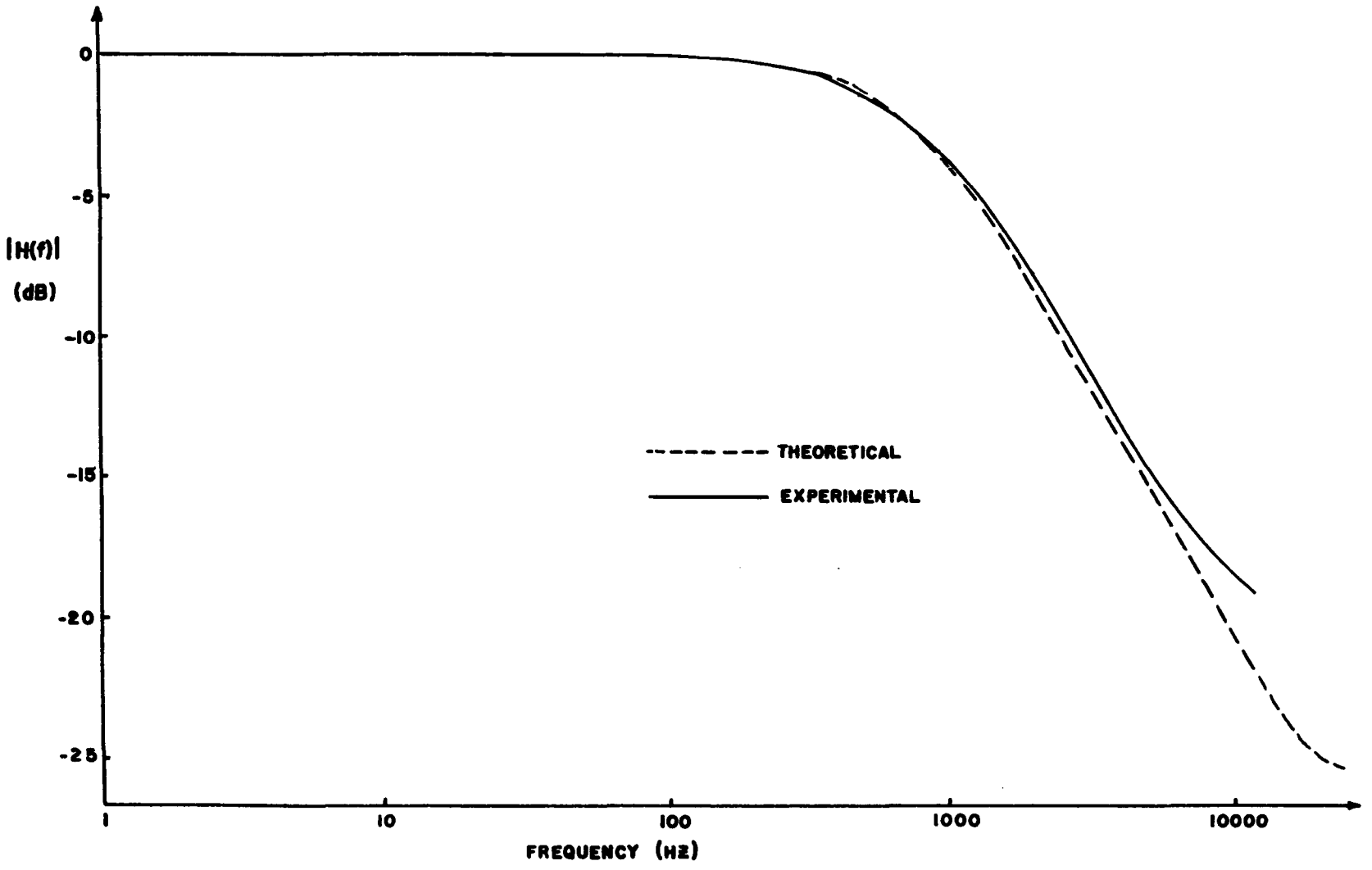
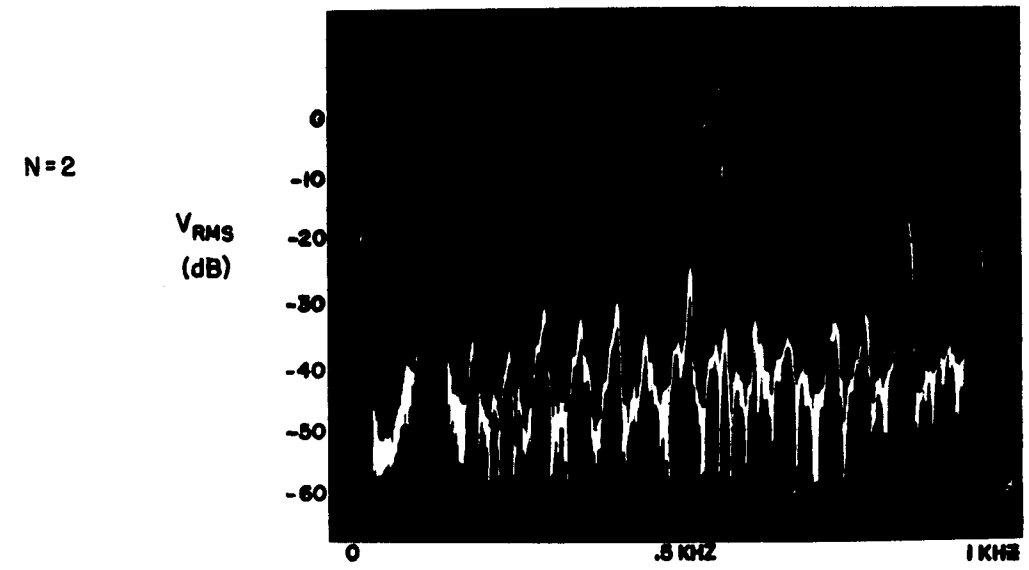


FIG. 5-7 EXPERIMENTAL AND THEORETICAL PLOT OF THE DIGITAL PHASE LOCKED LOOP BANDWIDTH



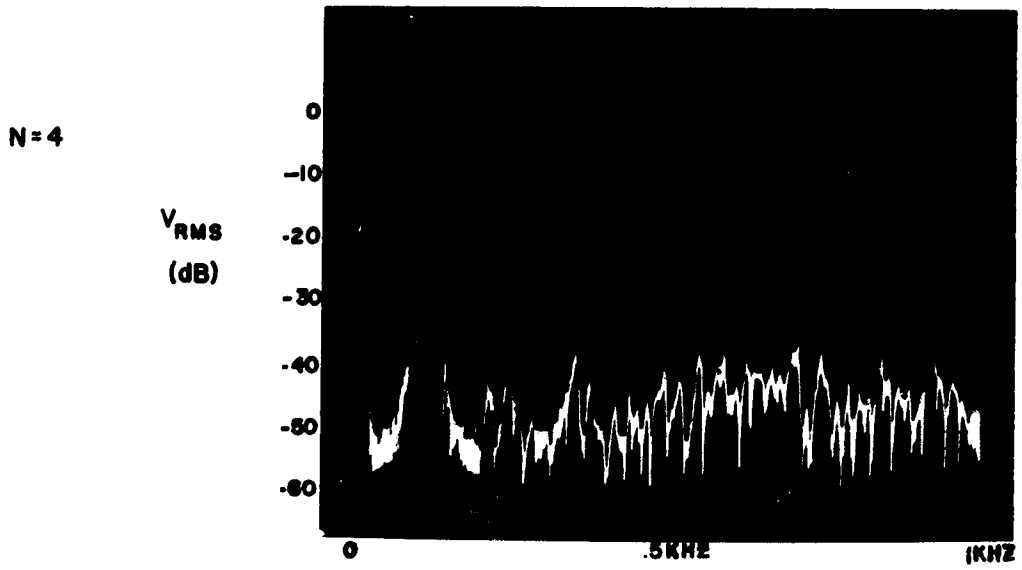
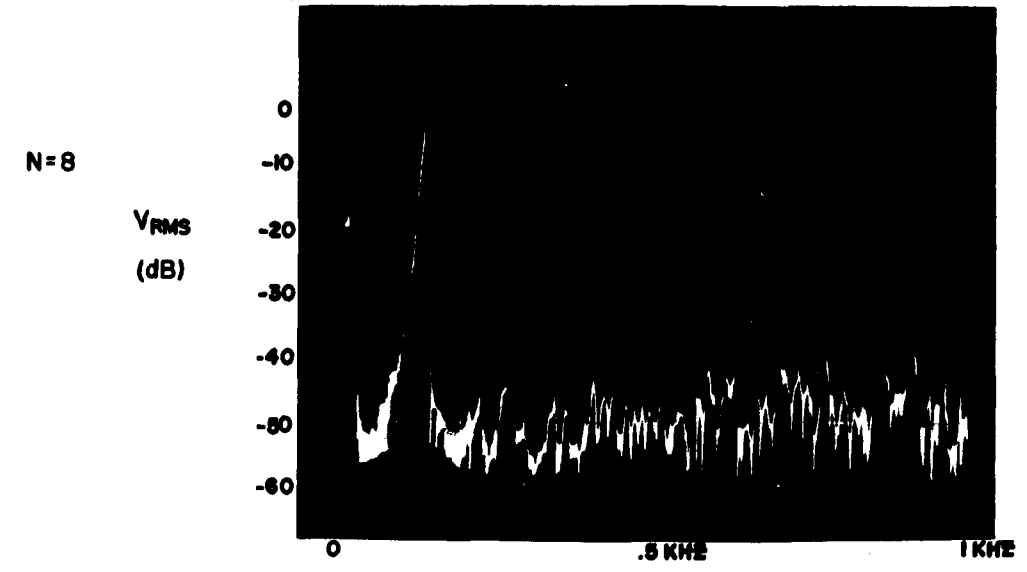


FIG.5-8a SPECTRAL DENSITY OF THE LOOP OUTPUT FOR N=2,4 (f_l=100HZ)



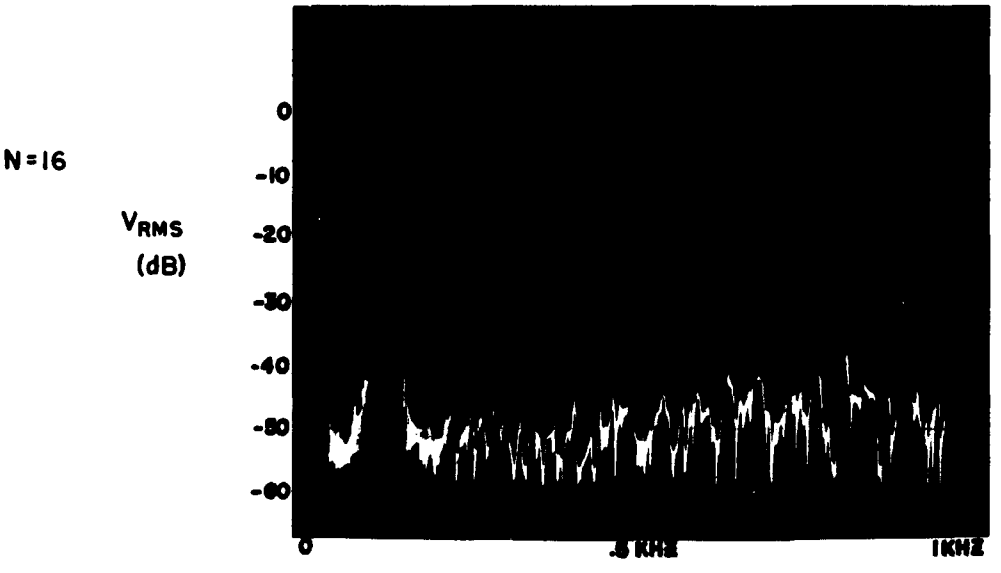


FIG. 5-8b SPECTRAL DENSITY OF LOOP OUTPUT FOR N=8,16 (f_i =100 Hz)

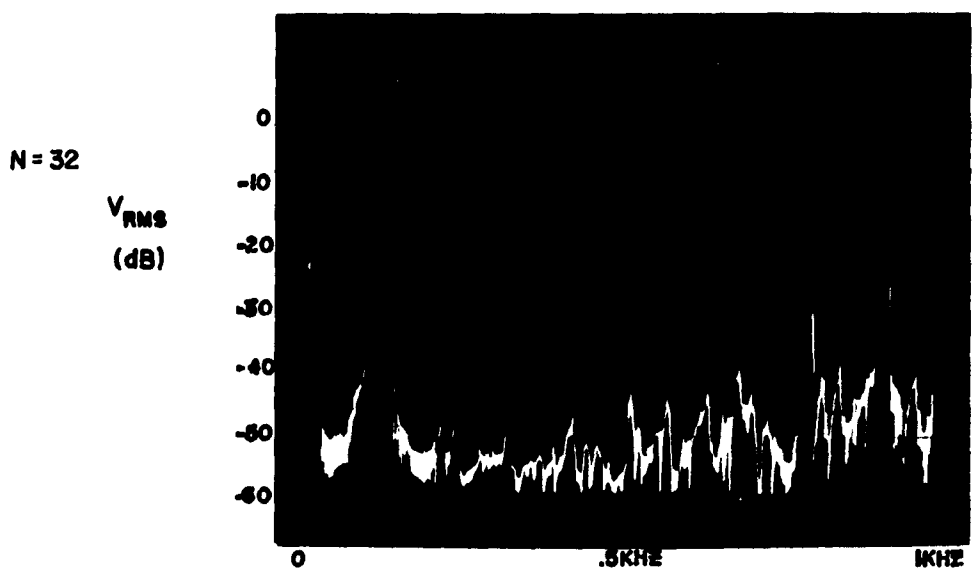


FIG. 5-8c SPECTRAL DENSITY OF THE LOOP OUTPUT FOR N=32 SHOWING THE APPEARANCE OF A HARMONIC WITHIN THE LOOP BANDWIDTH

for sinewave modulation) were used in the experimentation.

It is interesting to note that the distortion term that is folded down to DC from (5.18)(the last term shown), contributes a 2N harmonic of the offset that appears at the output of the loop. For a low-pass filter cutoff of f_M, this distortion term will appear if

$$2N\,\Delta f \leq f_M$$

where Δf is the input frequency offset. The experimental results were obtained for N = 16 and a maximum f_M of 225 Hz. Therefore a criterion for the input where a 2N harmonic does not appear is,

$$\Delta f \geq \frac{f_M}{2N} = 7 \text{ Hz}$$

Therefore, including positive and negative offsets, the deviation is restricted so that

$$\begin{aligned} 7 \text{ Hz} \leq \Delta f \leq 675 \text{ Hz} \quad & \text{for positive offsets} \\ -7 \text{ Hz} \geq \Delta f \geq -675 \text{ Hz} \quad & \text{for negative offsets} \end{aligned} \tag{5.45}$$

The loop was tested with $\beta = 3$ and $\beta = 10$ for a frequency offset and the following fixed parameters:

$S = 10^{-2}$ volts

$G_v = \pi/2.5$ rad/volt

$1/2^{n_1} = 1/16$

$\Delta f = 675$ Hz

$T = 20 \times 10^{-6}$ seconds

$B_{IF} = 2(\beta + 1) f_M$

$S_i = 2$ (volts)^2

$f_M = 67.5$ Hz, 225 Hz

The output signal-to-noise ratio versus carrier to noise ratio is plotted along with the theoretical results of (5.42) in Fig. 5-9. Note the high correlation between the theoretical and experimental curves. As expected, at higher carrier-to-noise ratios the output signal-to-noise ratio approaches a constant, since the quantization noise dominates. Note at very high input carrier-to-noise ratios, the experimental results show a higher output signal-to-noise ratio than the theoretical prediction. This phenomenon is caused by the deterministic nature of the input signal. The development of quantization noise performance assumed a random input which is the case when noise is added to a signal. However, in the absence (or near absence) of input noise, the output signal-to-noise ratio will be governed by the system noise.

The PLL is usually tested using either sinusoidal modulation or a fixed frequency offset. Since the system is quantized, a slowly varying sinusoid (the frequency of the sinusoid is typically much less than the bandwidth of the loop) will dwell on the same quantization level for many sampling periods. Therefore, the use of an input frequency offset simulates the sinusoidal signal. Furthermore, a frequency offset simulates an M-ary FSK system.

5.4.3 Response to Sinusoidal Modulation

When the FM carrier is modulated with a sinusoid,

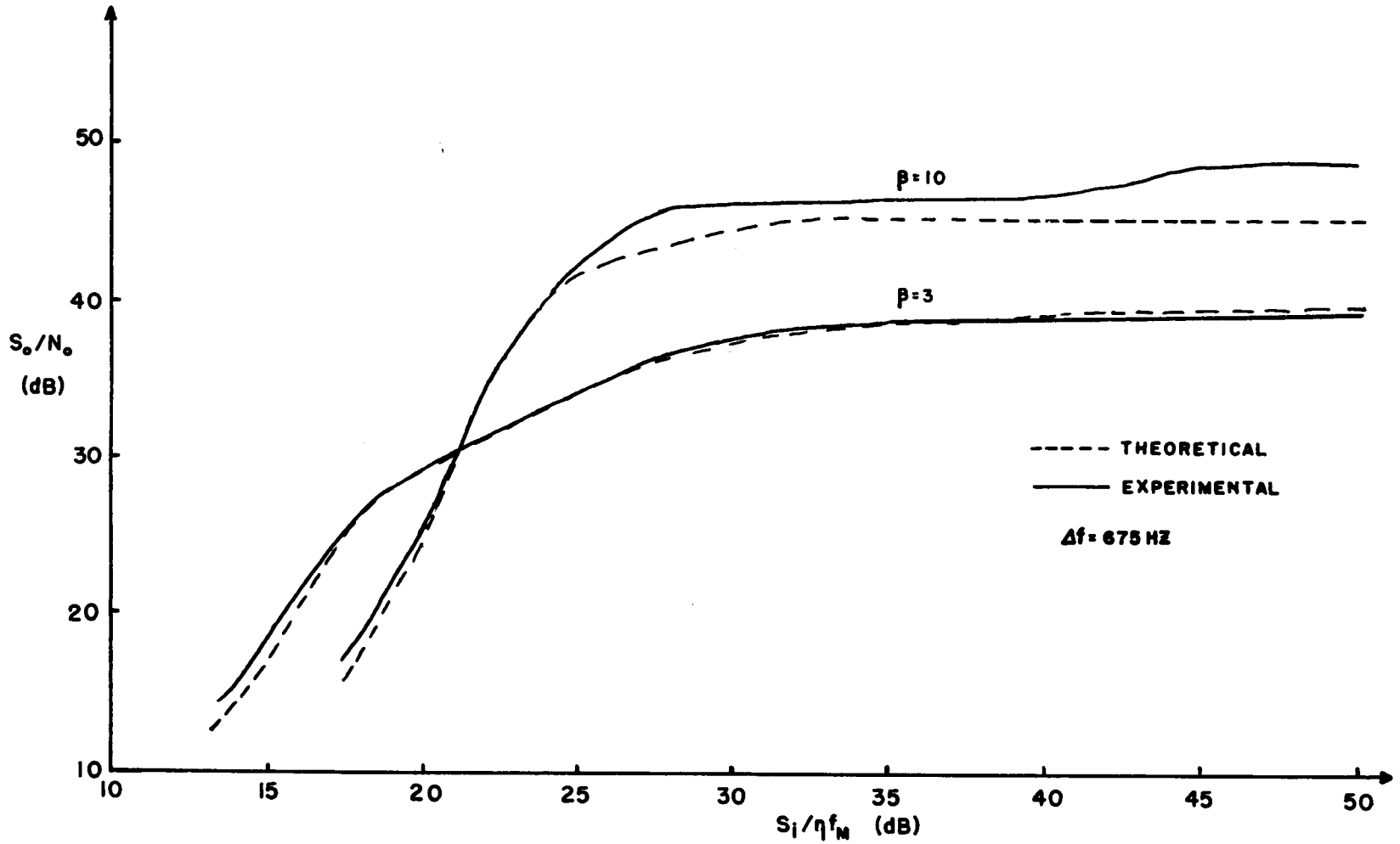


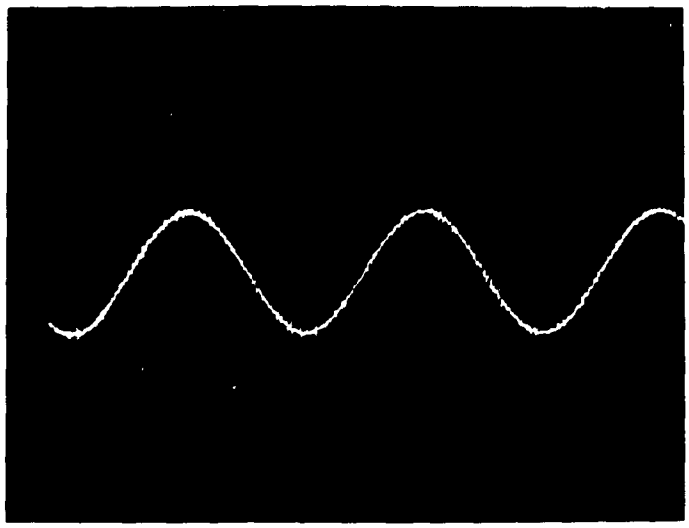
FIG. 5-9 FIRST ORDER DIGITAL PHASE LOCKED LOOP RESPONSE TO A FREQUENCY OFFSET

the output signal-to-noise ratio obeys the same formula for a frequency offset, (5.42), except that the deviation, Δf, becomes the rms deviation, $\Delta f/\sqrt{2}$.

The Digital Phase Locked Loop was tested to determine its output signal-to-noise ratio for a sinusoidal modulated carrier. Again modulation indexes of $\beta = 3$ and $\beta = 10$ were used. Figure 5-10a displays the output of the loop for an input carrier-to-noise ratio, $S_i/\eta f_M$, of 16 dB. Note the thermal noise that appears with the sinusoid. For a carrier-to-noise ratio of 13dB, the loop operates below threshold and spike or impulse noise appears at the output as shown in Fig. 5-10b.

The output signal-to-noise ratio of the loop is shown in Fig. 5-11. As is seen, close correlation exists between the analytical and experimental results. Again, at very high carrier-to-noise ratios, the output signal-to-noise ratio is dominated by system noise as in the previous section.

a) ABOVE THRESHOLD
$S_i/\eta f_M = 16\,dB$



b) BELOW THRESHOLD
$S_i/\eta f_M = 13\,dB$

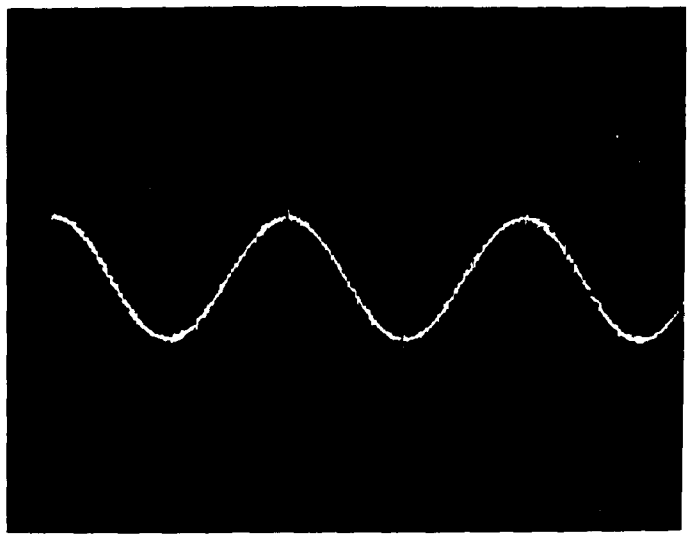


FIG.5-10 DIGITAL PHASE LOCKED LOOP RESPONSE TO SINUSOIDAL MODULATION AND CHANNEL NOISE; a) ABOVE THRESHOLD, b) BELOW THRESHOLD ($\beta=3$)

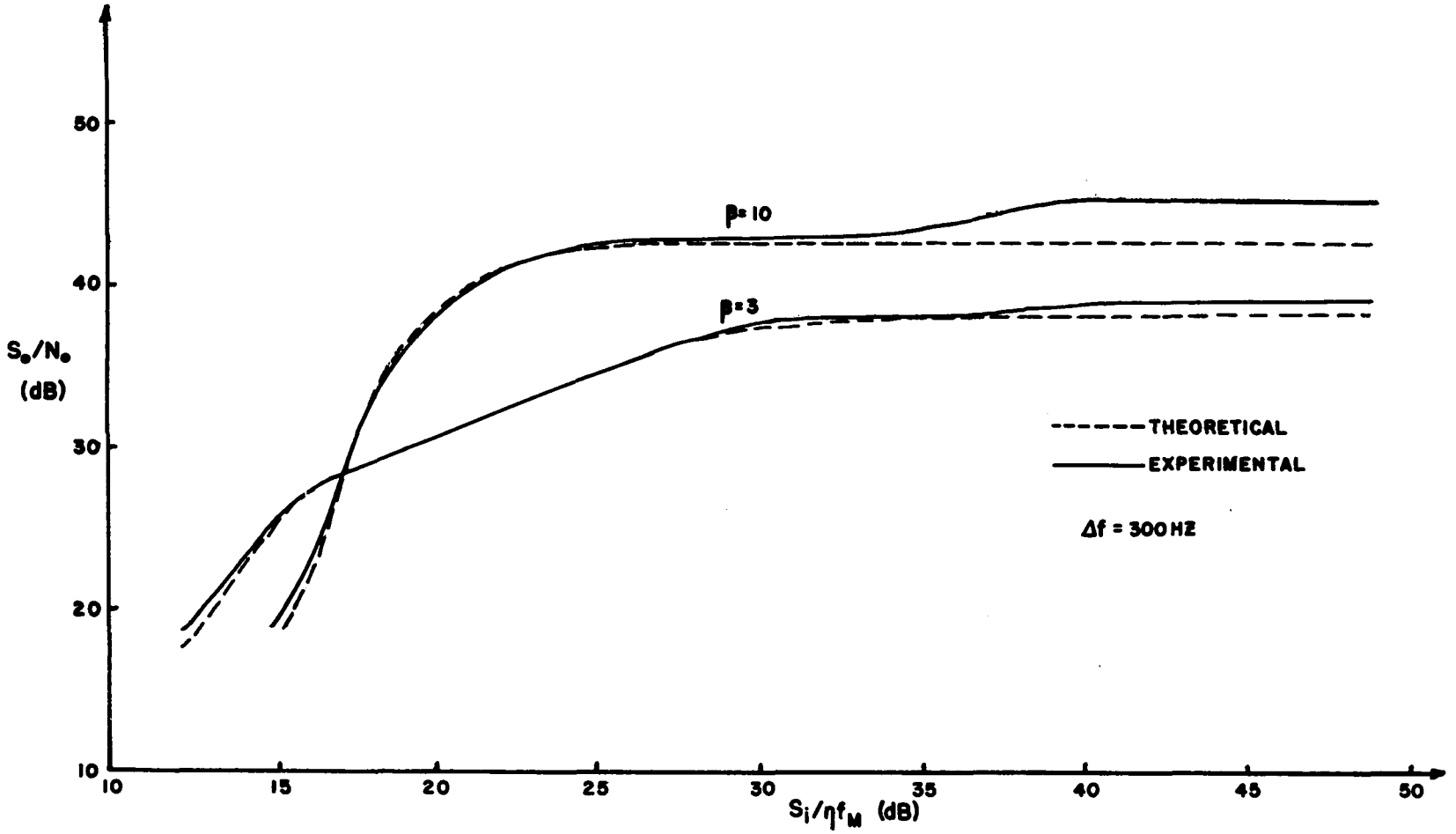


FIG.5-11 DIGITAL PHASE LOCKED LOOP RESPONSE TO SINUSOIDAL MODULATION

Chapter 6

CONCLUSIONS

6.1 Summary

Three all digital implemented structures comprising sections of communications systems were designed, constructed, and analyzed theoretically and experimentally. The primary measure of performance was the output signal-to-noise ratio. Results were obtained both experimentally and theoretically and design criteria for each system are stated.

6.1.1 Delta Modulation

It was stated and shown experimentally that a linear delta modulator suffered limited dynamic range of output signal-to-noise ratio when the input signal power varied. By approximating a previously developed optimum scheme, two realizations of an adaptive delta modulator are found. With the use of extended arithmetic, it was shown that each system produced an output signal-to-noise ratio relatively independent of input signal power.

One system (α =, $\beta = 0.5$) showed adaptability to video signals while the second system ($\alpha = 1$, $\beta = 0.0$) was more suitable to speech inputs. Although subjective testing of video signals was not performed (the subject remains as a new area of research), voice tapes were produced that served as a subjective test of the speech system. For an error free channel, inaudible distortion was detected using

the Digital Adaptive Delta Modulator, and zero loss in intelligibility was obtained at sampling rates as low as 19.2 kilobits per second.

6.1.2 Digital Discrimination

Utilizing zero-crossing detection, equations and generalized design procedures were developed for an All Digital FM Discriminator. The output signal-to-noise ratio is determined both theoretically and experimentally for several design examples. It was found analytically that the digital system performed similar to existing differentiating and zero-crossing types of discriminators. The experimental results also proved this point.

6.1.3 The Digital Phase Locked Loop

The All Digital Phase Locked Loop using a squarewave VCO algorithm was implemented and tested for output signal-to-noise ratio. It was shown that by manipulation of the sampling frequency, the performance of the loop could be predicted by a linearized model.

Design criteria and constraints are presented that determine the loop bandwidth and output noise dependent on the signal parameters. Although the message signal was band-limited to the subaudio range in the constructed system ($f_M \leq 100Hz$), the use of state of the art devices would result in the demodulation of voice transmission.

6.2 Suggestions for Future Work

6.2.1 Delta Modulation

The theoretical and experimental results of the performance of the Digital Adaptive Delta Modulator assumed an error-free transmission channel. Studies should be made on the degradation of performance when the binary channel is corrupted with thermal noise simulating space and deep space conditions.

The implemented system employed 8, 9, and 10 bit accuracies producing approximately a 6dB increase in dynamic range for each bit extension of the word length. Current A/D converters have 15 bit accuracies; hence an implemented scheme with extended arithmetic should be attempted to verify the extension of dynamic range.

The adaptive scheme described in Chapter 3 should be applied to other existing types of linear delta modulation currently in the feasibility stage. These existing types include the multilevel modulator [6-1] and the multiplexed linear delta modulator [6-2]. Each of these systems increases the output signal-to-noise ratio but has dynamic range limitations.

It was demonstrated that the adaptive scheme having the internal parameters, α and β, equal to 1 and $\frac{1}{2}$ respectively, reproduced sharp transitions of the input signal with good fidelity. This fact intimates that such an adaptive scheme would be suitable for video reproduction

and the subject should be pursued in the future.

6.2.2 Digital FM Discriminator

There is no memory involved from one computation interval to the next in the Digital FM Discriminator. Hence, the demodulation of many FM signals involves merely an analog switch on the input and output of the system. The effects of multiplexing on the parameters of the system should therefore be investigated.

When transmitting a binary FSK signal, it is well known that the use of a matched filter yields an optimum means of detection. If the frequency divider described in Chapter 3 is made large enough so that only one computation is performed for each transmitted bit of the FSK signal, the Digital Discriminator doubles as a digital matched filter.

6.2.3 Digital Phase Locked Loops

In a paper by Osborne and Schilling [6-3], it was shown that threshold extension can be obtained by augmenting the loop to second and third orders. With the advent of the feasibility of a totally digitized loop, higher order loops should be implemented and investigated for threshold extension.

To reduce third harmonic distortion it was found that

the error appearing at the output of the digital multiplier should be contained to small values. However, if the loop is allowed to reach steady state (which it does for a frequency offset input), the error can be as large as $\pi/2$ (greater values than $\pi/2$ yield cycle slipping). Therefore, the loop is capable of demodulating an M-ary FSK signal, and the performance of the loop for this type of input should be investigated.

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